BIDIRECTIONAL TRANSCEIVER MODULE FOR 8-28 GHZ PHASED ARRAY APPLICATIONS AND A NOVEL METHOD TO REDUCE AMPLITUDE AND PHASE ERRORS IN VARIABLE GAIN AMPLIFIERS

by
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ABSTRACT

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Keywords: wideband, transceiver, phased array, bidirectional, VGA

Next-generation communication applications utilize phased arrays with thousands of transceiver modules. The area and cost are as crucial as the performance of the transceiver module because of the large-scale integration. The technology and architecture of the module are critical and define the specifications of the sub-blocks. Each sub-block has a vital role to play and comes with its challenges. First, a novel technique is presented in this thesis to reduce the amplitude and phase errors in current steering variable gain amplifiers. This technique is implemented in a wideband variable gain amplifier using IHP 0.13 μm SiGe BiCMOS technology. It can be utilized in unidirectional transceiver architectures to control the amplitude of the signal with minimum error and high resolution. Also, low phase error, power consumption, and noise figure are achieved in a small chip area. Second, a bidirectional transceiver module operating between 8 to 28 GHz is presented. SiGe BiCMOS technology is preferred due to its high performance and integration with CMOS. The module consists of a bidirectional common chain and an RF front-end circuit. The common chain contains a true time delay, attenuator, and bidirectional amplifier, to control the amplitude and time delay of the system. The RF front-end includes a power amplifier, low noise amplifier, and single-pole double-throw switch to transmit high power and receive with low noise figure. Design and implementation of each block will be given, and the combined front-end will also be presented. Each sub-block has comparable or better performance with the state-of-the-art works in the literature.

ÖZET

8-28 GHZ FAZ DİZİLİ SİSTEMLER İÇİN ÇİFT YÖNLÜ ALICI/VERİCİ MODÜLÜ VE DEĞİŞKEN KAZANÇLI KUVVETLENDİRİCİLERDEKİ GENLİK VE FAZ HATALARINI DÜŞÜRECEK ÖZGÜN YÖNTEM

KUTAY ALTINTAŞ

ELEKTRONİK MÜHENDİSLİĞİ YÜKSEK LİSANS TEZİ, AĞUSTOS 2022

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Anahtar Kelimeler: genişbant, alıcı/verici, faz dizili sistem, çift yönlü, VGA

Yeni nesil haberleşme uygulamaları, binlerce alıcı-verici modülünden oluşan faz dizili yapıları kullanır. Alan ve maliyet, büyük ölçekli entegrasyon nedeniyle alıcı-verici modülünün performansı kadar önemlidir. Modülün teknolojisi ve mimarisi alt blokların özelliklerini tanımlayacağı için kritiktir. Her alt bloğun kritik bir görevi ve zorlukları vardır. Bu tezde, ilk olarak, değişken kazançlı kuvvetlendiricilerdeki genlik ve faz hatalarını azaltmak için yeni bir yöntem sunulmaktadır. Bu yöntem, genişbantlı bir değişken kazançlı kuvvetlendiricide IHP'nin 0.13 μm SiGe BiCMOS teknolojisi kullanılarak uygulanmıştır. Sinyalin genliğini minimum hata ve yüksek çözünürlükle kontrol etmek için tek yönlü alıcı-verici mimarilerinde kullanılabilir. Ayrıca, küçük bir çip alanında düşük faz hatası, güç tüketimi ve gürültü figürü elde edilir. İkinci olarak, 8 ila 28 GHz arasında çalışan çift yönlü bir alıcı-verici modülü sunulmaktadır. Yüksek performansı ve CMOS ile entegrasyon kabiliyeti sebebi ile SiGe BiCMOS teknolojisi tercih edilmiştir. Modül, çift yönlü bir ortak hat ve bir RF ön uç devresinden oluşur. Ortak hat, sistemin genliğini ve zaman gecikmesini kontrol etmek için doğru süre geciktirici, zayıflatıcı ve çift yönlü kuvvetlendirici içerir. RF ön uçta bir güç kuvvetlendiricisi, düşük gürültülü kuvvetlendirici ve tek kutuplu çift atışlı anahtar, yüksek gücü iletmek ve düşük gürültü ile almak için bulunur. Her bloğun tasarımı ve uygulaması verilecek ve birleştirilmiş ön uç devresi de sunulacaktır. Her alt blok, literatürdeki en son çalışmalarla karşılaştırılabilir veya daha iyi performansa sahiptir.

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To my family...
Aileme...

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1. INTRODUCTION

1.1 Phased Arrays

The recent generation Radio Detection and Ranging (RADAR) systems utilize phased arrays due to its superior performance compared to single antenna structures. Phased arrays contain several antenna elements where each elements phase is controlled independently to achieve a better performance. Fig. 1.1 shows a example phased array system with four antennas. The phase of each radiating element is controlled by the transmit/receive (T/R) module and the main beam's direction can be changed. Main beam is the addition of these signals coming from different antennas. This way, main beam can be steered electronically. In earlier RADAR applications, a mechanically rotating antenna was used to scan the environment which was slow. Use of phased arrays allows electronic scanning of the environment which is very fast with hundreds of scans per second, compared to mechanical scanning. For both next generation commercial and military communication applications, phased arrays are used for achieving high data rate and reliability (Mailloux, 2017).

Number of elements in a phased array system impacts the performance dramatically. For the transmitter, the addition of each elements output powers enables a high power radiation which achieves long range communication. Very high output powers cannot be reached with single T/R modules using current Complementary Metal-Oxide-Semiconductor (CMOS) and Silicon Germanium (SiGe) technologies due to the scaling down the device sizes and having low breakdown voltages. For the receiver, phased arrays achieve higher signal-to-noise ratio (SNR) hence lower noise figure (NF) because signals add up to each other where the uncorrelated noise contribution of each element does not. Also, high number of elements result in very high array gains. Increasing the number of elements is beneficial for both transmitter and receiver chains, however it does have a limitation. Today, thousands

of T/R modules are utilized in a single phased array and implemented on a single chip. The cost of the chip is increasing dramatically with the number of elements. As the area of the system increases, the yield and repeatability of integrated circuit (IC) manufacturing decreases (Jeon, Wang, Wang, Bohn, Natarajan, Babakhani & Hajimiri, 2008).

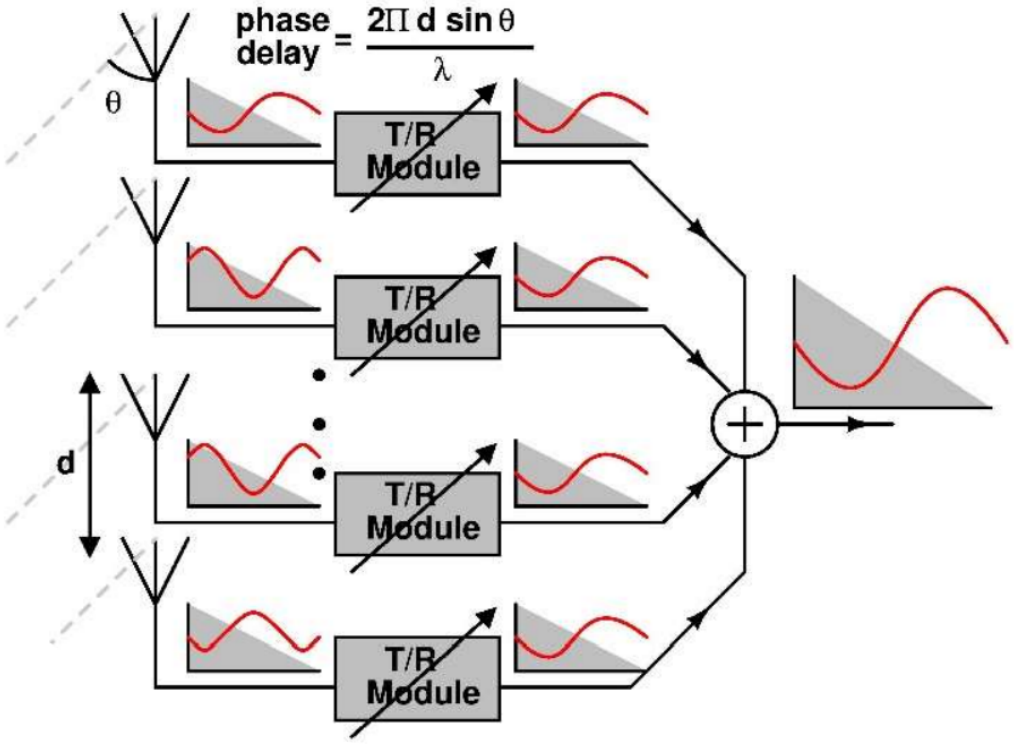


Figure 1.1 A four element active phased array example. (Çalışkan, 2019)

There are active and passive phased array structures based on the feeding mechanisms. Simple structure of a passive phased array is shown in Fig. 1.2. Only one low-noise amplifier (LNA) and power amplifier (PA) are used, and the phase shifters are located between the antenna and the amplifiers. Using less active (amplification) blocks results in lower power consumption compared to its active counterpart. On the other hand, active phased array shown in Fig. 1.1 has an LNA and PA in each element. This structure is more reliable because a failure in a T/R module can be tolerable, but an LNA or PA failure in passive phased arrays will result in the failure of the whole operation. Also, since PA and LNA are directly connected to the antenna, NF will be lower and the output power will be higher compared to the passive counterparts. This is because the phase shifters will introduce a loss which directly adds to the NF and decreases the output power. Superior performance of active phased arrays over passive makes them the general choice for communication systems (Çalışkan, 2019).

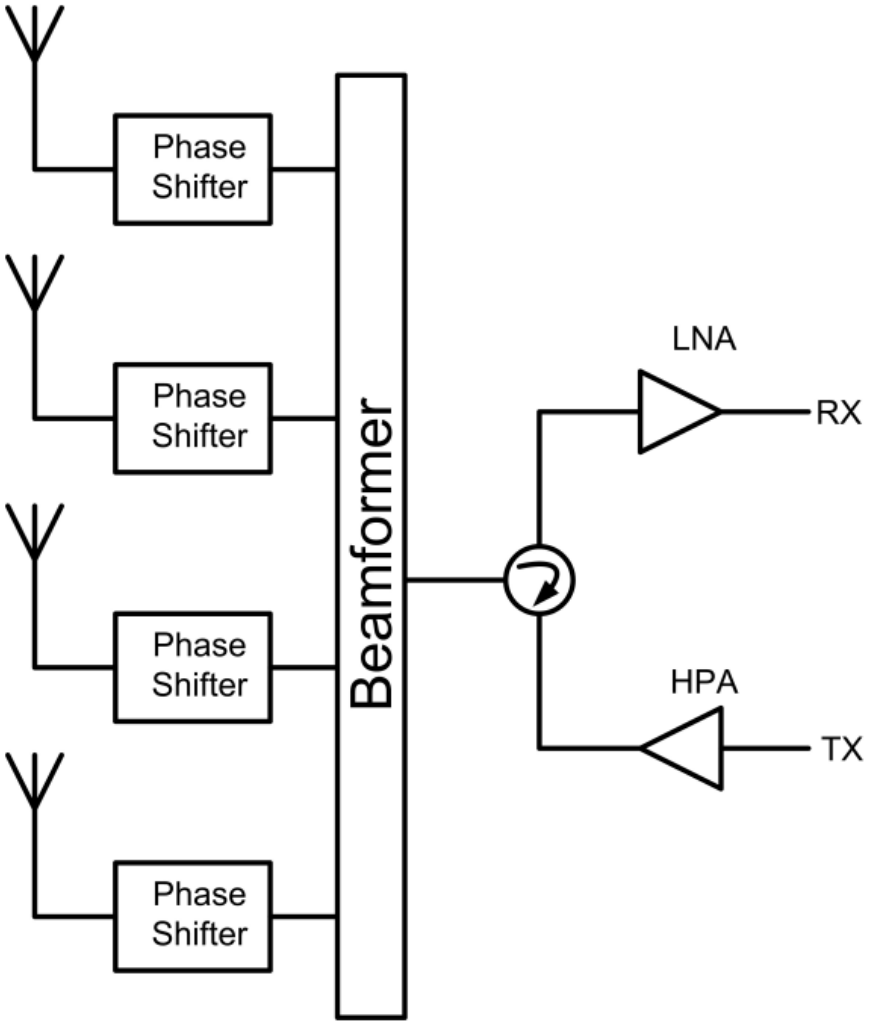


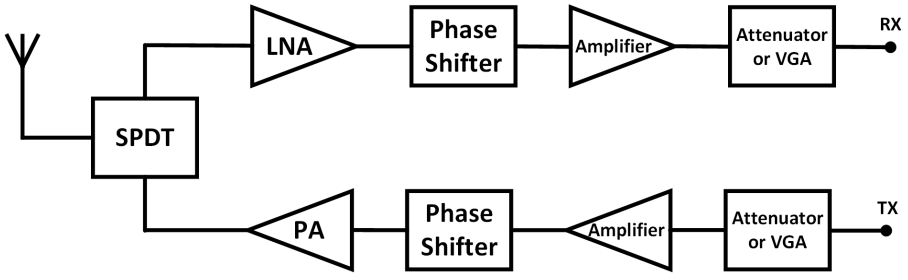
Figure 1.2 Passive phased array structure. (Burak, 2017)

Phase control is also possible in the intermediate frequency (IF) to avoid design challenges and high loss in RF frequencies. But this will result in an increased area due to larger passive components in IF. Digital phase shifting is also another alternative with a cost of very high power consumption of analog-to-digital converters (ADCs). All RF approach presents RF phase shifting with high performance and enables integration in a small area with low cost. The performance of the all RF approach strongly depends on the transceiver module performance (Burak, 2017).

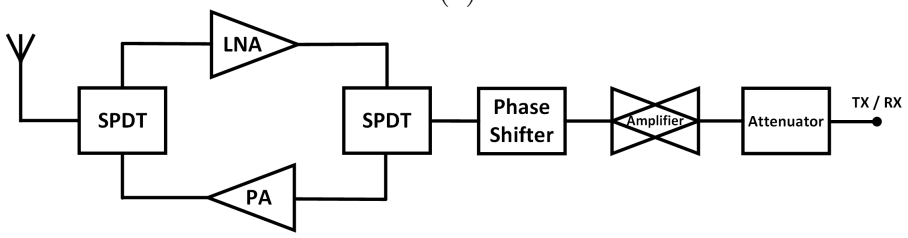
1.2 Transceiver Modules

There are different architectures and building blocks for transceiver modules. Mostly an LNA, a PA and a single-pole double-throw (SPDT) switch are used as a front-end. For beamforming, phase shifter or time delay elements are used for controlling the phase and delay, attenuator or variable gain amplifier (VGA) are used for adjusting the amplitude. Amplifiers are also used for compensating the insertion loss of the passive blocks.

Fig. 1.3 shows two different half-duplex transceiver architectures. The SPDT switch after the antenna selects the mode as transmitter or receiver. Since these architectures cannot transmit and receive at the same time, they are half-duplex. In Fig.1.3(a), separated architecture is shown. There are different paths for the receiver and the transmitter. The SPDT switch isolates these paths. Since receiver(RX) and transmitter(TX) paths are unidirectional, active phase shifters and VGAs can be used for additional gain with increased power consumption. Fig.1.3(b) offers a more compact solution by using a bidirectional path for the common blocks such as phase shifters and attenuators. In this case, phase shifters (or time delay blocks) and attenuators should be passive which enables bidirectional operation. To compensate the insertion loss, bidirectional amplifier can be implemented. This architecture promises superior performance such as lower power consumption and smaller area by the use of bidirectionality. However, the RF performance requirements of the sub-blocks makes the design challenging (Bentini et al., 2014).



(a)



(b)

Figure 1.3 Transceiver architectures (a) separated (b) bidirectional.

1.3 SiGe BiCMOS Technology

CMOS is the most widely used technology in the electronics industry. Aggressive scaling has increased the speed of the CMOS transistors like Moore's Law predicts (Moore, 2006). The success of CMOS is aimed to be also used for RF transceiver applications. However, with the shrinkage of the devices, the low breakdown voltages limit the output power of the transistors. Also, low transconductance leads to limited frequency response and low performance in RF frequencies. The silicon-on-insulator (SOI) CMOS technology offers very high transit frequency (f_t) (England et al., 2013). Low minimum noise figure (NF_{min}) and inductors with high quality factor makes SOI promising for RF transceiver applications. But still, the output power capability, linearity and efficiency of this technology is quite low.

III-V group technologies such as Gallium Arsenide (GaAs) and Gallium Nitrate (GaN) achieve the best performance metrics like low NF, high linearity and efficiency, and superior frequency response compared to silicon based technologies. This makes them a good candidate for RF transceiver applications but the low yield and large area increases the cost and limits the number of elements in a phased array. Also, integration of bulk CMOS containing analog and digital circuits, and III-V technologies on a single chip is not possible. Integration with silicon is one of the most important parameters since the leading technology in the industry is CMOS based.

SiGe Bipolar CMOS (BiCMOS) technology enables the integration of CMOS and bipolar devices on the same die. The heterojunction bipolar transistors (HBTs) show superior RF performance than CMOS such as high transconductance, output power and efficiency. The output power and noise figure performances are still modest compared to its III-V counterparts, but the integration capabilities of SiGe BiCMOS offers lower area, lower cost and high performance system-on-chip solutions for RF phased array applications (Cressler & Niu, 2002). IHP's 0.13 μm SiGe BiCMOS technology offers an high f_t of 240 GHz and maximum oscillation frequency (f_{max}) of 340 GHz. The current gain is around 900 and the collector-emitter breakdown voltage is 1.65 V which can be increased to 1.8 V with a cascode structure.

1.4 Motivation and Organisation

Earth observation, satellite and space communication, air-land-sea RADARs, mapping of infrastructure and natural resources, and even medical applications utilize phased arrays (Arnieri et al., 2019). Growing need for phased arrays require high performance transceiver modules. High bandwidth, output power, precision and low noise figure are needed to achieve the requirements for these systems. Above all, low area and low cost are the main requirements for the transceiver modules to be used in a commercial service.

For a unidirectional transceiver architecture, VGA can be preferred over an attenuator due to its gain and low area. However, VGAs have lower amplitude control ranges than an attenuator and the phase difference is too high. If the phase difference is lowered in an moderate amplitude control range, VGAs will be superior than an attenuator. In Chapter 2, a new design technique will be explained that decreases the amplitude error in VGAs which allows them to have higher amplitude control range. This technique also achieves low phase difference and low area.

Bidirectional transceiver architectures could achieve superior performance and low area compared to unidirectional ones. Some wideband transceivers in the literature are given in Table 1.1. Bentini et al. (2014) and Jeong, Yom, Kim, Lee & Lee (2018) demonstrated high performance in output power, phase and amplitude control and NF using GaAs technology. The chip area for these works are more than 20 mm^2 and the cost is high. Sim, Kang, Kim, Chun, Jang & Jeon (2015) and Sim, Jeon & Kim (2013) showed good performance in CMOS but in a narrowband operation range. Cho, Han, Kim & Kim (2014) achieved high bandwidth in CMOS but the gain is low and NF and output power information is not available. Lastly, Cho, Song & Cressler (2018) implemented only a common-chain in SiGe technology that has modest performance but NF and output power results are not available. To achieve good performance in high bandwidth with a low cost and integration capabilities, SiGe BiCMOS technology is preferred. Proposed transceiver module covers X, Ku and K bands with a bandwidth from 8 to 28 GHz. The proposed architecture uses true time delay (TTD) because phase shifting can limit the bandwidth due to beam squinting (Garakoui et al., 2011). The specifications of the proposed module is also given in Table 1.1. Details of the design and sub-block performance specifications, and the design methodology of each sub-block in the proposed transceiver will be given in Chapter 3.

Finally, Chapter 4 will conclude the thesis and comment on future studies.

Table 1.1 Bidirectional Wideband Transceiver Modules in Different Technologies

Reference	(Bentini et al., 2014)	(Jeong et al., 2018)*	(Sim et al., 2015)	(Sim et al., 2013)	(Cho et al., 2014)*	(Cho et al., 2018)*	**Proposed***
Technology	0.18µm GaAs	0.25µm GaAs	0.13µm CMOS	0.13µm CMOS	0.13µm CMOS	0.13µm SiGe	**0.13µm SiGe**
Frequency	6-18 GHz	6-18 GHz	9-10 GHz	8.5-10.5 GHz	8-16 GHz	2-20 GHz	**8-28 GHz**
RX/TX Gain	21/18 dB	11/11 dB	12/9 dB	3.5/3.5 dB	-1/-1 dB	-3.6/-3.6 dB	**20/20 dB**
Amp. Res.	5 bit	7 bit	5 bit	5 bit	6 bit	6 bit	**5 bit**
Phase Res.	4 bit	8 bit	6 bit	6 bit	7 bit	7 bit	**6 bit**
Amp. Error	0.8 dB	1 dB	0.4 dB	0.3 dB	-	1.6 dB	**0.5 dB**
Phase Error	13°	1.7 ps	2.3°	4.3°	1.6 ps	10 ps	**1.9 ps**
Noise Figure	8 dB	18 dB	-	7.5 dB	-	-	**5 dB**
OP_{1dB}	17 dBm	16.5 dBm	11 dBm	6.5 dBm	-	-	**15 dBm**
P_{DC}	1.25 W	1.6 W	800 mW	150 mW	280 mW	285 mW	**<350 mW**
Area	25.8 mm^2	20 mm^2	11 mm^2	1.2 mm^2	3.9 mm^2	5.5	**<5 mm^2**

*Time delay is used instead of phase shifting.

2. VARIABLE GAIN AMPLIFIER WITH A NOVEL AMPLITUDE AND PHASE ERROR REDUCTION TECHNIQUE

Today's telecommunications, military and commercial radars, weather monitoring systems, and air traffic controls utilize phased-array transceiver modules. Phased arrays need accurate amplitude and phase control as the bandwidth range increases. Increasing the performance of phased arrays and beamforming systems depends on low sidelobe levels to reduce tracking errors and steer the main beam. Low amplitude and phase errors in a wide range of frequencies must be maintained to achieve these low sidelobes. Root mean square (rms) phase errors of less than 3.2° are needed to achieve ultralow sidelobe levels (Kang, Kim, Min & Rebeiz, 2009; Padovan, Tiebout, Neviani & Bevilacqua, 2016; Roques, Cazaux & Pouysegur, 1990; Tayrani, Teshiba, Sakamoto, Chaudhry, Alidio, Kang, Ahmad, Cisco & Hauhe, 2003).

VGAs or attenuators can be utilized to control the amplitude of a signal. Attenuators have some advantages over VGAs, such as linearity and DC power consumption (P_{DC}). Still, they require a large area and suffer from high insertion loss due to their passive structure (Davulcu, Burak & Gurbuz, 2020). On the other hand, VGAs are active blocks that supply a system with gain while controlling the amplitude. High linearity and a wideband operation can be incorporated into the design to make a VGA even more advantageous than an attenuator. Since phased array receivers also require low noise for high dynamic range, VGAs can be designed as low noise variable gain amplifiers (LNVGAs) and can be utilized as the noise suppression block in a receiver. Thus, a wideband LNVGA with high linearity can be a superior choice for a phased array radar system.

Several VGA topologies such as variable g_m, variable load, feedback control, and current steering have been proposed in the literature (Baumgratz, Saavedra, Steyaert, Tavernier & Bampi, 2019; Min & Rebeiz, 2008). Hybrid topologies combining attenuators and VGAs have also been published (Xu, Yi, You & Zhao, 2019). The current steering topology offers superior performance among VGA topologies. For example, matching the input impedance in all gain settings is easier in the current steering topology since the transconductance of the input transistor does not change

(Min & Rebeiz, 2008).

8-18 GHz covers all the X and Ku-Bands used for military radar applications and air traffic control (Qorvo, 2022). Covering both bands with one circuit and using a VGA instead of an attenuator reduces the area, hence the system's cost. As mentioned above, design constraints such as wideband operation, high linearity, and low noise make the design challenging. Maintaining low phase and amplitude errors are also crucial for the performance of a phased array radar system.

In the following sections, the current steering topology and its shortcomings in amplitude and phase responses will be analyzed. A detailed explanation of improving the amplitude and phase responses with a novel method will be given. The proposed technique is utilized in a wideband LNVGA, operating between 8 and 18 GHz, with a gain control range (GCR) up to 30 dB. The circuit is designed and implemented in IHP's 0.13 µm SiGe BiCMOS technology.

2.1 Conventional Current Steering Topology

Current steering topology is widely used in the literature with phase error reduction techniques (Kim, Jang, Kim & Park, 2020; Padovan et al., 2016; Siao, Kao & Wang, 2014; Tsai & Lin, 2019). Ideally, the conventional current steering topology has a very low phase error. But, the need for phase error reduction techniques suggests that this topology has high phase error. In this section, the conventional design will be analyzed, and the reason for the phase error increase will be highlighted. After that, a novel method to compensate for this increase will be proposed without any extra cascaded stages with major changes to the conventional topology.

Fig. 2.1 shows a simple schematic representation of a current steering topology without bias or matching networks. As Q3 steers the current from Q2, the transconductance of Q2 changes, resulting in a different signal level at the output. The small-signal model can be used to derive the current gain to understand the effect on phase response. For easier calculations, Q1 is only taken as a current source since the parameters of Q1 are not changing with respect to the control voltage. The small-signal model for conventional current steering topology is shown in Fig. 2.2. Ignoring the inductors, writing node equations, and rearranging will give the current gain, $\mathrm{I}_{out}/\mathrm{I}_{in}$. From the transfer function, the phase response is calculated as in (2.1). This equation shows minimal phase error because as g_{m2} decreases, g_{m3}

will increase at the same rate, making the sum g_{m2}+g_{m3} constant. Also, as the current in Q2 decreases, $C_{\pi 2}$ will decrease, and as the current in Q3 increases, $C_{\pi 3}$ will increase, making the sum $C_{\pi 2}$+$C_{\pi 3}$ constant.

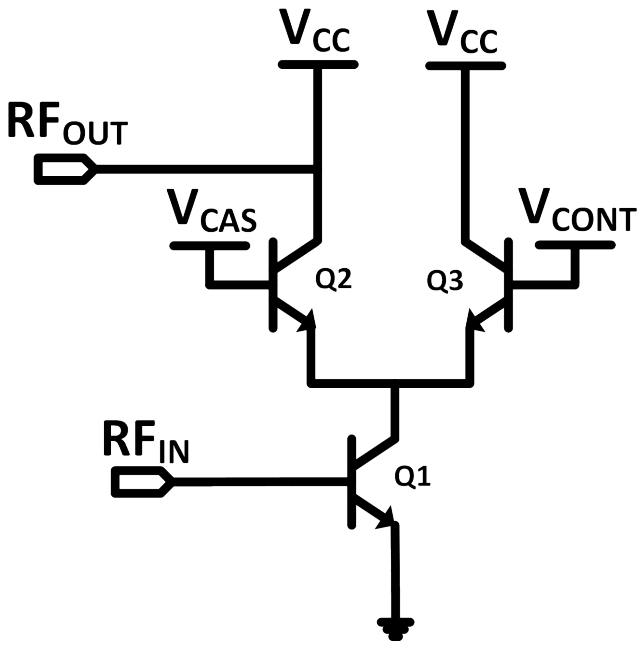


Figure 2.1 Conventional current steering topology.

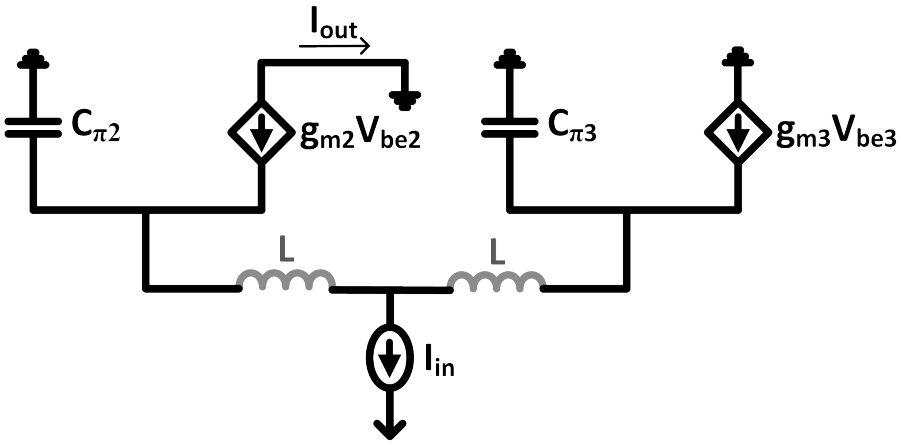


Figure 2.2 Small signal model of conventional current steering topology.

$$\angle\beta_{conv} = \tan^{-1}\left(\frac{g_{m2}+g_{m3}}{w(C_{\pi 2}+C_{\pi 3})}\right) - 90^{\circ} \tag{2.1}$$

Observations showed that this ideal phase behavior is not holding after the layout is drawn. One major parasitic effect caused by the core layout is the connections between the transistors. With their connections, the parasitic inductance will be

introduced at the emitters of Q2 and Q3. These inductance values are as low as 10 to 20 pH but result in high phase errors. Fig. 2.3 shows the core layout of the proposed design. Here, parasitic inductor formation can be observed. Parasitic inductors at the emitters of Q2 and Q3 are added to the small-signal model to understand their effects on the phase response further. Writing node equations at the emitters and between the inductors will be enough to derive the current gain β, which is given in (2.2). Subscript "conv" shows that this is for the conventional topology. Resulting insertion phase from this transfer function is given in (2.3). This equation shows a major contribution of phase difference with the inclusion of the parasitic inductor L. This contribution is the second term where there is a term that only depends on g_{m3}. As g_{m3} increases with the control voltage, this phase term will change drastically, creating a phase difference. Also, it is seen that this contribution is getting more severe as the value of L increases. Amplitude for conventional method are given in (2.4). Ideally, the amplitude should only be controlled by g_{m2}, but many more terms are involved, resulting in a frequency and parasitic inductance dependent response. These analyses reveal why phase difference and amplitude error increase rapidly after layout.

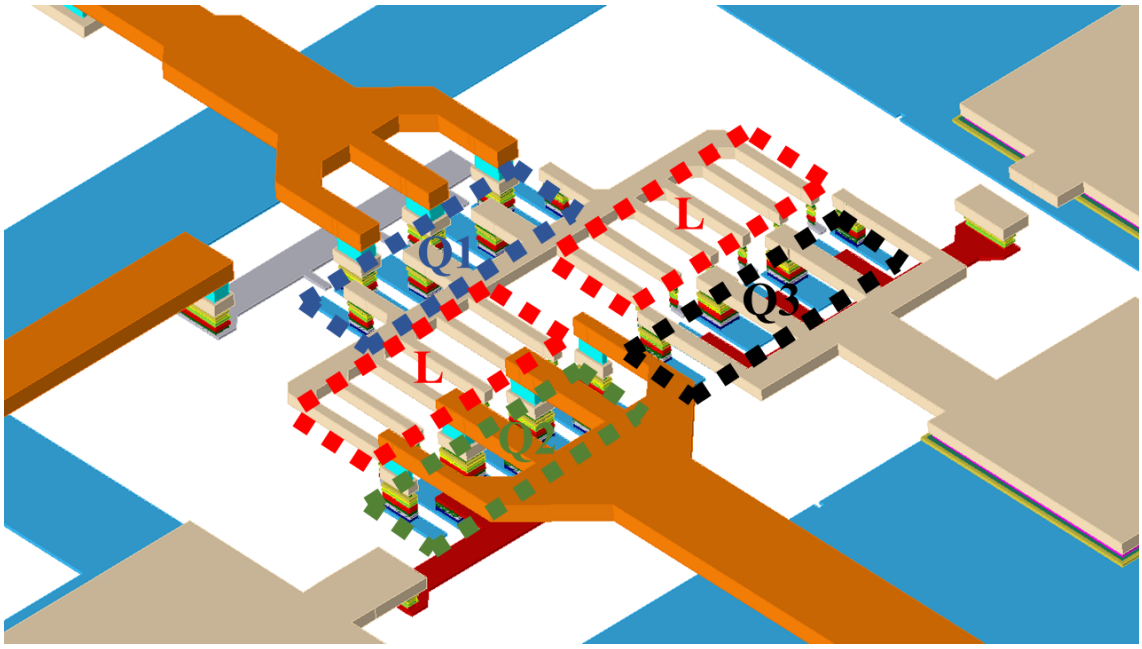


Figure 2.3 Core layout of the proposed design.

$$(2.2) \qquad (I_{out}/I_{in})_{conv} = \beta_{conv} = \frac{-w^2L^2g_{m2}g_{m3} + jwLg_{m2}}{w^2L(C_{\pi2} + C_{\pi3} - Lg_{m2}g_{m3}) - jwL(g_{m2} + g_{m3}))}$$

$$\angle\beta_{conv} = \tan^{-1}\left(\frac{g_{m2}+g_{m3}}{w(C_{\pi 2}+C_{\pi 3}-Lg_{m2}g_{m3})}\right) - \tan^{-1}\left(\frac{1}{wLg_{m3}}\right) \tag{2.3}$$

$$|\beta_{conv}| = \sqrt{\frac{g_{m2}^2(1+w^2L^2g_{m3}^2)}{w^2(C_{\pi 2}+C_{\pi 3}-Lg_{m2}g_{m3})^2+(g_{m2}+g_{m3})^2}} \tag{2.4}$$

2.2 Proposed Method to Reduce Phase and Amplitude Error

A novel approach is proposed to decrease the phase difference due to the parasitic inductance. Fig. 2.4 shows the schematic of the proposed topology. Instead of bypassing the base of Q3, it is open-circuited by a 1 kΩ resistor. This way, a constant insertion phase can be achieved between different gain settings with the parasitic inductance at the emitters of Q2 and Q3. Analysis using the small-signal model will give more insight into this methodology. Fig. 2.5 shows the open-circuited base and the inclusion of the capacitor $C_{\mu 3}$ since both sides are no longer grounded. Equations (2.5),(2.6),(2.7) are written at nodes V_{e2}, V_x and V_{e3}. The series combination of $C_{\pi 3}$ and $C_{\mu 3}$ are taken as $C_{\mu 3}$ since $C_{\mu 3}$ is an order of magnitude smaller than $C_{\pi 3}$. Using these equations and knowing the fact that $g_{m2}V_{be2} = -I_{out}$, current gain β_{new} is derived as in (2.8). The constant α is equal to the voltage division between the capacitors $C_{\mu 3}$ and $C_{\pi 3}$ which is $\frac{C_{\mu 3}}{C_{\pi 3}+C_{\mu 3}}$, and it is much smaller than 1. The subscript "prop" indicates the current gain of the proposed method.

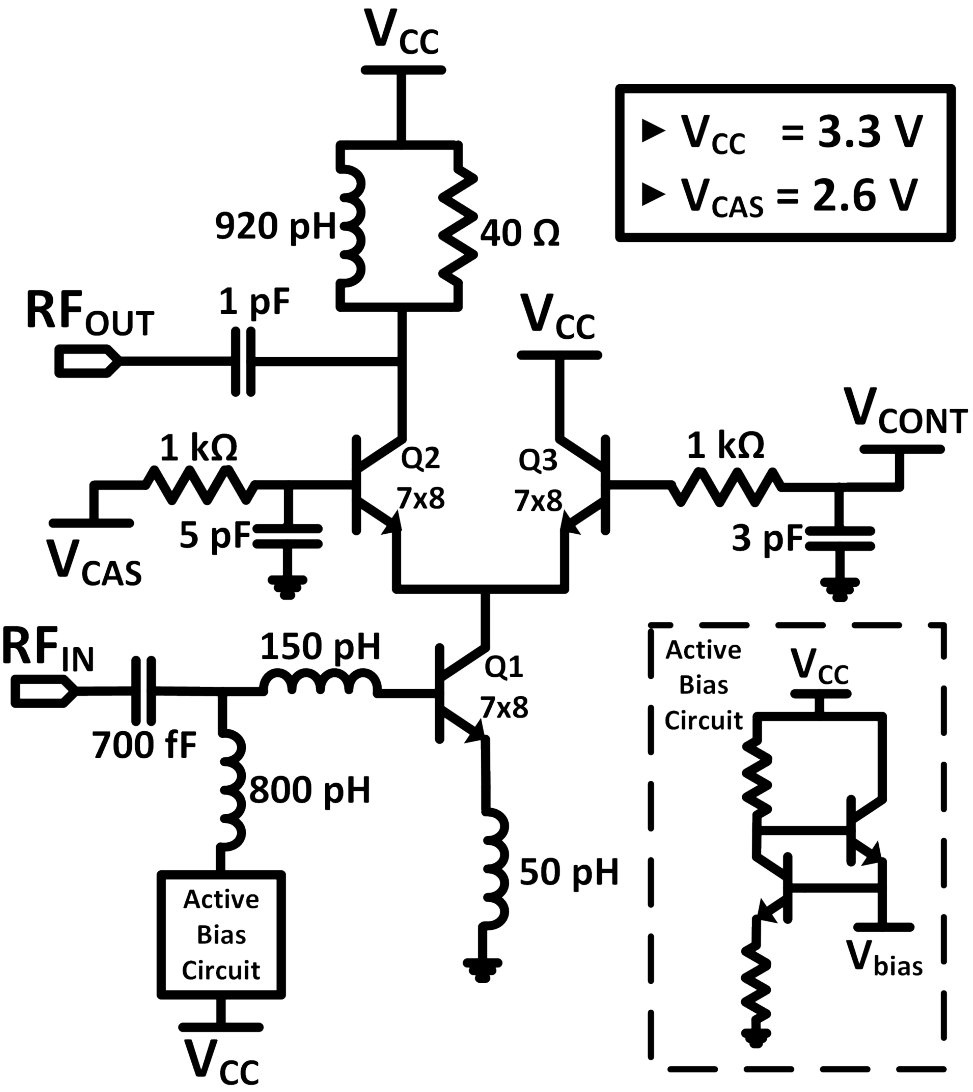


Figure 2.4 Schematic of the proposed LNVGA.

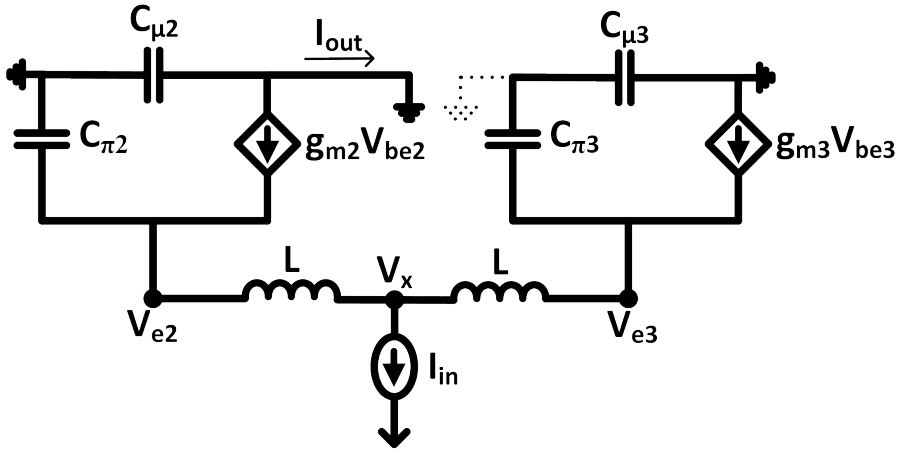


Figure 2.5 Small signal model of the proposed topology.

$$\frac{V_{e2}-V_x}{Z_L}+\frac{V_{e3}-V_x}{Z_L}=I_{in} \tag{2.5}$$

$$\frac{V_{e3}-V_x}{Z_L}+\frac{V_{e3}}{Z_{C_{\mu 3}}}=g_{m3}(-V_{e3}\frac{C_{\mu 3}}{C_{\pi 3}+C_{\mu 3}}) \tag{2.6}$$

$$\frac{V_{e2}-V_x}{Z_L}+\frac{V_{e2}}{Z_{C_{\pi 2}}}=g_{m3}(-V_{e2}) \tag{2.7}$$

$$(I_{out}/I_{in})_{prop}=\beta_{prop}=\frac{-w^2L^2g_{m2}g_{m3}\alpha+jwLg_{m2}}{w^2L(C_{\pi 2}+C_{\mu 3}-Lg_{m2}g_{m3}\alpha)-jwL(g_{m2}+g_{m3}\alpha))} \tag{2.8}$$

2.2.1 Reduction in Phase Error

Equation (2.9) shows the insertion phase of the proposed method. Here, α is multiplied with g_{m3}, and knowing that α is much smaller than 1, it decreases the contribution of g_{m3} to the insertion phase, as seen in the second term in (2.9). For the first term in (2.9), at lower gain settings, $g_{m3}\alpha$ is much smaller than g_{m2}; and $C_{\mu 3}$ is constant with respect to the control voltage. So, the dominating factor is g_{m2} at the numerator and $C_{\pi 2}$ at the denominator. This results in a low phase difference because as g_{m2} decreases, $C_{\pi 2}$ will also decrease.

$$\angle\beta_{prop}=\tan^{-1}(\frac{g_{m2}+g_{m3}\alpha}{w(C_{\pi 2}+C_{\mu 3}-Lg_{m2}g_{m3}\alpha)})-\tan^{-1}(\frac{1}{wLg_{m3}\alpha}) \tag{2.9}$$

The phase difference is defined as the gain control state's insertion phase normalized to the reference state. Phase differences for the proposed and conventional designs are given in (2.10) and (2.11), respectively. Subscript "ref" means that the term's value is given in the reference state, whereas the subscript "att" shows the value in an gain control state. Frequency and parasitic inductance are not changing with respect to the control voltage, so they are given without a subscript. Table 2.1 gives the DC

operating points for the terms used in the equations for different control voltages. At V_{CONT} = 2 V, the current of Q3 is almost zero, meaning this is the reference state. The reference state is not selected at a base voltage of 0 V to avoid the breakdown of the collector-base junction. For the last two terms in equation (2.10), α's decrease as g_{m3} increases will also keep the phase difference low. Comparing these two equations will intuitively conclude that the proposed method will have a superior phase response.

$$
\begin{aligned}
(2.10)\quad PD_{prop} &= \angle\beta_{prop,att} - \angle\beta_{prop,ref} \\
&= \tan^{-1}\left(\frac{g_{m2,att} + g_{m3,att}\alpha_{att}}{w(C_{\pi 2,att} + C_{\mu 3,att} - Lg_{m2,att}g_{m3,att}\alpha_{att})}\right) \\
&\quad - \tan^{-1}\left(\frac{g_{m2,ref} + g_{m3,ref}\alpha_{ref}}{w(C_{\pi 2,ref} + C_{\mu 3,ref} - Lg_{m2,ref}g_{m3,ref}\alpha_{ref})}\right) \\
&\quad - \tan^{-1}\left(\frac{1}{wLg_{m3,att}\alpha_{att}}\right) + \tan^{-1}\left(\frac{1}{wLg_{m3,ref}\alpha_{ref}}\right)
\end{aligned}
$$

$$
\begin{aligned}
(2.11)\quad PD_{conv} &= \angle\beta_{conv,att} - \angle\beta_{conv,ref} \\
&= \tan^{-1}\left(\frac{g_{m2,att} + g_{m3,att}}{w(C_{\pi 2,att} + C_{\pi 3,att} - Lg_{m2,att}g_{m3,att})}\right) \\
&\quad - \tan^{-1}\left(\frac{g_{m2,ref} + g_{m3,ref}}{w(C_{\pi 2,ref} + C_{\pi 3,ref} - Lg_{m2,ref}g_{m3,ref})}\right) \\
&\quad - \tan^{-1}\left(\frac{1}{wLg_{m3,att}}\right) + \tan^{-1}\left(\frac{1}{wLg_{m3,ref}}\right)
\end{aligned}
$$

Table 2.1 DC Operating Points for Different Control Voltages

V_{CONT}	2 V	2.5 V	2.6 V	2.62 V	2.65 V
g_{m2} (mS)	237	230	125	90	45
g_{m3} (mS)	1	10	125	160	201
$C_{\pi 2}$ (fF)	190	187	150	136	118
$C_{\pi 3}$ (fF)	75	100	150	162	177
$C_{\mu 3}$ (fF)	10	10.1	10.5	10.9	11
α	0.12	0.09	0.07	0.06	0.06

Further analysis via inserting DC operating points and comparing the phase differences with respect to frequency will provide a more solid comparison, as shown in Fig. 2.6. The proposed method achieves an almost constant phase difference with the parasitic inductance, whereas the phase difference increases dramatically with parasitic inductance in the conventional method. The proposed method has a lower

phase difference after 10 pH, a very small inductance value.

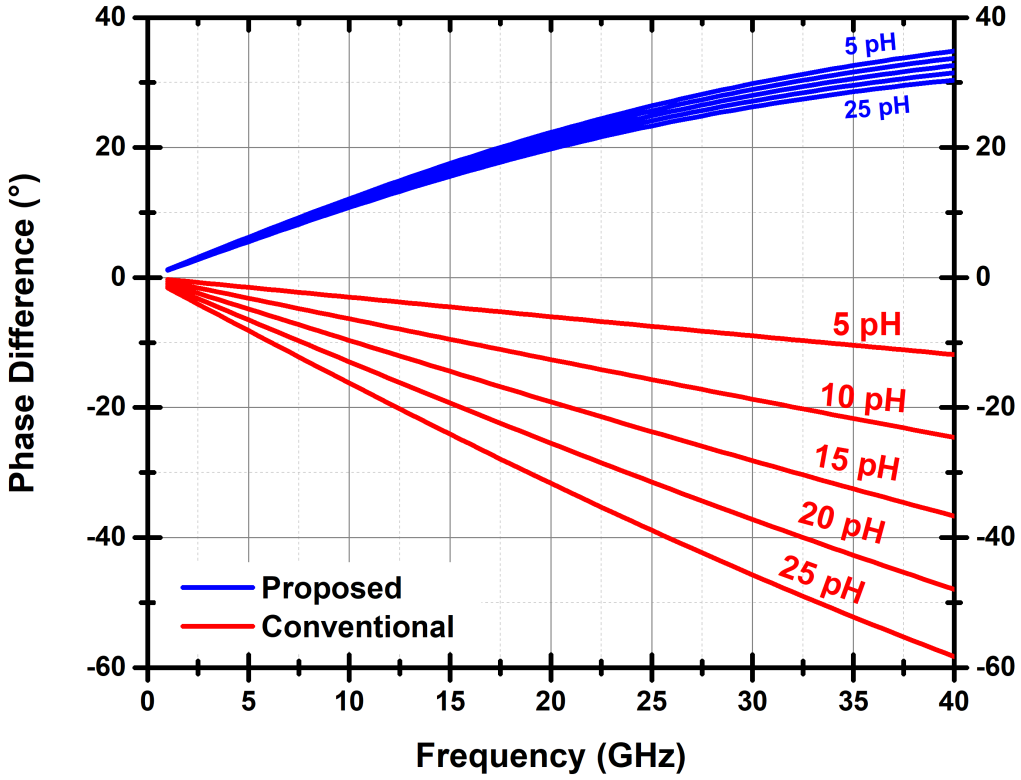


Figure 2.6 Comparison of the phase responses for conventional and proposed designs with respect to parasitic inductance.

2.2.2 Reduction in Amplitude Error

Amplitude response of the current gain in (2.8) can be derived as in (2.12) for the proposed method. Ideally, the amplitude should only be controlled by g_{m2}, but many more terms are involved. The ratio of the amplitude of a state and the reference state should not be changing with respect to frequency to get the same gain in a wideband operating range. The inclusion of α to the proposed method will allow the amplitude to be flat with frequency and constant with the parasitic inductor value.

$$|\beta_{prop}| = \sqrt{\frac{g_{m2}^2(1+w^2L^2g_{m3}^2\alpha^2)}{w^2(C_{\pi2}+C_{\mu3}-Lg_{m2}g_{m3}\alpha)^2+(g_{m2}+g_{m3}\alpha)^2}} \tag{2.12}$$

DC operating points in Table 2.1 are inserted into (2.4) and (2.12) in reference

and low gain state. Fig. 2.7 shows the plot of the amplitude ratio between low gain and reference state, which is a relative state in linear scale. The proposed method achieves a flat gain with respect to frequency, and the variance with parasitic inductance is very low. On the contrary, the conventional method has a very high variance with frequency and parasitic inductance.

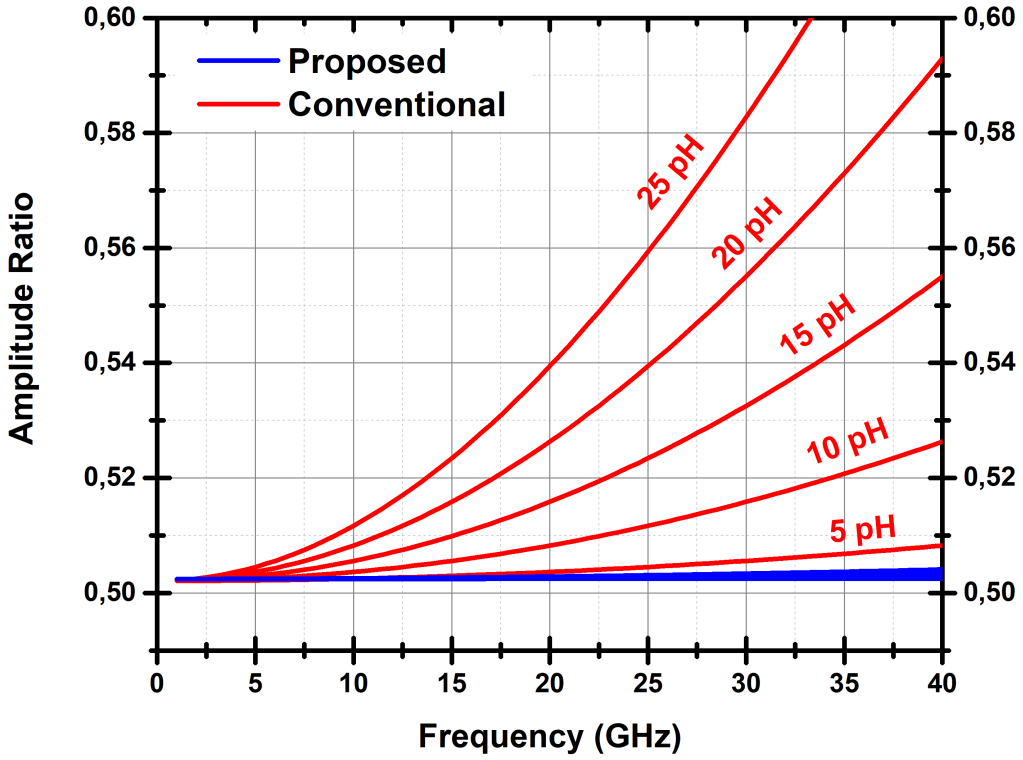


Figure 2.7 Comparison of the amplitude responses for conventional and proposed designs with respect to parasitic inductance.

2.3 Proposed Low Noise Variable Gain Amplifier

Using the proposed method to reduce the phase error, matching networks are added as shown in Fig. 2.4. Even though analog control is used, 0.5 dB step size is aimed with a precision of 1 mV in control voltage. This way, measurements will be done using an ordinary power supply, or one can alternatively use a basic digital-to-analog converter (DAC) to control the gain control states. Q1 and Q2 transistors form the reference cascode, and their sizes are selected for simultaneous noise and power matching. To achieve a symmetric layout and maintain fine gain control steps, the current steering transistor, Q3's size, is also 7x8. The base bias of Q1 is selected as

0.84 V to ensure the minimum noise figure. This bias results in a current of 6.95 mA.

Wideband input and output matchings are required while using minimum matching components. DC block capacitors and RF choke inductors are also used for matching purposes to save area. The quality factor of the output inductor is reduced with a shunt resistor to increase the bandwidth to cover the X-to-Ku band in full. For the input matching, the conventional approach uses a series base inductor and bias with a large resistor to achieve a low noise figure. However, this matching technique is narrowband. (Çaışkan, Kalyoncu, Yazici & Gurbuz, 2019). By switching the resistor with an inductor, wideband matching is obtained at the expense of a small increase in chip area. The sizes of these inductors are optimized for the smallest values while providing proper matching. Also, a small degeneration inductor is used at the emitter of Q1. All component values are given in the schematic. To increase linearity and power handling capability of the LNVGA, V_{CC} is selected as 3.3 V, and the base bias of Q2 is 2.6 V, making V_{CE} of Q2 1.8 V, which is the collector-emitter breakdown voltage of the HBTs. Series 1 kΩ resistors are employed to bias the bases of Q2 and Q3. The total power consumption of the circuit is 23 mW, including the dissipation in the active bias circuit and the 2.6 V bias of Q2.

2.4 Measurement Results and Discussion

The fabricated chip micrograph is shown in Fig. 2.8. The total area is 0.58 mm^2 with pads, and the core area is 0.24 mm^2 without pads. DC probes were used to supply bias voltages. Two ground pads are left open since 5 tip DC probes were used. This did not cause any problems since there were 5 more ground pads left. A total of 7.1 mA is drawn from 3.3 V source, resulting in 23.4 mW power consumption. S-Parameters were measured using RF probes with Keysight N5224A PNA Network Analyzer.

2.4.1 Reference State

Fig. 2.9 shows high consistency between simulation and measurement results. In the simulations, input and output are well matched between 8 and 18 GHz. Measurements revealed that the output matching peak is moved 2 GHz to higher frequencies due to the pad capacitance. Gain is maximum at 10 GHz with 12.4 dB and, 3-dB bandwidth is between 7.5 and 18 GHz. Input return loss is below -8.2 dB from 8 to 18 GHz, and output is well matched from 10 GHz to 18 GHz but drops to -5.5 dB at 8 GHz.

Noise Figure measurements are performed with Keysight 346CK01 noise source and Agilent E4448A Spectrum Analyzer. The measurement result is given in Fig. 2.10, which is very similar to the simulation. NF is minimum at 15 GHz with 1.93 dB and is not exceeding 2.8 dB in the 8-18 GHz band. NF is very low within a high bandwidth.

Agilent E8267D Vector Signal Generator and Agilent E4448A Spectrum Analyzer are used for large-signal measurements. Fig. 2.11(a) shows the result of the gain measurements when a large signal is applied at the center frequency, 13 GHz. Gain compression with respect to input power is given, and the input 1-dB compression point (IP_{1dB}) is 3.75 dBm. Also, two-tone is applied 10 MHz apart from 13 GHz. Then, fundamental and 3^{rd} harmonic power levels are measured, which are given in Fig. 2.11(b). The lines are extrapolated to find the third-order intercept point (IP_3), resulting in an input IP_3 of 1 dBm.

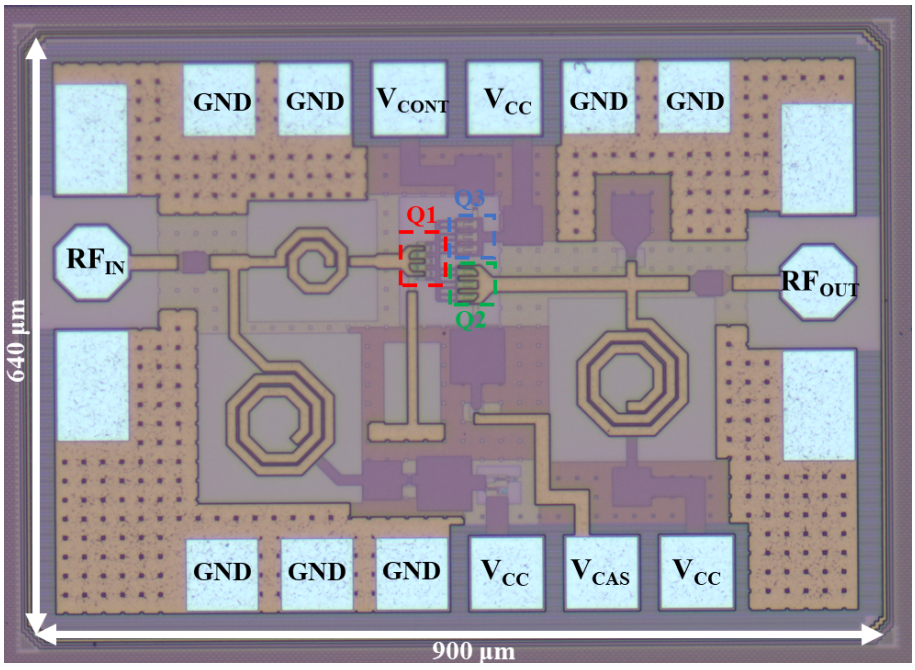


Figure 2.8 Micrograph of the measured die.

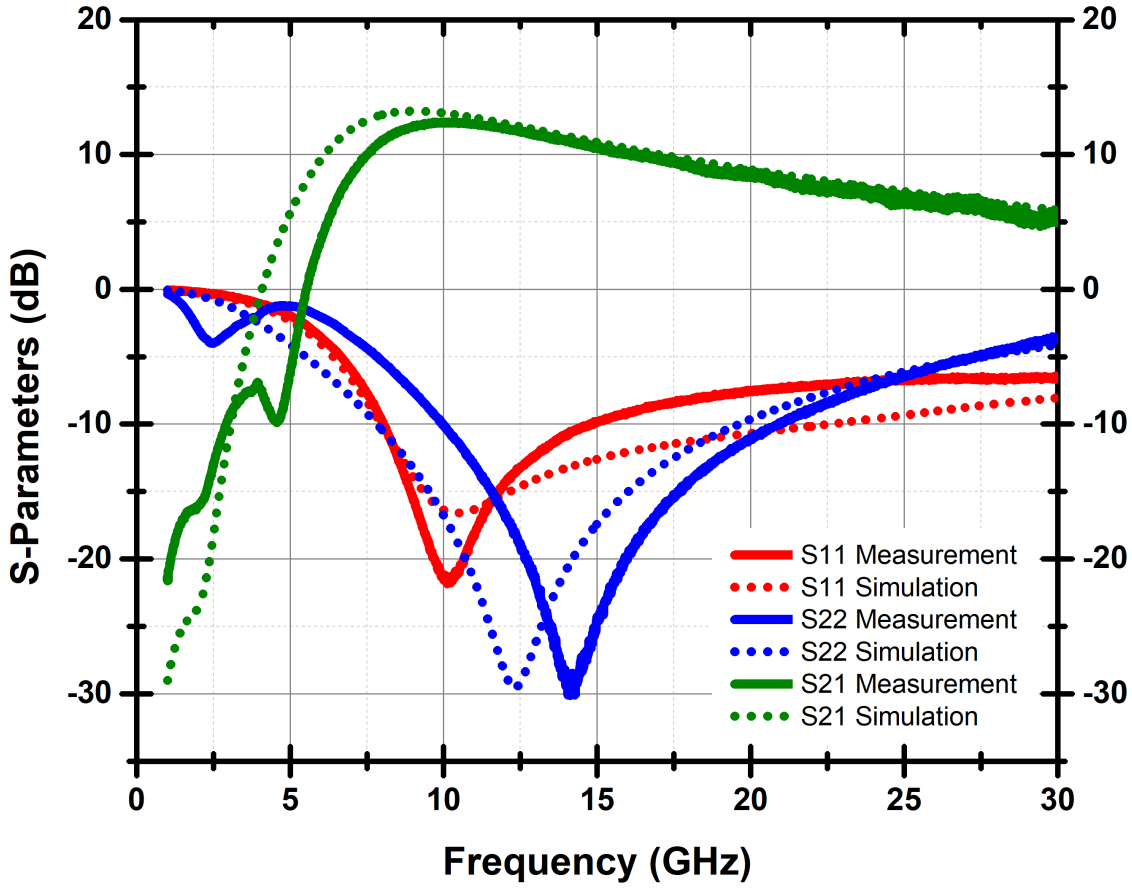


Figure 2.9 Measured S-Parameters vs simulations.

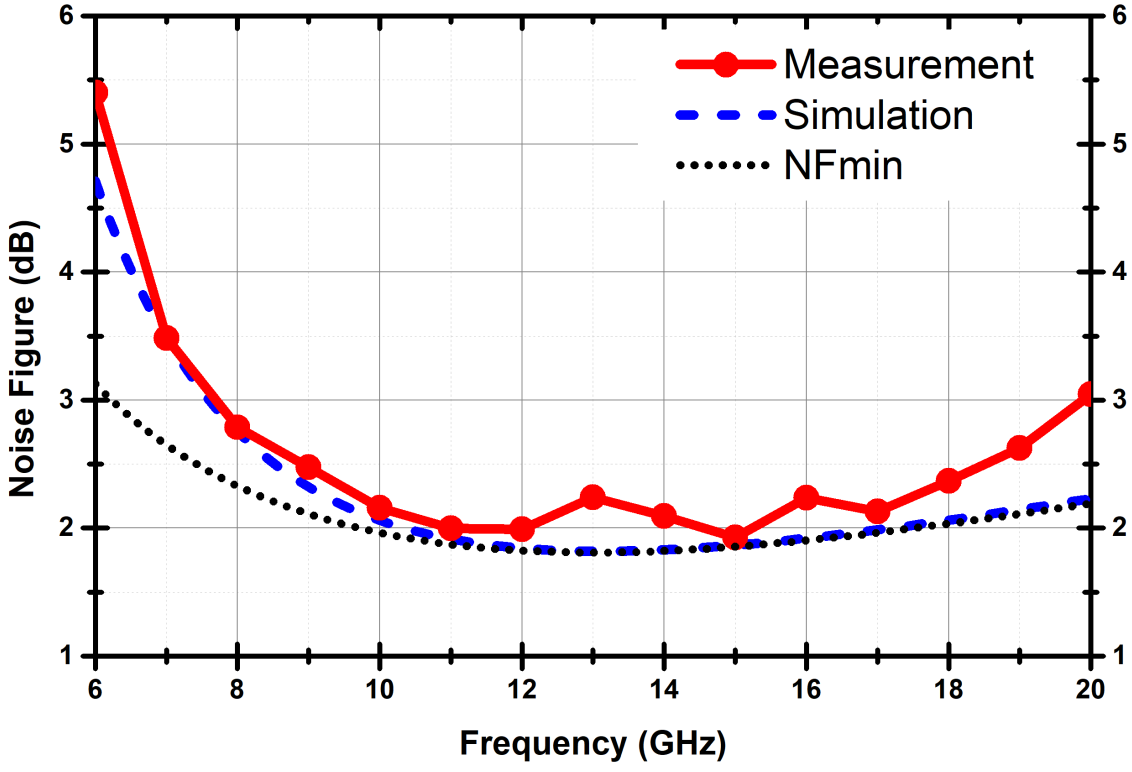
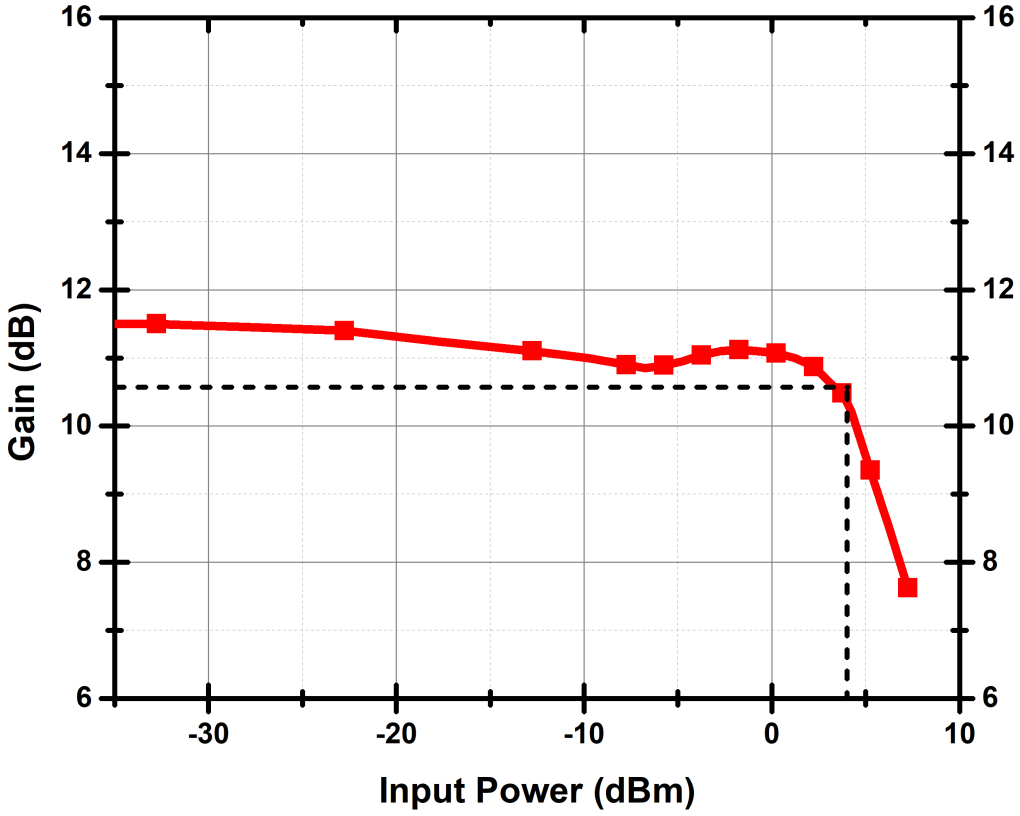
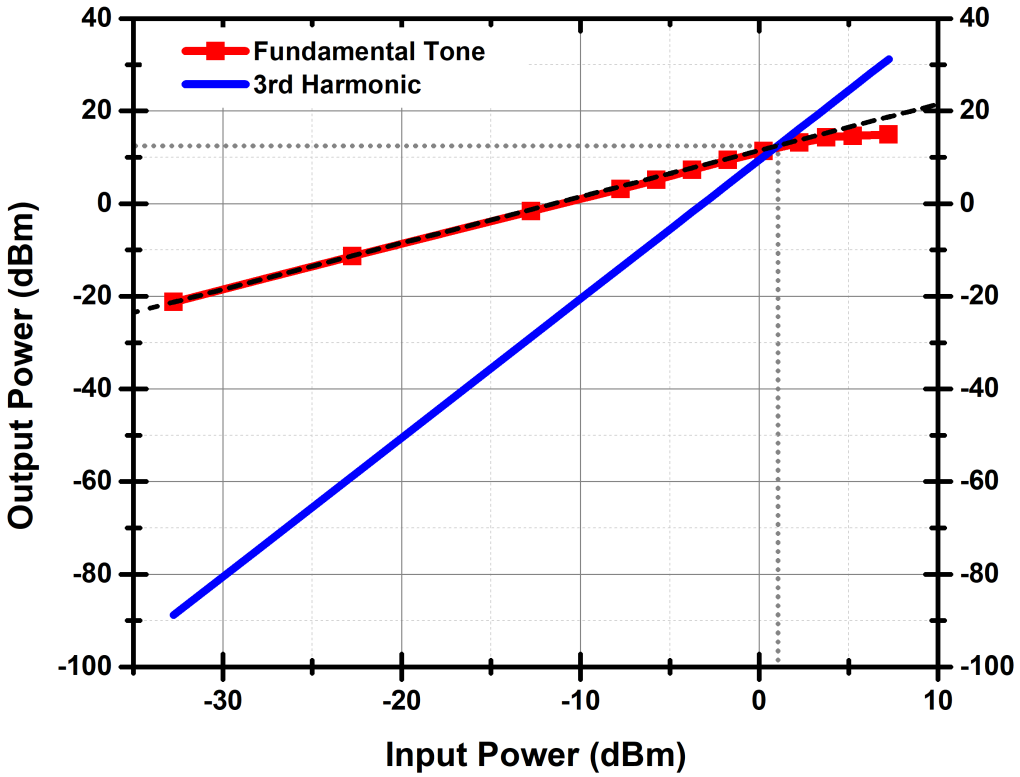


Figure 2.10 Measured Noise Figure vs simulations.



(a)



(b)

Figure 2.11 Large signal measurements.

These measurements are performed from 8 to 20 GHz to understand the large-signal behavior of the proposed design with respect to frequency. Fig. 2.12 shows IP_{1dB} and IIP_3 vs frequency. Also, simulated results are added to ensure that measurements are in line with simulations. IP_{1dB} is highest at 16 GHz with 3.9 dBm, and it is lowest at 8 GHz. Single-stage design with high V_{CC} enables high output swing and achieves excellent power handling capability constant with frequency. A minimum of -1.5 dBm IIP3 is achieved throughout the bandwidth, with a maximum of 1.2 dBm at 14 GHz. Both results show very low variance with frequency, and measured values are similar to the simulations.

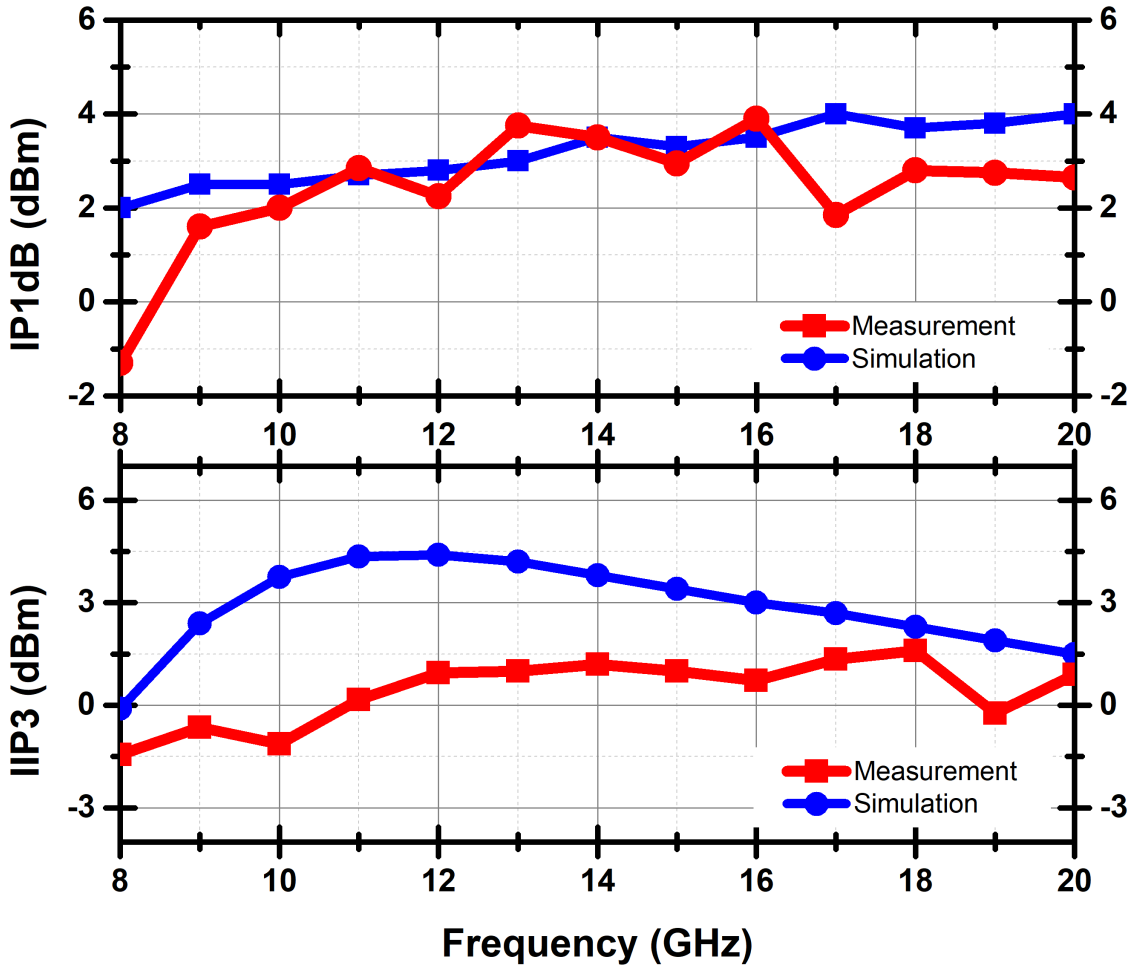


Figure 2.12 IP_{1dB} and IIP_3 vs frequency.

2.4.2 Gain Control States

Output impedance seen from the collector of Q2 is dominated by the g_m and r_0 of Q1. Since the current flowing through Q1 is constant, g_m and r_0 of Q1 are not changing. Also, matching circuits' behavior is stable, resulting in almost the same input and output return losses for all gain control states.

Gain control states are given up to 16 dB in Fig. 2.13. As the gain decreases, constant behavior with frequency is getting harder to meet, increasing the amplitude error. Also, with decreasing gain, phase error will increase as well. This is also because Q1's collector current will not be constant for lower gains. For some value of V_{cont}, the collector current of Q3 will be higher than 7.1 mA, which is the collector current of Q1 in the reference state. After that point, Q2 will still be conducting a small current, but it is not zero. As the control voltage increases further, the current of Q1 will increase. Furthermore, very small currents, below 100 µA, are flowing through Q2, which is hard to keep constant. These will result in an increase in the amplitude and phase error.

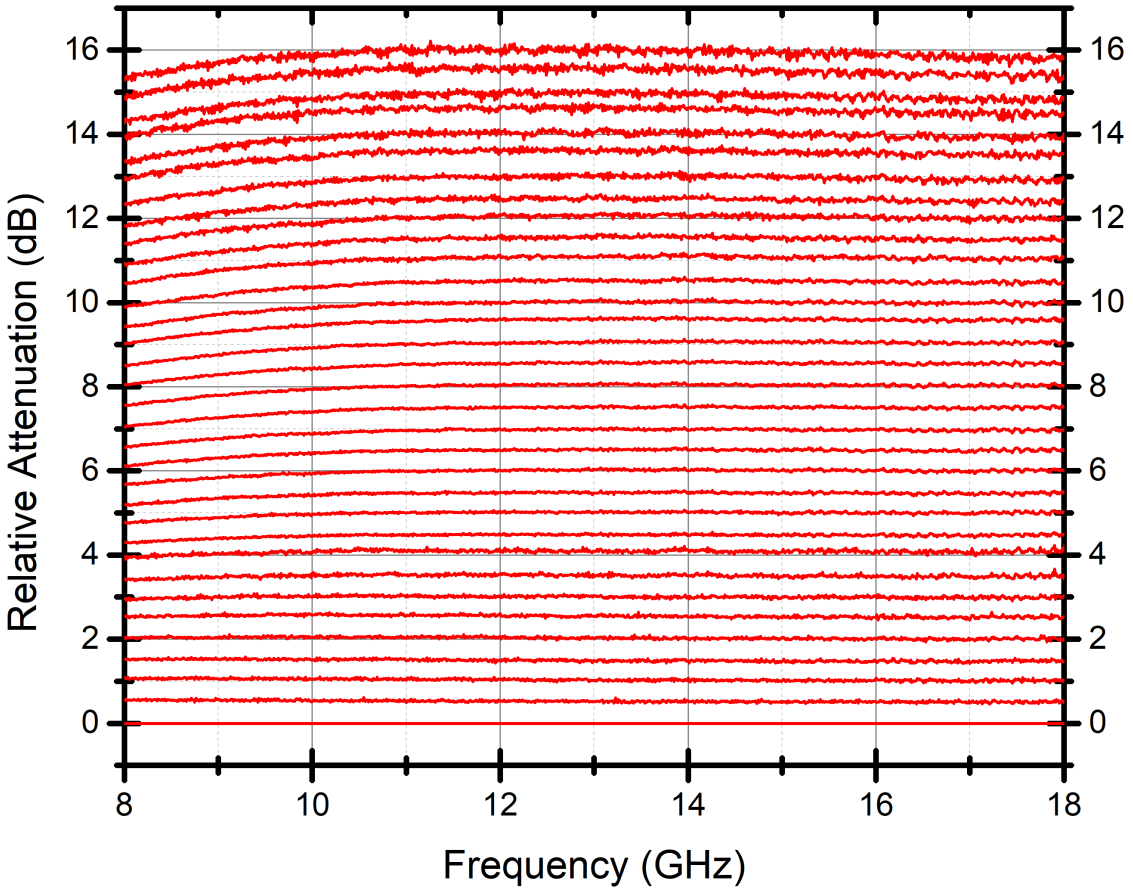


Figure 2.13 Relative gain control states.

Fig. 2.14 shows the measured and simulated rms phase and amplitude errors. The proposed technique achieves excellent phase response, and rms phase error is 0.8° at the center frequency, 13 GHz. Investigating the phase difference with respect to the reference state can also be meaningful since rms phase error is calculated with respect to the mean phase. At 13 GHz, the maximum phase difference between a state and the reference state is 2°. For the whole bandwidth, the maximum rms phase error is 4.3° and the maximum phase difference with respect to the reference state is 12.3°. rms amplitude error is very low with 0.05 dB at 13 GHz and highest at 18 GHz with 0.26 dB.

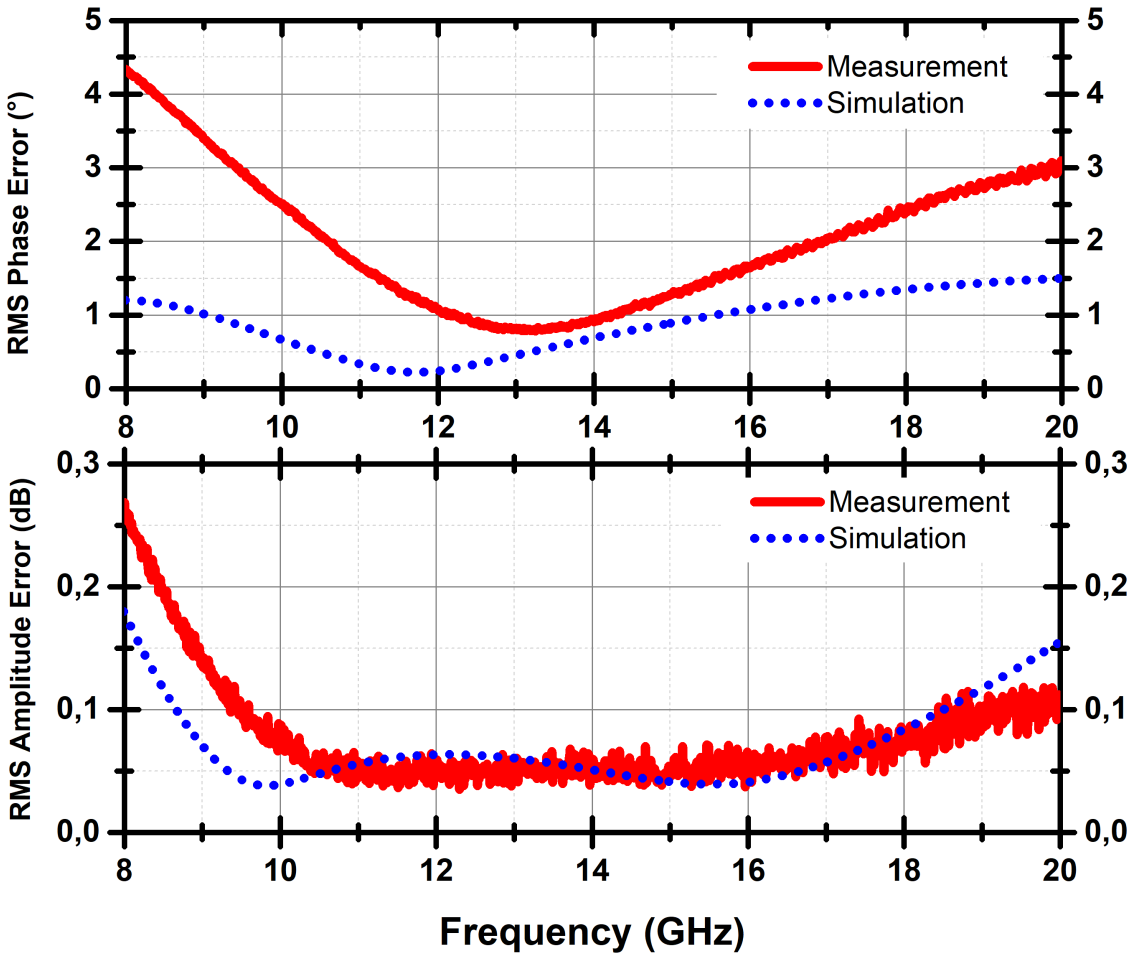


Figure 2.14 rms phase and amplitude errors.

Maintaining low rms phase and amplitude errors throughout a wide bandwidth is challenging, so the proposed design can also be used in a narrow bandwidth between 12 and 14 GHz with excellent performance. Since the circuit exhibits superior performance in the center frequency, this narrowband design will avoid performance degradation. Between 12 and 14 GHz, the maximum rms phase error is only 1°, and the phase change with respect to the reference state is 2.8°. The rms amplitude error is not higher than 0.06 dB in the proposed band, which is remarkably low.

Also, S11 and S22 are below -10 dB, and NF is a maximum of 2.24 dB.

The proposed design can also be configured to have a higher GCR. Nevertheless, as the GCR increases, the rms phase and amplitude errors also increase significantly. As an example, 30 dB GCR is shown in Fig. 2.15. Any GCR up to 30 dB is achievable. After around 30 dB, rms amplitude error begins to exceed 0.5 dB, which could result in poor performance when beamforming. In this case, step size might be increased to 1 dB for better performance in expense from precision. Fig. 2.16 shows the rms phase and amplitude errors. For 8-18 GHz bandwidth, the maximum rms phase error is 12.3°, and the rms amplitude error is 0.49 dB. Overall, this design has a configurable GCR and can be used as a wideband or narrowband depending on the application.

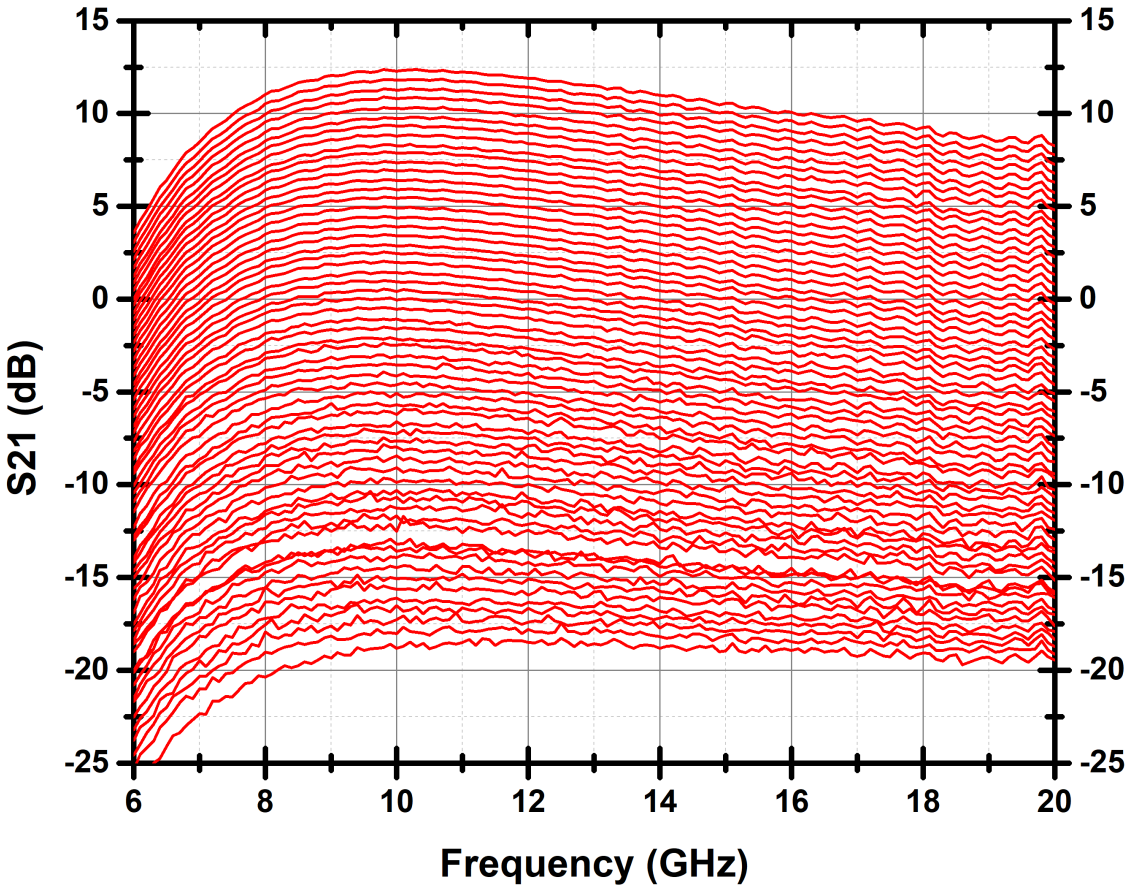


Figure 2.15 All 60 gain states for 30 dB GCR.

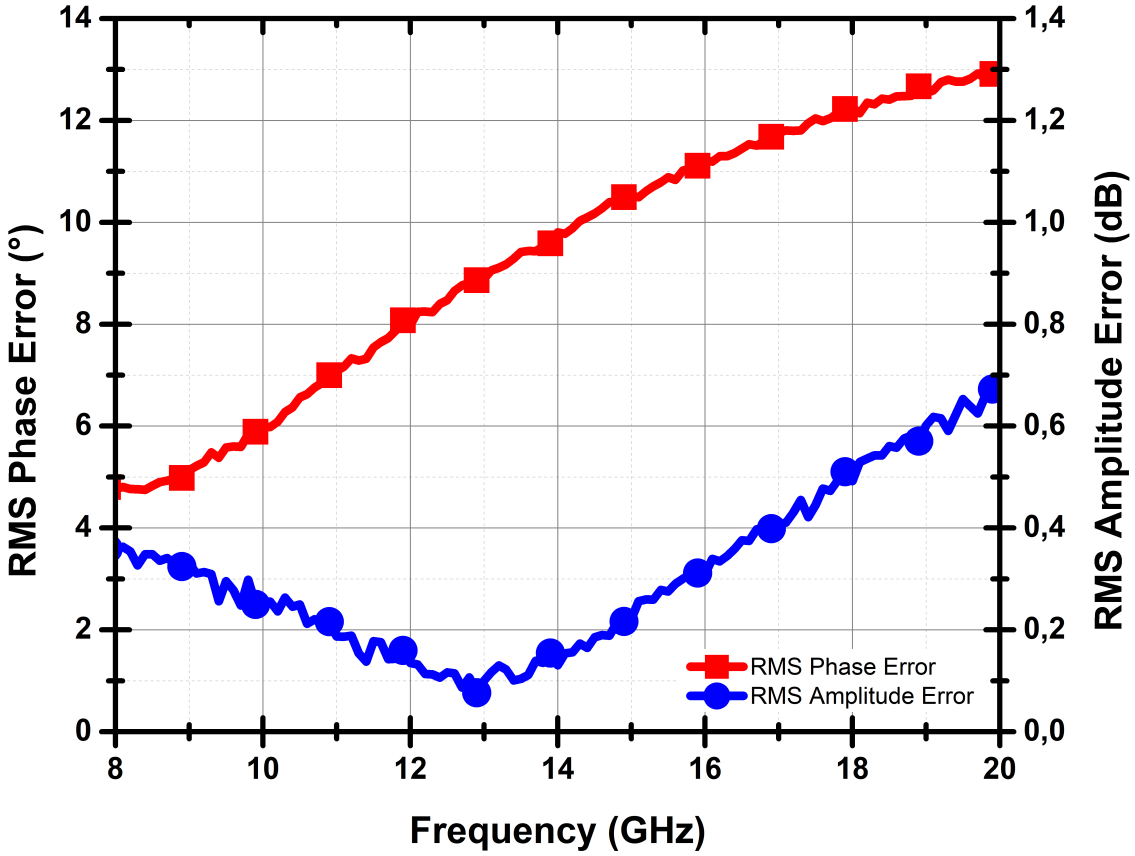


Figure 2.16 rms phase and amplitude errors for 30 dB GCR.

Table 2.2 presents a performance summary of the proposed design for two different frequency ranges and a comparison with the state-of-the-art VGAs. Lowest NF, highest linearity performances and lowest DC power consumption are achieved by our work. The highest fractional bandwidth is also achieved without insertion loss, where (Wang, Li, Wang, Cheng, Li & Zhuang, 2022) is actually an attenuator designed as a VGA. For the narrowband version, superior phase imbalance and very low amplitude error are achieved, and lower phase imbalances in (Padovan et al., 2016) and (Zhang, Zhao, Yu, Wu, Liu, Che, Xue & Kang, 2022) use more than three times DC power. Single-stage topology results in a low chip area. Overall, the proposed novel LNVGA shows excellent performance in all metrics.

Table 2.2 Comparison With the State-of-the-Art VGAs

Reference	(Padovan et al., 2016)	(Wang et al., 2022)	(Suh et al., 2018)	(Gao et al., 2021)	(Zhang et al., 2022)	**This Work**	**This Work**
Technology	SiGe Bipolar	0.18 µm SiGe	65 nm CMOS	65 nm CMOS	65 nm CMOS	**0.13µm SiGe**	**0.13µm SiGe**
Frequency	10-14.4 GHz	6-18 GHz	6-8 GHz	6.5-12 GHz	24-28 GHz	**8-18 GHz**	**12-14 GHz**
Gain	13 dB	-2 dB	11.5 dB	20.2 dB	29.4 dB	**13.2 dB**	**12 dB**
Step Size	-	2 dB	1.8 dB	2.25 dB	0.2 dB	**0.5 dB**	**0.5 dB**
GCR	22 dB	20 dB	9.2 dB	18 dB	6.2 dB	**16 dB**	**16 dB**
rms Amp. Error	-	0.55 dB	0.1 dB	0.6 dB	0.13 dB	**0.26 dB**	**0.06 dB**
rms Phase Error	0.5°	1.3°	4°	4.5°	0.92°	**4.3°**	**1°**
Noise Figure	5.1 dB	-	6.7 dB	3.26 dB	4.8 dB	**1.93 dB**	**1.93 dB**
IP_{1dB}	-17 dBm	-5 dBm	-5.8 dBm	-5 dBm	-22.1 dBm	**3.9 dBm**	**3.9 dBm**
IIP_3	-3 dBm	-	-	-6 dBm	-	**1 dBm**	**1 dBm**
P_{DC}	83 mW	71 mW	72.5 mW	75 mW	103 mW	**24 mW**	**24 mW**
Area	0.7 mm^2	0.98 mm^2	1.16 mm^2	0.98 mm^2	0.14* mm^2	**0.58 mm^2**	**0.58 mm^2**

*Area without pads

3. BIDIRECTIONAL TRANSCEIVER MODULE FOR 8-28 GHZ PHASED ARRAY APPLICATIONS

The proposed bidirectional transceiver aims to work continuously for different frequency bands (X-to-K) simultaneously. 8-28 GHz is selected as the operating frequency, and the system and its sub-blocks should achieve good RF performance at a very high bandwidth. For beamforming, instead of phase shifting, time delay is preferred. Generally, phase shifters are utilized in phased-array applications due to time delay circuits having large area and insertion loss. However, as the bandwidth increase, a phenomenon called "beam-squint" affects the beamforming performance of the system severely. This is because since the phase is dependent on frequency, the beam will have a reduced gain in different frequencies, hence limited bandwidth. This phenomenon is illustrated in Fig. 3.1. The main beam is pointing in the direction of θ_0. However, the beam at frequency $f_0 + \Delta f$ is pointing at $\theta_0 + \Delta\theta$, instead of θ_0. Effectively, for frequency $f_0 + \Delta f$, the gain is reduced. As the bandwidth increases, the gain reduction will be more severe, which limits the operating frequency range.

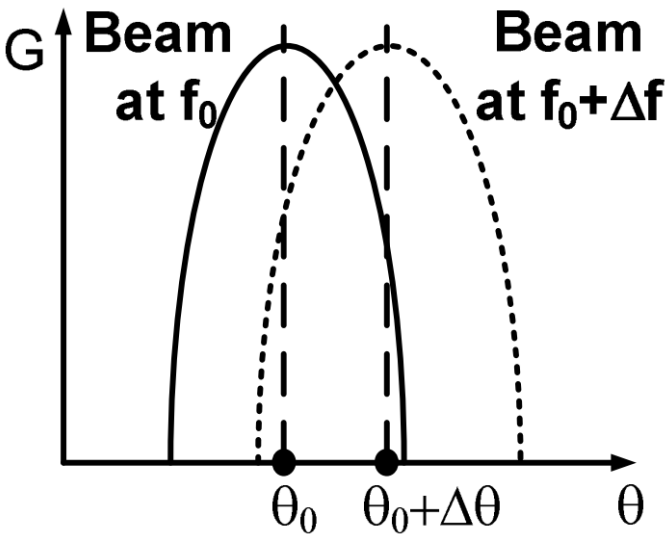


Figure 3.1 Beam squint illustration. (Garakoui et al., 2011)

3.1 System Design Specifications and Methodology

To achieve wideband performance, TTD is used instead of a phase shifter. Also, the passive structure of the TTD allows bidirectional operation. 6-bit TTD is proposed with a resolution of 1.9 ps and a maximum delay of 124 ps. 124 ps correspond to 360° at 8 GHz, and 1.9 ps correspond to 5.5°. In order to form the beam and suppress the sidelobes, a 5-bit attenuator (ATT) with 0.5 dB resolution and 16 dB attenuation range are utilized. To compansate the insertion losses of the passive attenuator and TTD, a bidirectional amplifier (BDA) is used. BDA should have an increasing gain with respect to frequency since TTD has an increasing loss in higher frequencies. BDA, TTD, and attenuator form the transceiver's common chain, and the bidirectionality will reduce the area and power consumption of the system. RF front-end of the system is composed of LNA, PA, and SPDT switch. SPDT should provide high isolation between the LNA and PA with low insertion loss. For receiver sensitivity, LNA should have low NF, maximum 3 dB, and 20 dB gain to suppress the noise contribution of the following blocks. PA should supply constant and high output power in a wide frequency band and high gain for the transmitter. 20 dB gain with 15 dBm output 1-dB compression point (OP_{1dB}) is required at the center frequency for the PA. The block diagram of the proposed transceiver is given in Fig. 3.2. TTD and attenuator are divided into two parts with BDAs between them to increase the linearity, power handling, and noise performance of the system. The number of BDAs can be changed depending on the total insertion loss of TTD and attenuator.

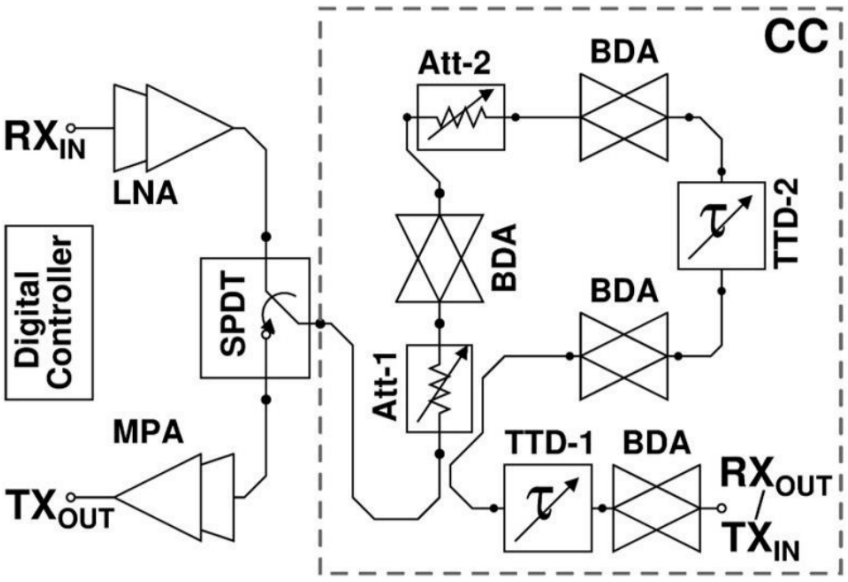


Figure 3.2 Block diagram of the proposed transceiver.

Individual sub-block performances will determine the transceiver's performance, and it is essential to carefully decide on these performance parameters. For example, if BDA and SPDT cannot achieve high enough OP_{1dB}, then the transmitter won't be able to reach an output power of 15 dBm regardless of the PA's performance since it is limited by the blocks before PA. Similar investigations can be done for the receiver as well. The losses of SPDT, TTD, and attenuator are equal to their NF, so regardless of the LNA's noise performance, other blocks can increase the receiver's NF above 5 dB if careful placement and losses of the blocks are not considered. Each sub-block should satisfy challenging specifications, each having a comparable or better performance with the state-of-the-art works in the literature. Table 3.1 summarizes each block's performance specifications and gives the proposed system performance. Input and outputs of the sub-blocks are matched to 50 Ω between 8-28 GHz. Each sub-block will be explained in a separate section. PA, BDA, and attenuator are designed by the author of this thesis and will be described in detail. TTD, LNA, and SPDT are designed by a colleague, Cengizhan Kana, and will be briefly mentioned. The reader may find detailed explanations of these blocks in his thesis (Kana, 2022). The RF front-end designed by both the author of this thesis and Cengizhan Kana will also be presented in a separate section. The proposed design procedure is as follows. First, each block will be designed according to its specifications. Then, the RF front-end and common chain (CC) will be designed separately to see the expected performance holds. Finally, after verification of the performance through measurements, RF front-end and CC will be combined.

Table 3.1 Performance Specifications for the Transceiver and Sub-Blocks

	BDA	TTD	ATT	LNA	PA	SPDT	**System**
Gain (dB)	10	-20	-10	20	20	-2	**20***
OP_{1dB} (dBm)	-2	-	-	5	15	0	**15**
NF (dB)	10	20	10	3	-	2	**5**
P_{DC} (mW)	25	0	0	50	200	0	**350**
Area (mm^2)	0.25	2.5	1	0.5	1	0.1	**6**
Amp. Err. (dB)	-	0.5	0.5	-	-	-	**0.5**
Delay Err. (ps)	-	1.9	1.9	-	-	-	**1.9**

*Both RX and TX gain.

3.2 Power Amplifier

Distributed power amplifiers (DPAs) are utilized in the literature for wideband applications and can easily cover multi-band frequencies. The well-known drawbacks of the distributed topology are the reduced gain, large area, and low efficiency. Expensive technologies such as GaN can achieve very high power levels and high efficiency of up to 35% with a cost of large size and integration problems with silicon-based systems (Campbell, 2019; Park, Nam, Choi, Kim & Kwon, 2018). With aggressive scaling in CMOS technologies, low breakdown voltages limit the output power of the devices. To overcome this limitation, transistor stacking is utilized to increase the output voltage swing (Chen, Su, Lee & Hsu, 2019; El-Aassar & Rebeiz, 2020a). Stacking is also used in SOI (El-Aassar & Rebeiz, 2020b; Çelik & Reynaert, 2021) and SiGe (Nguyen, Nguyen, Omori, Nguyen, Moroney, D'Agostino, Kennan & Pham, 2021) processes to increase the output power. However, stacking would result in poor efficiency and require complex bias networks for the additional transistors. To increase the efficiency of the DPAs, tapered line or stage scaling is employed (Fang, Levy & Buckwalter, 2016; Sewiolo, Fischer & Weigel, 2009). These solutions increased the efficiency but limited the output power and gain.

3.2.1 Design Procedure of the PA

As the number of stages increases in a distributed amplifier, bandwidth and output power increases. However, gain decreases due to the losses in the increased number of artificial transmission lines (ATLs) Kumar & Grebennikov (2015). Considering the trade-off between gain and output power, a 3-stage distributed amplifier yields a high output power, whereas the gain is still high. Most importantly, fewer inductors will result in smaller area requirements.

ATLs are formed with on-chip spiral inductors and the parasitic capacitances of the transistors in a unit cell. Equation (3.1) shows a limitation on the bandwidth, which is the cutoff frequency of an ATL. This equation suggests that a lower parasitic capacitance will result in higher bandwidth. Transistor sizes should be small to keep the parasitic capacitance low. On the other hand, small transistors will yield low transconductance and limit the bandwidth, gain and output power capability. Another design challenge is to keep the chip area small. Smaller inductor values are

beneficial to extend the ATLs bandwidth as suggested in (3.1). However, to achieve a 50 Ω characteristic impedance, the inductor value should be selected considering the parasitic capacitance, as shown in (3.2). Furthermore, transistors should be selected as small as possible to extend the bandwidth of the ATLs and keep the inductors small to save area while maintaining a high g_m to achieve the desired performance.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3.2}$$

Compared to NMOS transistors, SiGe HBTs can achieve higher current densities and lower parasitic capacitances while having the same transconductance. Also, due to higher breakdown voltages in SiGe HBTs, stacking is not required to increase the output voltage swing, increasing efficiency. Fig. 3.3 shows the schematic of the proposed DPA. The available power budget was around 170 mW to keep the efficiency high, and with V_{CC}=3.3 V, a 17 mA collector current is needed. Fig. 3.4 shows different combinations of emitter length and transistor numbers to get the maximum collector current of 18 mA (1 mA margin is left) since they will be biased close to their maximum currents to get minimum parasitic capacitance. Fig. 3.4 show that the (a) maximum f_t and (b) minimum parasitic capacitance are achieved by an emitter length of 1.5 µm and size of 1x6. Since we know each stage's capacitance value and consider the capacitances from the layout, we can calculate the required inductance from (3.2). Cascode topology is used in a unit cell due to its improved stability, high gain, and ability to achieve higher breakdown voltages.

Only a single DC voltage is required for the operation, which significantly simplifies a transmitter system's biasing and DC routing. Two active bias circuits are utilized to convert V_{CC} into appropriate bias values for the base voltages of the transistors. Base and collector lines are biased using large inductors chosen as 1 nH, the smallest value that behaves as an RF choke in the frequency of interest. Using an RF choke inductor rather than a large resistor at the base line results in a higher gain, higher output power, and symmetric layout. Bases of the cascode transistors are biased from a single bias circuit, and a 1 pF bypass capacitor is added to each base. 1 pF capacitors on the collector and base lines are purposed as DC blocks.

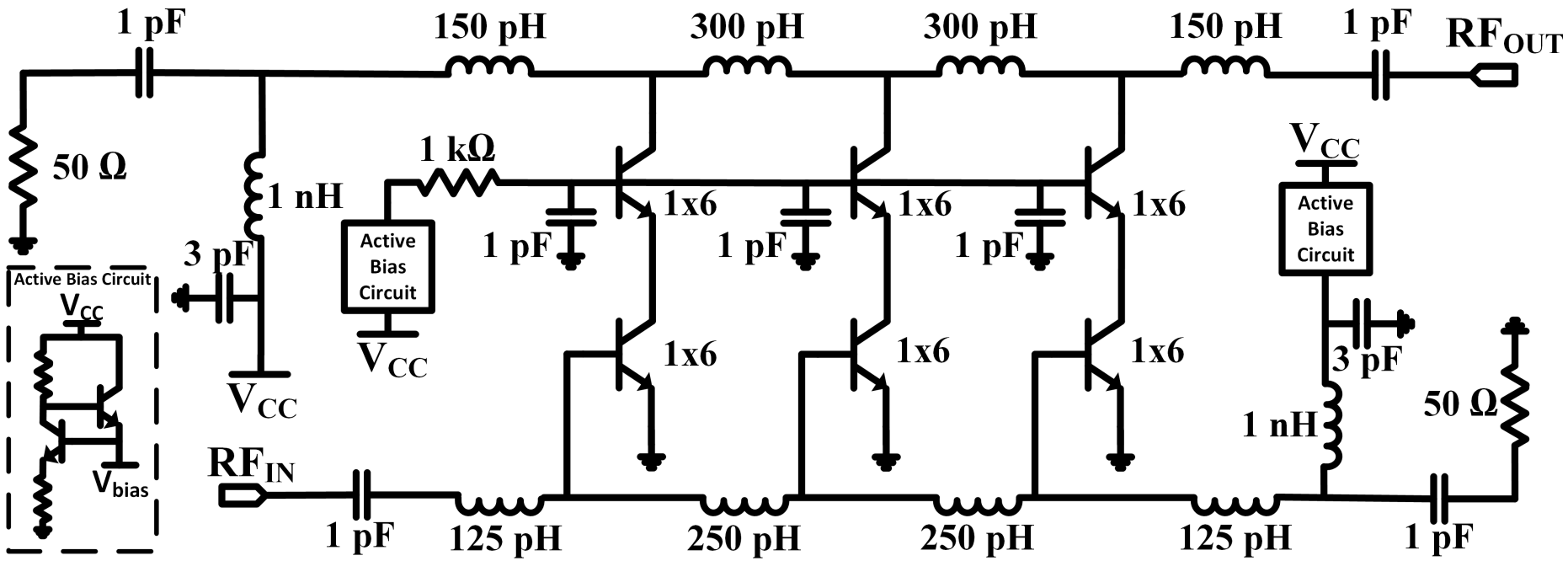
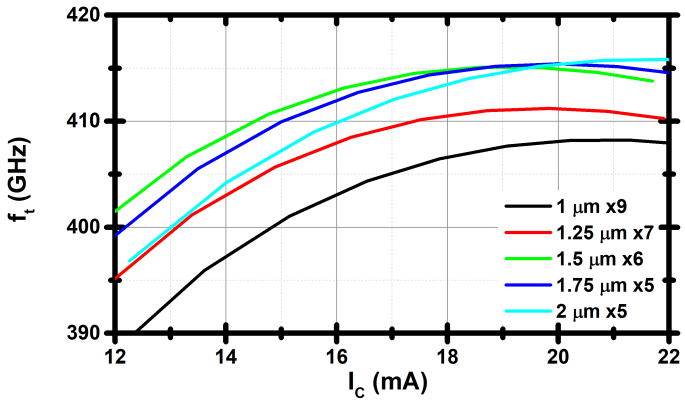
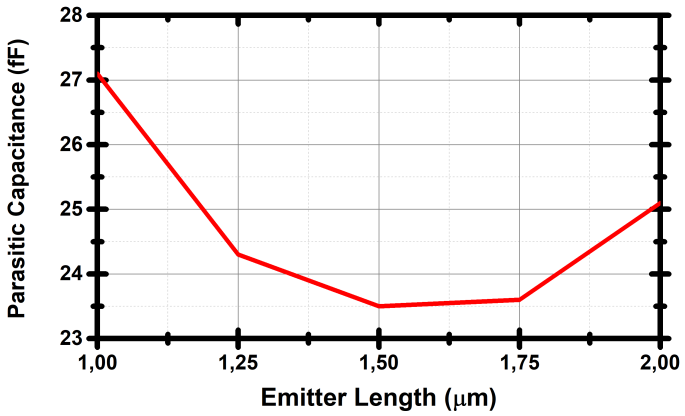


Figure 3.3 Schematic of the proposed DPA.

Inductors are placed as close as possible with ground shielding that minimizes electromagnetic interference. The width of the inductors in the collector line is specifically selected to handle high currents. A 3-stage, symmetric and compact layout decreased parasitic losses, increasing gain and efficiency and resulting in low chip area.



(a)



(b)

Figure 3.4 (a) f_t of different sized HBTs and (b) parasitic capacitance of devices, that can achieve maximum collector current around 18 mA.

3.2.2 Measurement Results of the PA

The micrograph of the proposed design is given in Fig. 3.5. Cores of three cascode stages and bias circuits are highlighted. The chip size is only 1.08x0.58 mm^2 and the core area is 0.33 mm^2. 3.3 V is applied to all V_{CC} pads, and a total of 51.8 mA is drawn from the supply. Total DC power consumption is 171 mW. Keysight N5224A PNA Network Analyzer was calibrated up to 40 GHz, and S-Parameters were measured. Measured results show a high correlation with the simulations, as

shown in Fig. 3.6. The measured peak S21 is 19.5 dB at 9.7 GHz which is the result of using a large bias inductor at the base line. Gain is 19.2 dB, 17.4 dB, and 15.5 dB at 8 GHz, 18 GHz, and 28 GHz, respectively. 3-dB bandwidth is between 4.9 and 24 GHz. Gain drops to 10.8 dB at 40 GHz. Input and output are well-matched to 50 Ω from 5 GHz to 40 GHz. S11 is below -9.5 dB, and S22 is a maximum -8 dB. According to K-Factor, the circuit is unconditionally stable up to 40 GHz.

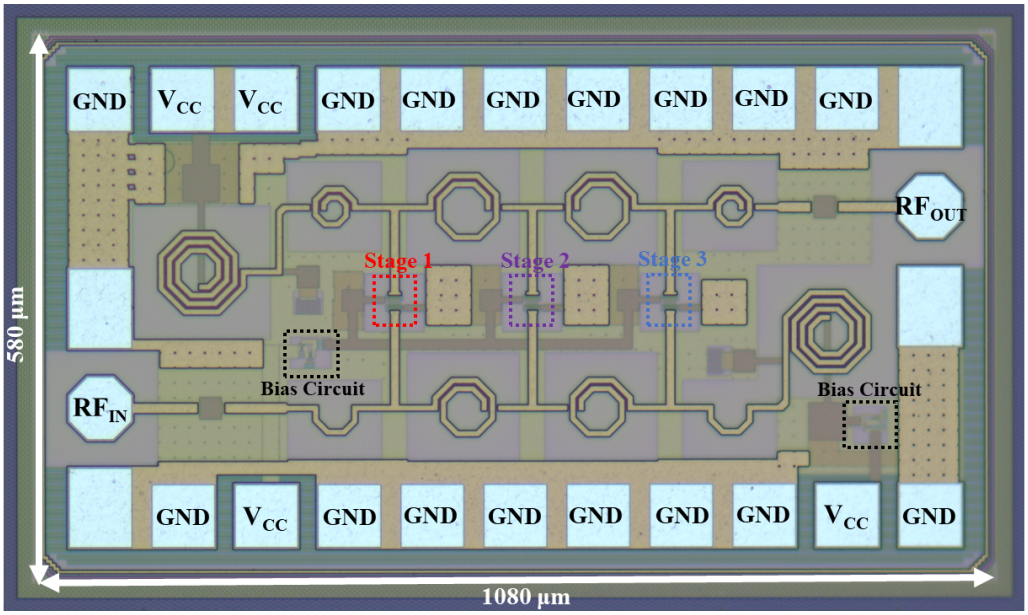


Figure 3.5 Micrograph of the proposed DPA.

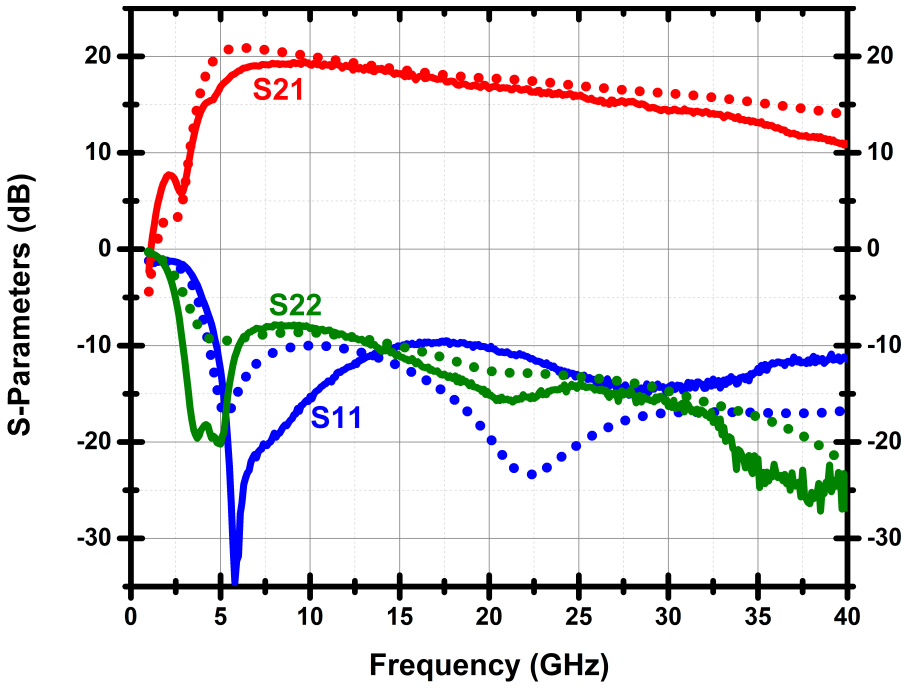


Figure 3.6 Measured (solid) and simulated (dotted) S-Parameters of the DPA.

For large-signal measurements, Agilent E8257D PSG Analog Signal Generator is used with Agilent E4448A Spectrum Analyzer. Fig. 3.7 and Fig. 3.8 shows the measured and simulated output power, gain, and power-added efficiency (PAE) versus input power for 8 and 18 GHz, respectively. Measured OP_{1dB} is 15.5 dBm and 14.4 dBm, and the saturated output power (P_{SAT}) is 17.9 dBm and 16 dBm at 8 GHz and 18 GHz, respectively. PAE is 19.4%, and 15.8% at IP_{1dB} and the peak value is 33.5% and 21% at 8 GHz and 18 GHz, respectively. Linearity measurements are also in accordance with the simulations and prove that a 3-stage compact design increases efficiency while maintaining high output power.

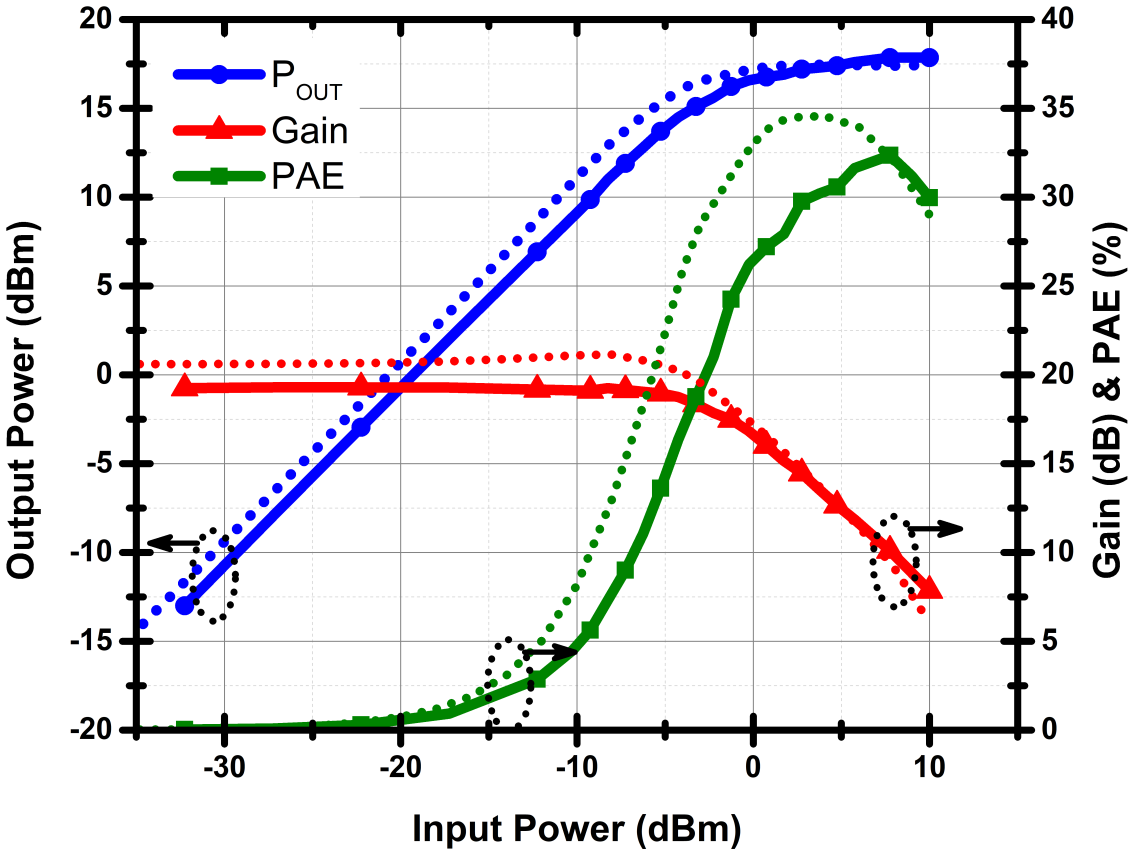


Figure 3.7 Measured (solid) and simulated (dotted) output power, gain and power added efficiency versus input power given for 8 GHz.

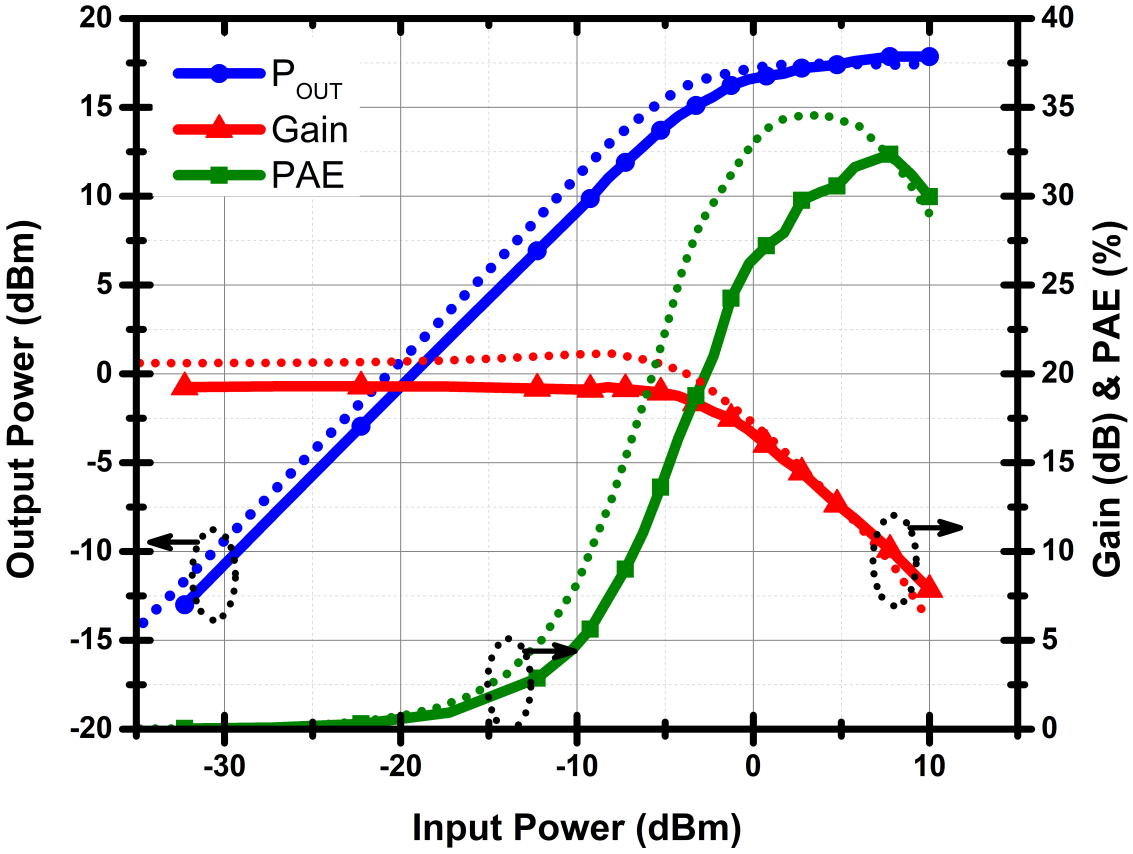


Figure 3.8 Measured (solid) and simulated (dotted) output power, gain and power added efficiency versus input power given for 18 GHz.

Output power and PAE measurements are taken from 4 GHz to 40 GHz, as given in Fig. 3.9. The top graph shows measured and simulated OP_{1dB} and P_{SAT} with respect to frequency. The highest OP_{1dB} is 16.4 dBm at 7 GHz, and it is 14.4 dBm at 24 GHz. Low variation in OP_{1dB} is achieved in the 3-dB bandwidth with only a 2 dB difference. A similar situation is valid for P_{SAT}, highest with 17.8 dBm at 7 GHz and 15.4 dBm at 24 GHz. At 40 GHz, OP_{1dB} and P_{SAT} drop to 9.6 and 10.8 dBm. Measurements and simulations of the peak PAE and PAE at IP_{1dB} are given in the bottom plot in Fig. 3.9. Peak PAE is maximum at 8 GHz with 33.5%, dropping to 17.8% at 24 GHz and 4.8% at 40 GHz. PAE at the compression point is a maximum of 26.5% at 7 GHz, and it is 15.5% and 3.9% at 24 GHz and 40 GHz, respectively.

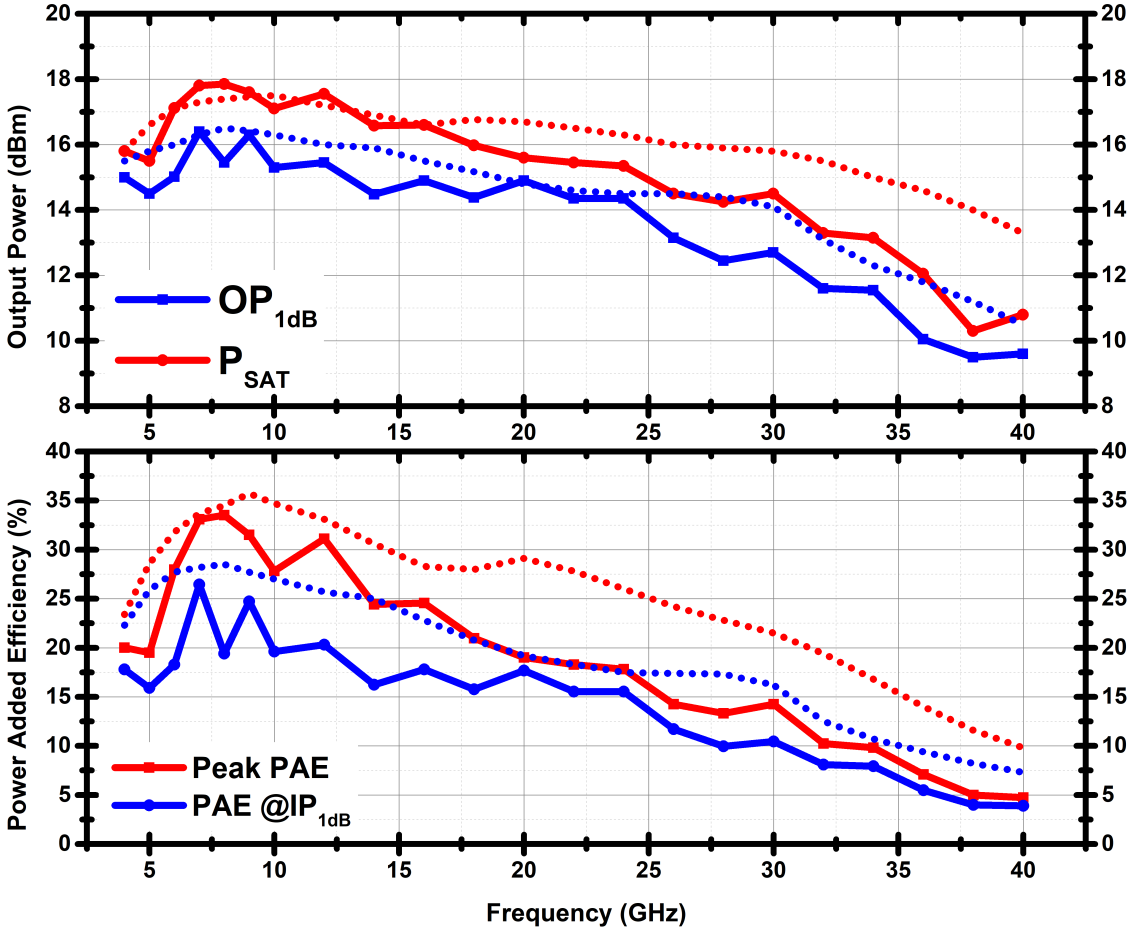


Figure 3.9 Measured output 1-dB compression point and saturated output power (top), peak PAE and PAE at the compression point (bottom) given for different frequencies. Dotted lines indicate simulation results.

3.2.3 Comparison of the PA with the State-of-the-art Works in the Literature

Table 3.2 compares the proposed design and the state-of-the-art DPAs. This work achieves the highest gain, efficiency, and area performances with high linearity. The works with higher linearity performances exhibit a high variance of OP_{1dB} in their operating frequencies, whereas it only changes by 2 dB in our work. Compared to the other works in the table, this work supports operation with one DC supply, due to on-chip bias circuits, which will be very convenient in a transmitter system. To the best of the author's knowledge, this work achieves the highest peak PAE and lowest area among the silicon-based DPAs published so far. The 3-dB bandwidth is 5-24 GHz, but this design can easily be used in the front-end of the 8-28 GHz bidirectional transceiver module.

Table 3.2 Comparison With the State-of-the-Art Silicon-Based Distributed Power Amplifiers

Reference	Technology	Frequency (GHz)	Min-Max OP_{1dB} (dBm)	Peak P_{SAT} (dBm)	Peak Gain (dB)	Peak PAE (%)	Area (mm^2)
Fang et al. (2016)	90 nm SiGe	14 - 105	4* - 14.9	17	12	12.6	1.51
Sewiolo et al. (2009)	0.25 µm SiGe	1 - 12	15* - 19.5	20 @7 GHz	12	22.1	2.1
Chen & Niknejad (2011)	0.13 µm SiGe	10 - 85	10.5* - 16.7	17.5	10	13.2	2.18
Kim & Nguyen (2014)	0.18 µm SiGe	10 - 19	11.4 @15 GHz	15.4	17.1	10	2
Tarar & Negra (2017)	0.13 µm CMOS	2 - 16	13 - 15.5	18.5	10	17	0.83
Kim (2019)	65 nm CMOS	0.5 - 38	7 - 18	21.7	15.7	25.2	3.3
Zhang & Ma (2017)	0.18 µm CMOS	2 - 22	8.9 - 14.5	16.8*	11.9	10	1.7
This Work	**0.13 µm SiGe**	**5 - 24**	**14.4 - 16.4**	**17.8**	**19.5**	**33.5**	**0.63**

*Estimated from the graphs.

3.3 Low Noise Amplifier

LNA's noise figure is crucial for the overall transceivers NF, and also, the gain should be high to suppress the noise contribution of the following blocks. Fig. 3.10 presents the schematic of the proposed LNA. This work belongs to a colleague, Cengizhan Kana. Two-stage cascode topology is employed for increased gain, where the first stage is biased and sized for simultaneous noise and power matching. Input and output are matched to 50 Ω between 8-28 GHz. Bias voltages are generated by bias circuits which enable operation using only 2.5 V. Total DC power consumption is 69 mW, including bias circuits. Fig. 3.11 shows the final layout of the LNA with input and output matching networks highlighted. The core area is 0.29 mm^2. Fig. 3.12 shows the simulated gain and NF performance of the proposed design. The maximum gain is 27.4 dB, and the minimum NF is 1.9 dB. Return losses are greater than 9 dB, and input IP_3 is a maximum -5 dBm throughout the operating bandwidth (Kana, 2022).

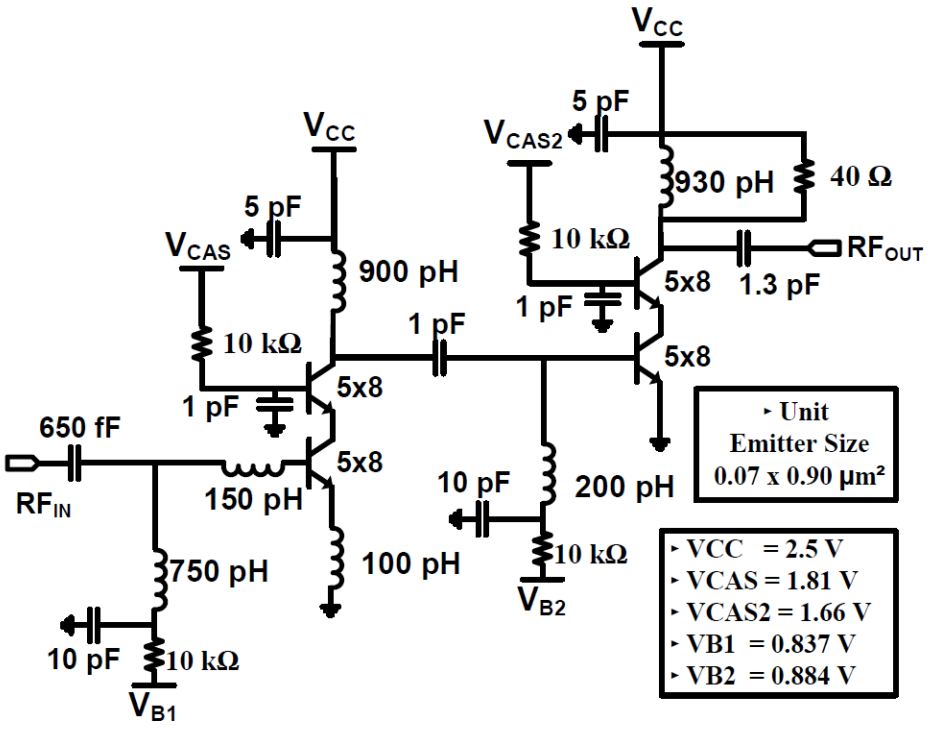


Figure 3.10 Schematic of the LNA (Kana, 2022).

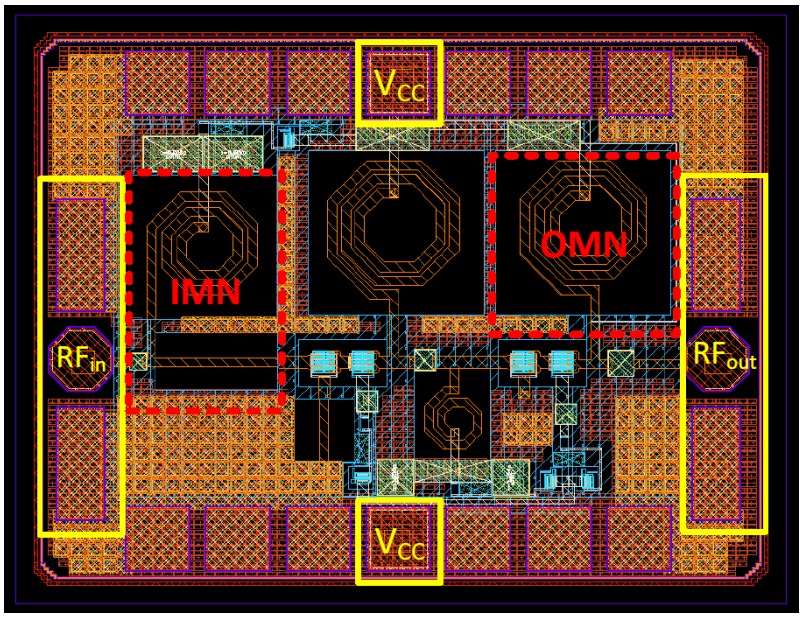
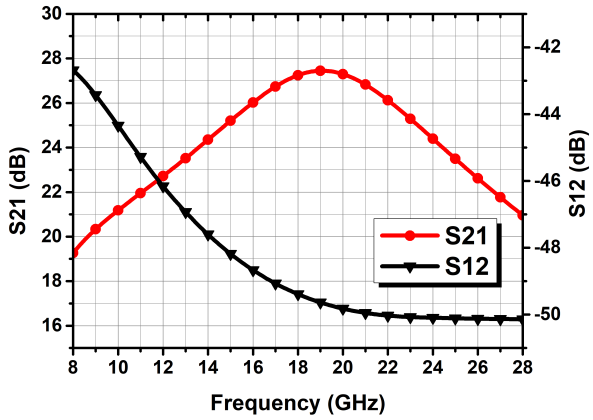
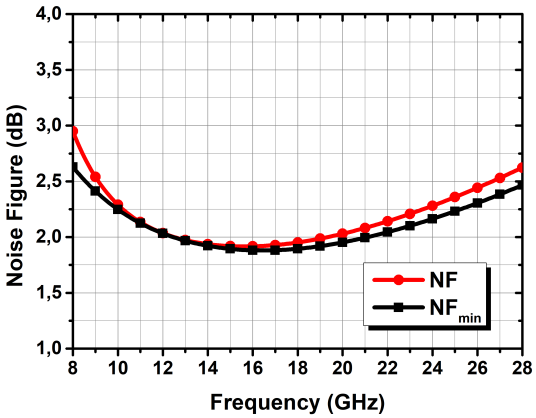


Figure 3.11 Layout of the LNA. Core dimensions are 0.68 x 0.43 mm^2 (Kana, 2022).



(a)

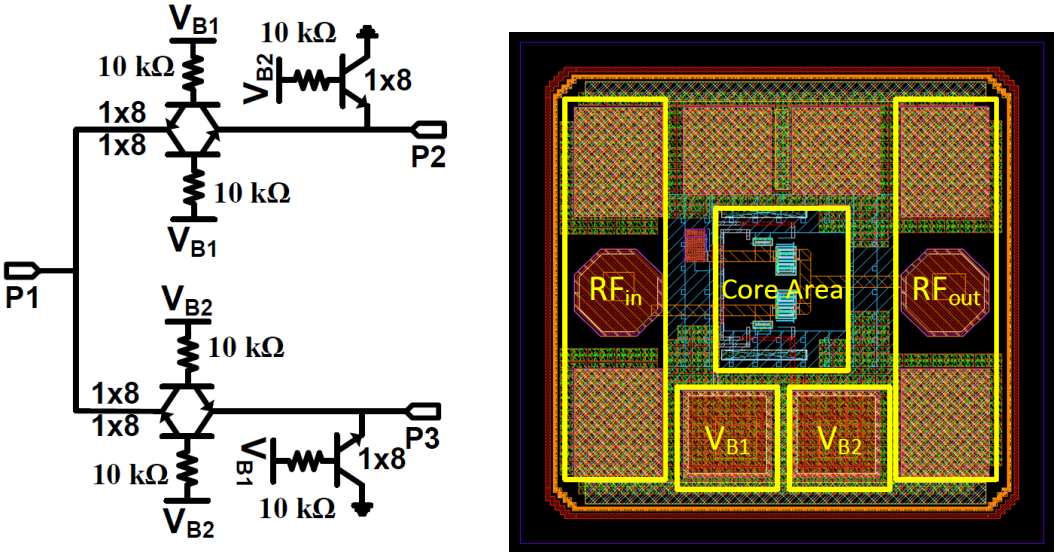


(b)

Figure 3.12 (a) Gain and (b) noise figure of the LNA (Kana, 2022).

3.4 Single-Pole Double-Throw Switch

An inductorless SPDT switch is designed using anti-parallel series switches by Cengizhan Kana (Kana, 2022). Schematic and the layout of the SPDT are given in Fig. 3.13. Control voltages are 3.3 V, and the core area of the layout is only 0.01 mm^2. The power consumption is 1.4 mW. Fig. 3.14 shows the insertion loss is maximum 1.6 dB and the isolation is minimum 25 dB. Return losses are greater than 10 dB between DC to 30 GHz, and the IP_{1dB} is 16.1 dBm at 18 GHz.



(a) (b)

Figure 3.13 (a) Schematic and (b) layout of the LNA (Kana, 2022).

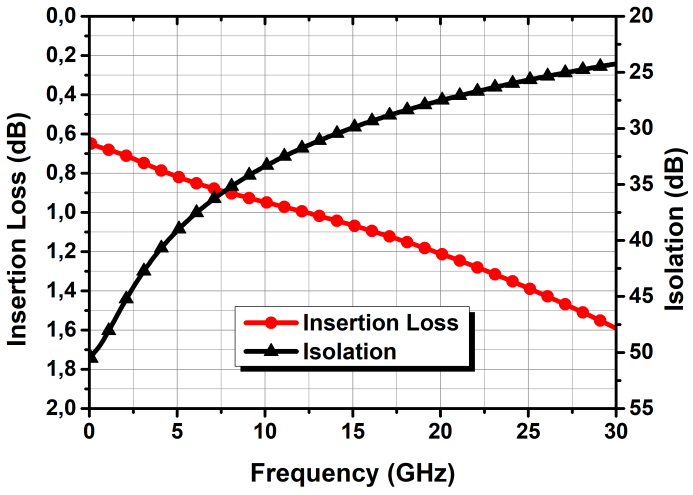


Figure 3.14 Insertion loss and isolation of the SPDT (Kana, 2022).

3.5 RF Front-End Module

RF front-end module consists of the PA, LNA, and SPDT mentioned in the previous chapters. The block diagram is given in Fig. 3.15. The LNA's input is connected to the RX_{IN}, and the PA's output is connected to the TX_{OUT}. Another SPDT is not used at these ports since III-V group LNA and PA can be used here to increase the performance further. In receiver mode, the PA is not conducting, and the SPDT is connected between the common chain and the LNA's output. In transmitter mode, the LNA is turned off, and the SPDT connects the PA and the common chain.

The connections of three sub-blocks are also EM simulated and added to the simulation results of individual blocks to analyze the performance of the front-end module. Fig. 3.16 shows the simulated gains of RX and TX in the operating bandwidth. RX gain is higher than 17 dB, and the peak gain is 25 dB. The gain is a minimum of 15 dB on the TX side with a peak of 20 dB. Fig. 3.17 shows the return losses of the ports. CC_{IN} is the output return loss when the circuit is in receiver mode, and CC_{OUT} is the input return loss when the front-end is in transmitter mode. All the return losses are higher than 9 dB between 8-28 GHz. The receiver noise figure is lower than 3 dB between 8-28 GHz, with a minimum of 2 dB, as shown in Fig. 3.18. Transmitter gain is given versus input power at 18 GHz in Fig. 3.19. The gain drops by 1 dB at an input power of -1 dBm. This corresponds to an OP_{1dB} of 15 dBm. The OP_{1dB} at 8 and 28 GHz are 16.4 and 14.3 dBm, respectively. Important port-to-port isolations are given in Fig. 3.19. In receiver mode, RX_{IN}-to-TX_{OUT} isolation is a minimum of 30 dB, and CC_{IN}-to-TX_{OUT} isolation is higher than 56 dB. In transmitter mode, RX_{IN}-to- CC_{OUT} isolation is higher than 72 dB. Fig. 3.21 shows the final layout of the front-end module, the area without pads is 0.81 mm^2, and the power consumption in TX and RX mode are 172 and 69 mW, respectively.

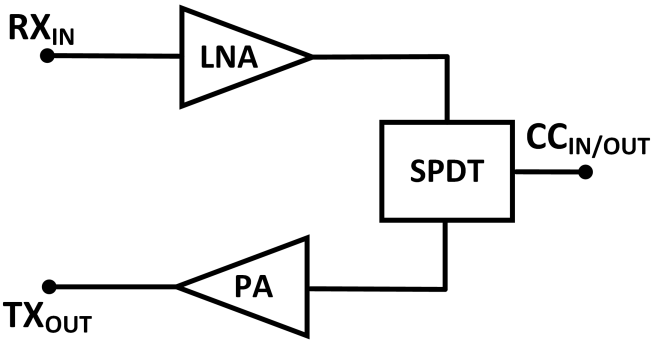


Figure 3.15 Block diagram of the front-end module.

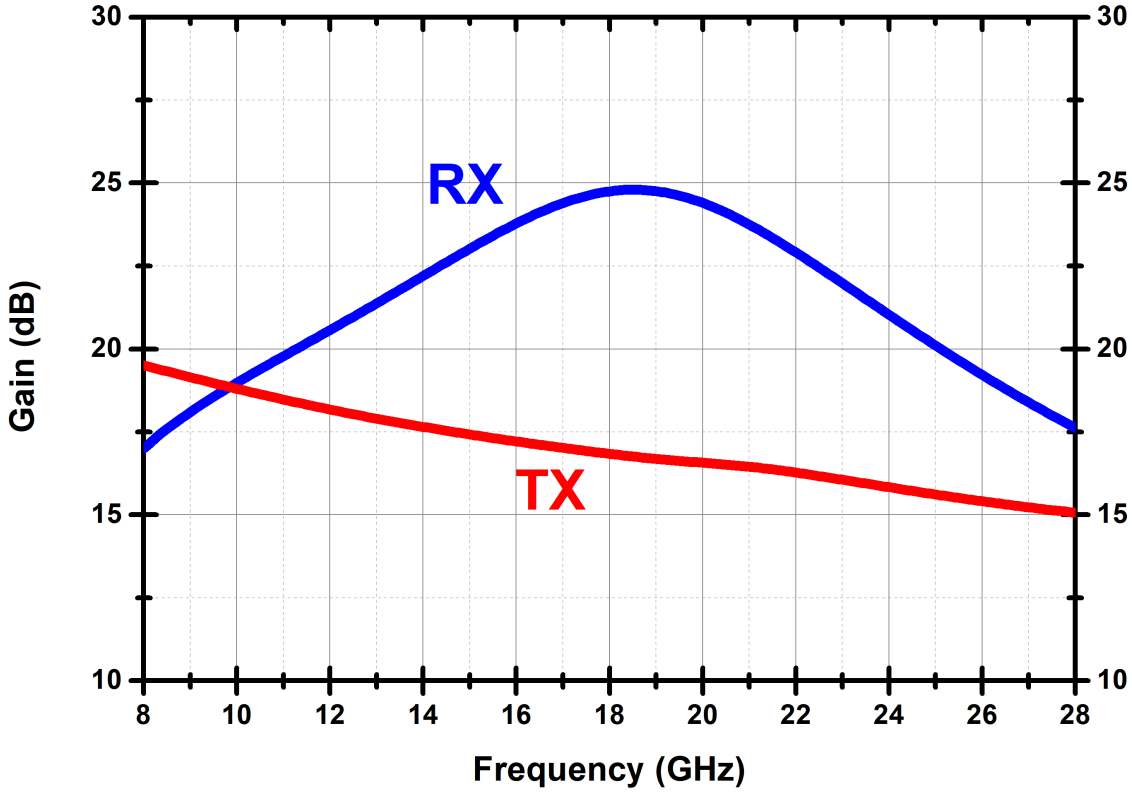


Figure 3.16 Simulated gain results of the front-end module.

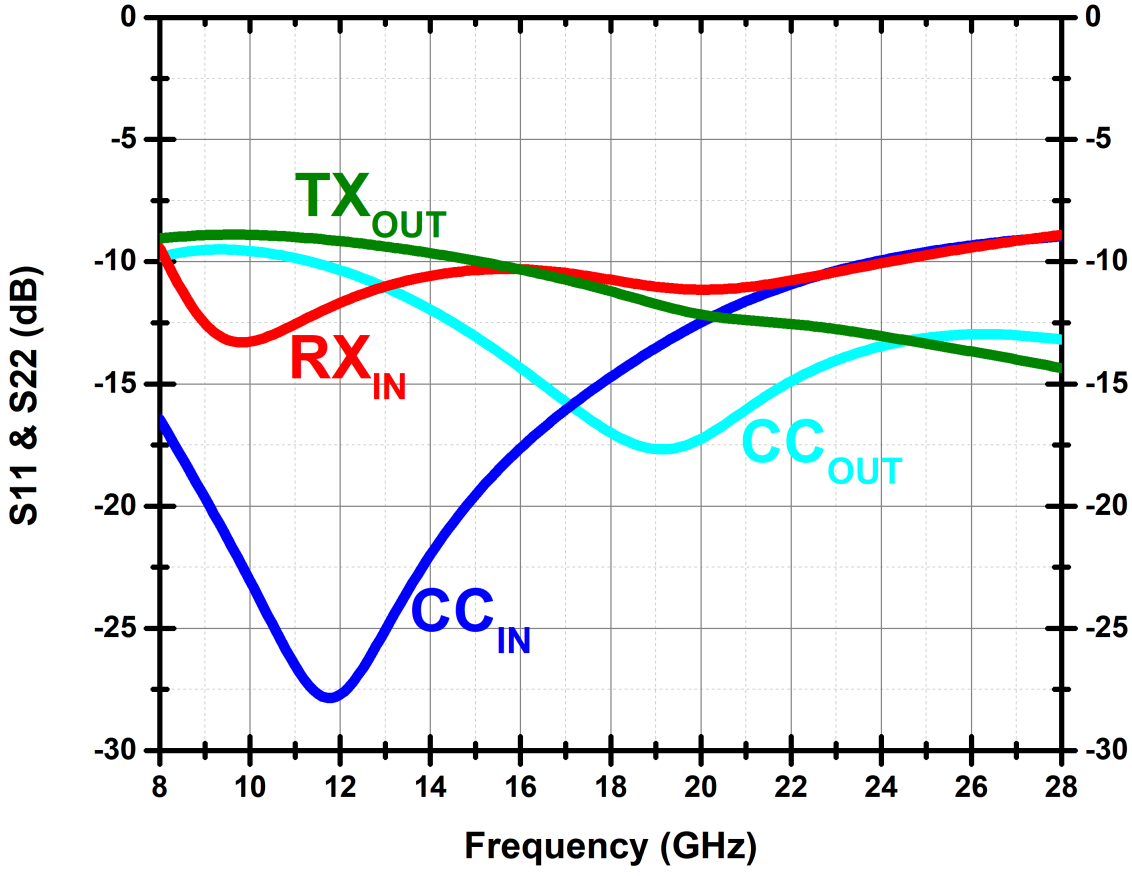


Figure 3.17 Simulated matching performance of the front-end module.

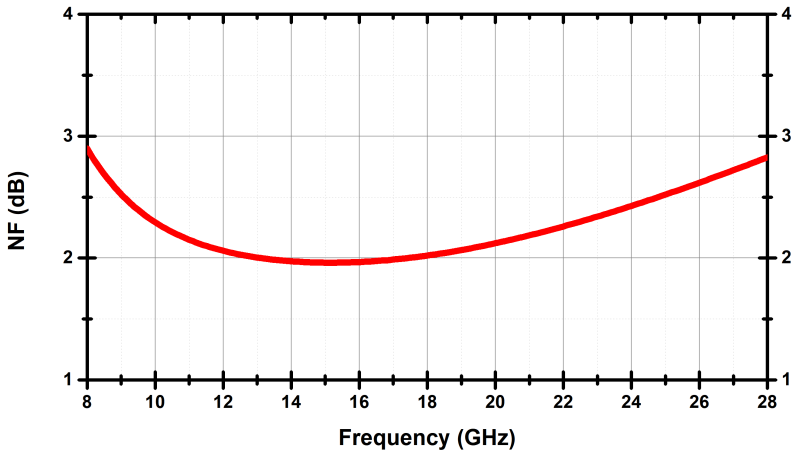


Figure 3.18 Simulated RX NF of the front-end module.

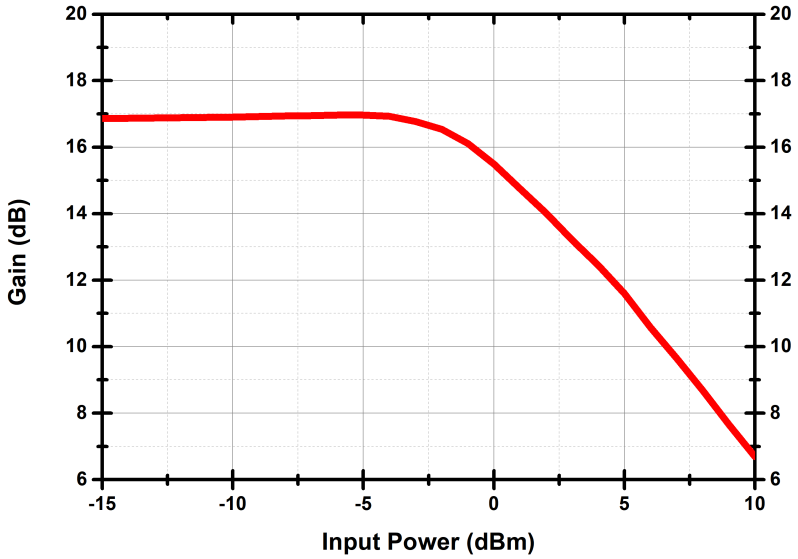


Figure 3.19 TX gain versus input power at 18 GHz. OP_{1dB} is 15 dBm.

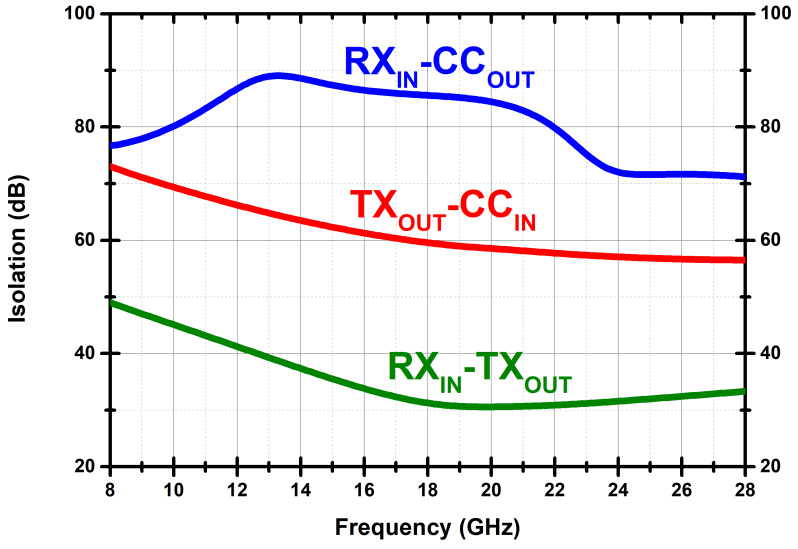


Figure 3.20 Port-to-port isolation results the front-end module.

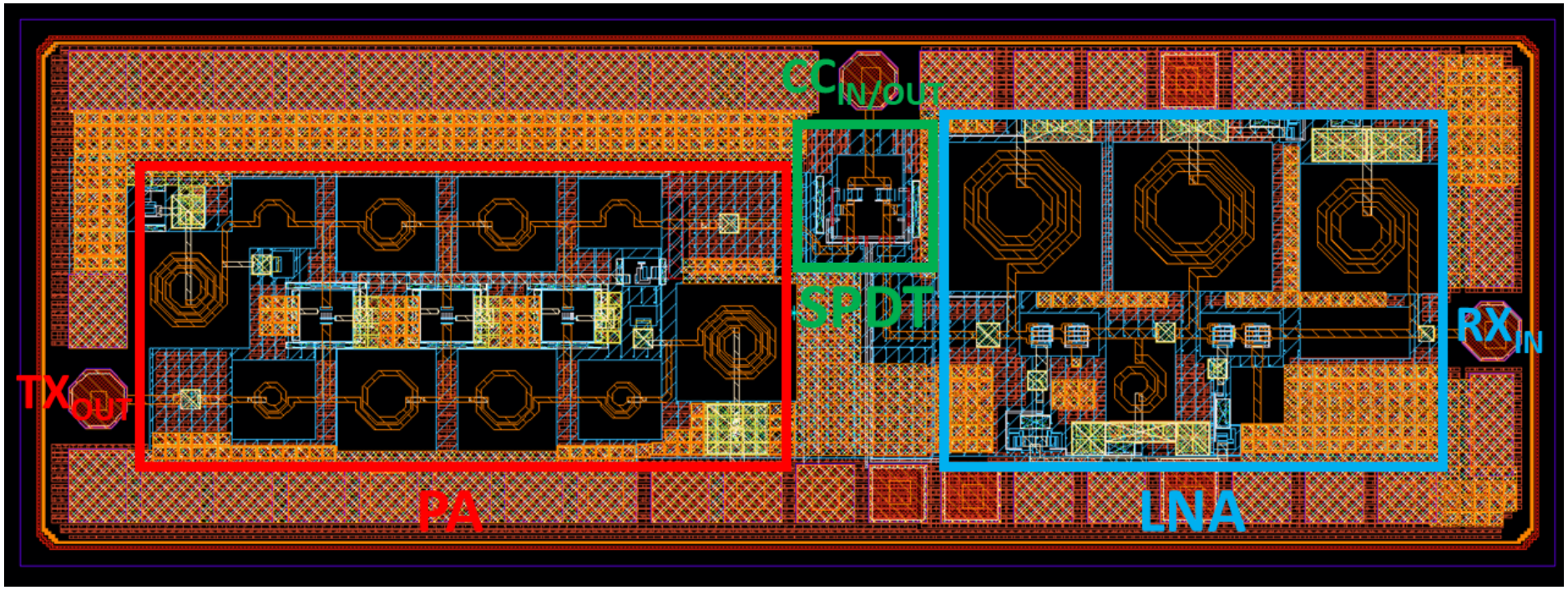


Figure 3.21 Layout of the front-end module. Dimensions are 2 x 0.7 mm^2 including pads.

3.6 Bidirectional Amplifier

The only active block in the common chain is BDA. The bidirectional operation for an active block is a challenge, and the architecture of the BDA needs to be selected according to the performance requirements. A straightforward solution might be using two amplifiers with two SPDT switches. However, SPDTs increase the performance requirements of the amplifiers since switches increase the NF and decrease the output power and gain. Another challenge is the high bandwidth of the amplifier. High bandwidth is achievable with distributed topology with a cost of area and power consumption. The BDA requires low power consumption and low area, which requires alternative architectures. Çalışkan, Yazıcı, Kaynak & Gurbuz (2020) presented a novel BDA architecture with good performance with low power consumption and high bandwidth.

3.6.1 Design Procedure of the BDA

The proposed BDA design is based on the work of Çalışkan et al. (2020), but reducing the number of inductors and capacitors. Fig. 3.22 shows the schematic of the proposed BDA. In the forward direction, Q1 and Q2 forms a cascode biased by V_{CC2} at 0.91 V through the 550 pH inductor. Q2 is biased by V_{CAS1} at 2.6 V, and collector current is supplied by V_{CC1} at 2.5 V. V_{EMIT2} is 2.5 V, V_{CAS2} is 0.9 V and V_{EMIT1} is grounded in the forward mode to ensure there is no current flow in Q3 and Q4. All the bias-purposed components are also used as matching networks. Input and output matching networks are symmetric, but the impedance is seen in Q1, and Q2 differs from Q3 and Q4 since the latter is not conducting. Hence, simultaneous matching of the input and output is challenging because the same component values should be used. Series 150 pH to the bases of Q1 and Q3 are added to increase the matched frequency range. HBTs are sized small due to low parasitic capacitance, which increases the bandwidth. Small HBTs handle low collector current at 6 mA. In the backward operation, the voltages are reversed. V_{EMIT2} will be grounded where V_{EMIT1} is 2.5 V. V_{CC2} and V_{CAS2} will be increased to 2.5 V and 2.6 V, respectively. Finally, V_{CC1} will be 0.91 V, and V_{CAS1} will be 0.9 V. Total power consumption of the BDA is 15 mW.

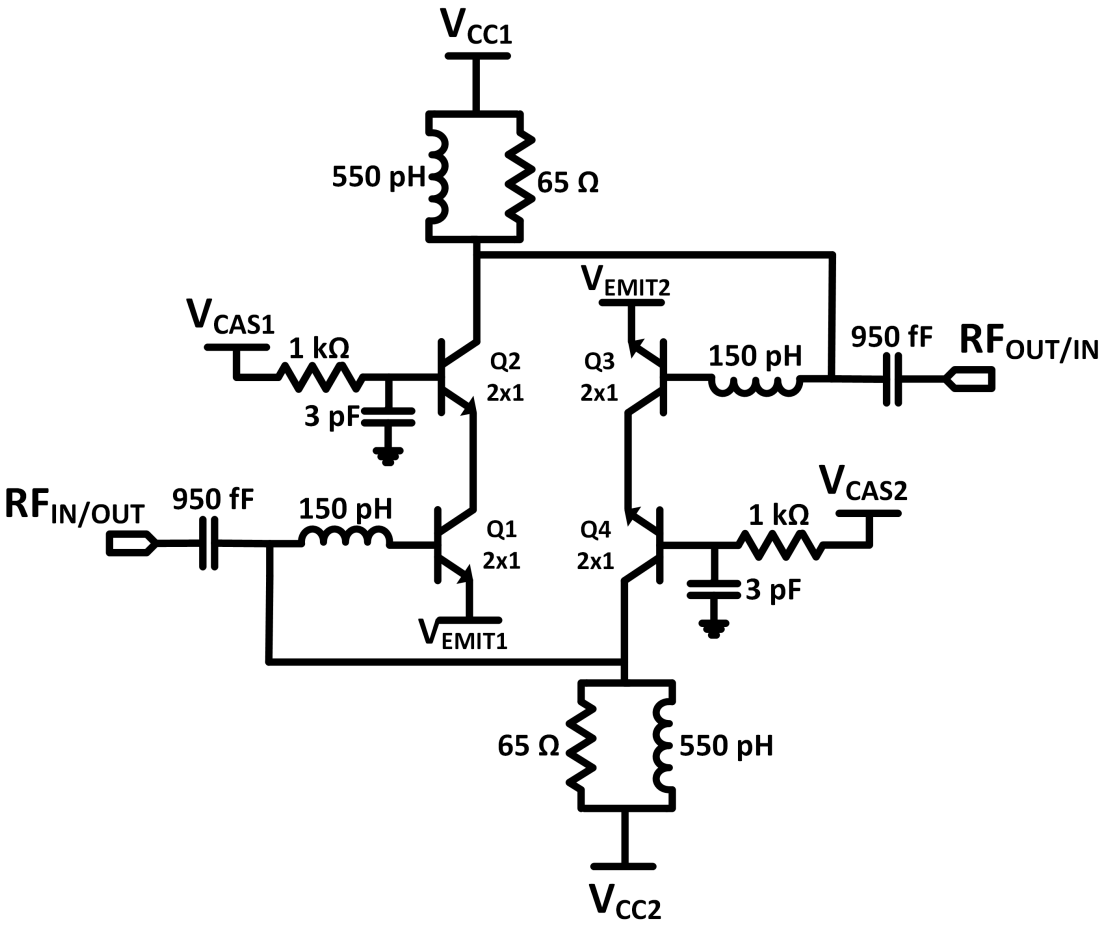


Figure 3.22 Schematic of the BDA.

Another design criterion of the BDA is to have a positive sloped gain. This means the gain should be higher in the upper parts of the operating bandwidth. Since the TTD has increasing loss with the frequency, the increasing gain of the BDA will compensate it and create a flat gain response in the common chain. The positive slope is achieved by effectively implementing an LC filter to the output. In forward operation, 550 pH at the output and the parasitic capacitance of Q3, mainly C_{be}, forms an LC band-stop filter around 13 GHz. This results in a reduced gain of around 13 GHz, leaving the gain of around 25 GHz the same. Hence, the positive slope in gain is achieved.

Layout drawing requires special attention in the BDA since the structure should be fully symmetric for identical forward and backward operations. Also, the size of the circuit needs to be as small as possible. 3D core layout of the proposed design is given in Fig. 3.23. In order to minimize the unused area, inductors are placed in the middle, where the transistors, capacitors, and transmission lines are placed at the sides. Generally, inductors are placed distant from each other to decrease coupling,

which increases area. Here, 150 pH inductors are placed on the first thick metal, whereas 550 pH are placed on the second thick metal. This layer difference decreases the coupling, and these inductors can be placed closer to each other. This technique saves the area with a small decrease in the quality factor of 150 pH inductors which has a small impact on performance. The area shown in Fig. 3.23 is 0.14 mm^2.

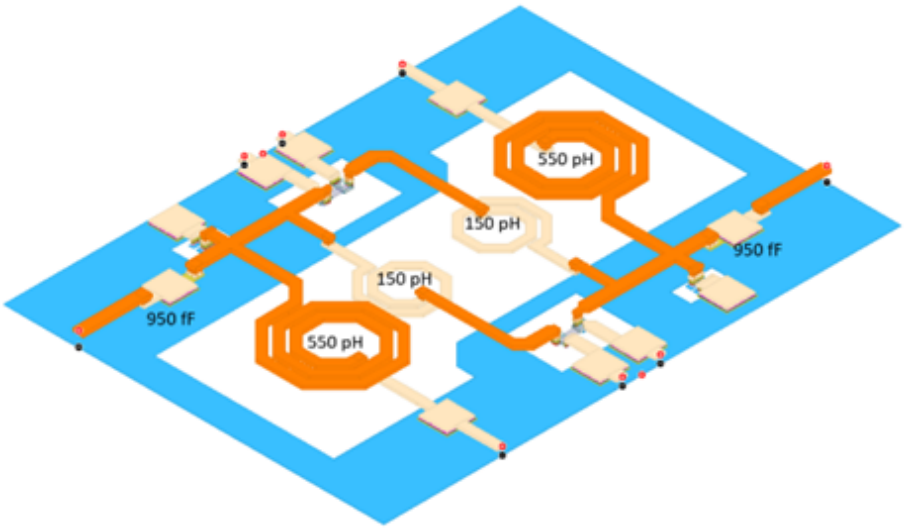


Figure 3.23 3D layout of the BDA. Dimensions are 0.41 x 0.34 mm^2.

3.6.2 Post-Layout Simulation Results of the BDA

EM simulations revealed the same performance in forward and backward operations due to a fully symmetric layout. Both ports are matched to 50 Ω. Fig. 3.24 shows the return losses of the BDA. S11 is below -9.8 dB and S22 is below -9 dB between 8 and 28 GHz. Gain performance is given in Fig. 3.25. The gain increases with the frequency up to 23.5 GHz, which is the point with the highest gain, 7.5 dB. The gains are the same at 18 and 28 GHz with 7 dB. The gain is 4 dB at 8 GHz, which makes the 3-dB bandwidth close to 8-28 GHz. The NF is given in Fig. 3.26, and it increases as the frequency decrease. This is due to the use of an LC band-stop filter for the lower frequencies. NF is 7.5 dB at 28 GHz and 9.3 dB at 8 GHz. Finally, large signal behavior at 18 GHz is given in Fig. 3.27. OP_{1dB} is -1.5 dBm at 18 GHz and 28 GHz, and it is highest at -0.5 dBm at 8 GHz.

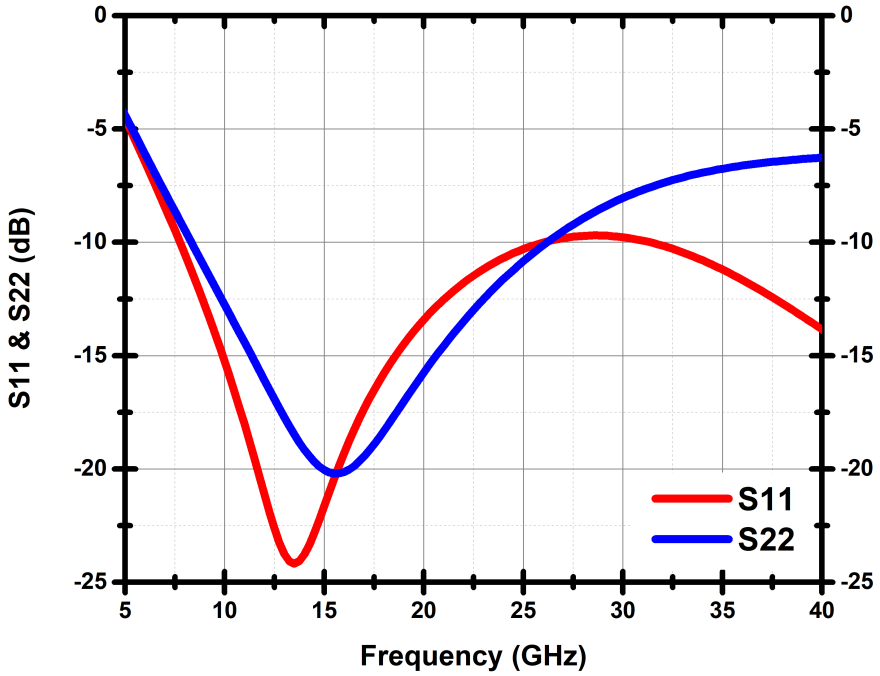


Figure 3.24 Simulated matching results of the BDA.

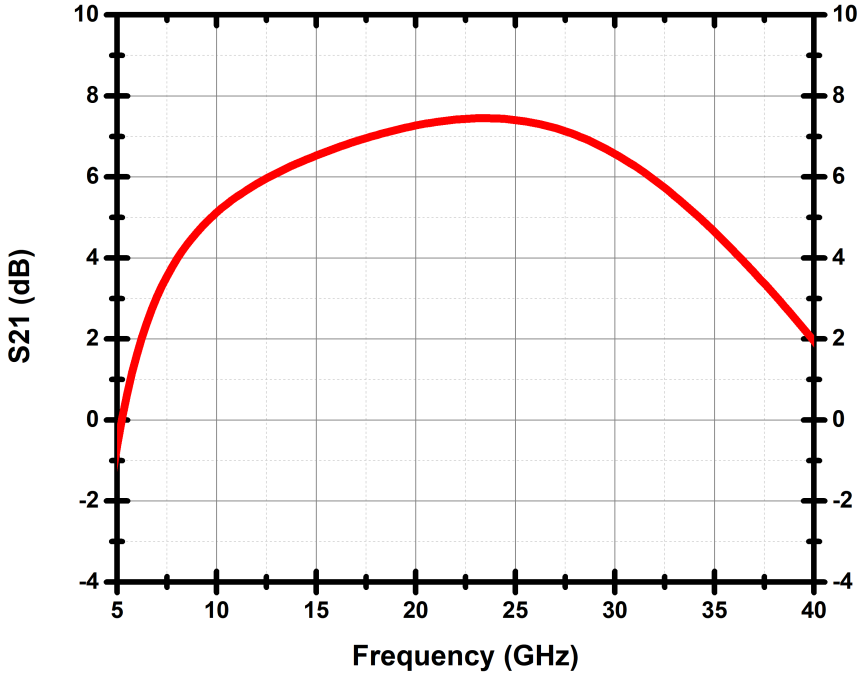


Figure 3.25 Simulated gain of the BDA.

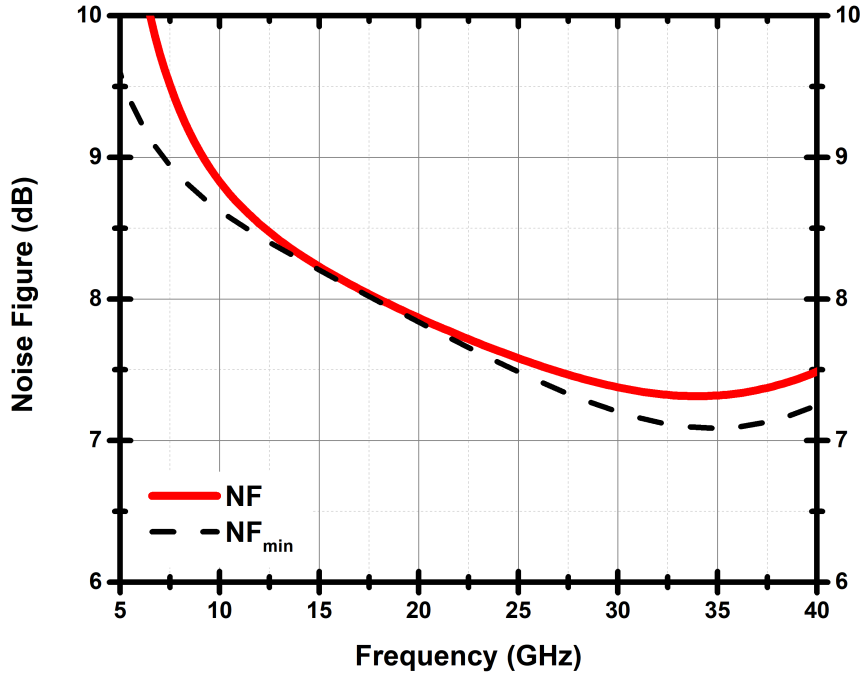


Figure 3.26 Simulated noise figure of the BDA.

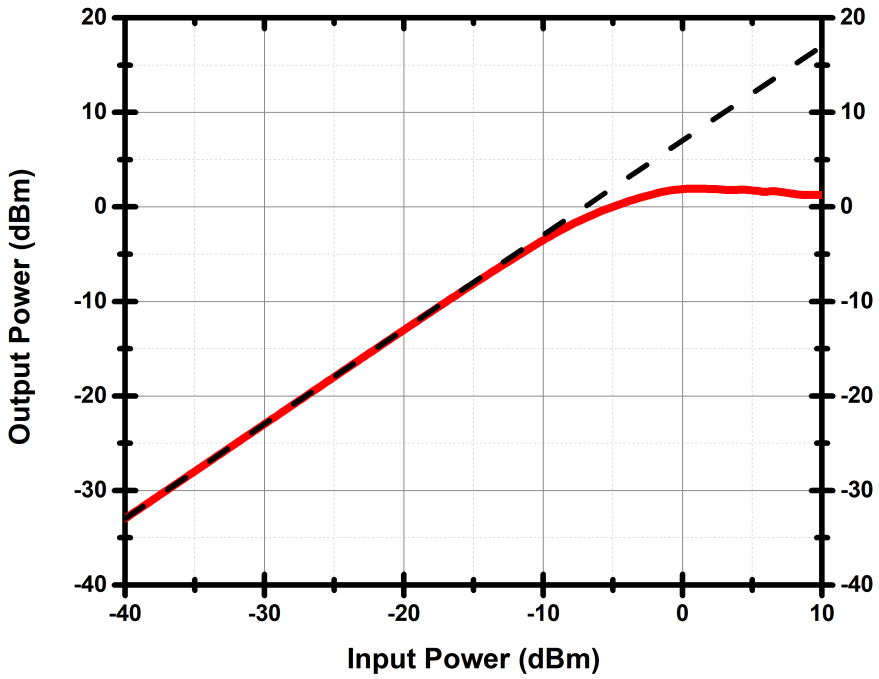


Figure 3.27 Simulated large signal behavior of the BDA.

3.6.3 Measurement Process and Comparison of the BDA with the Similar Works in Literature

The micrograph of the BDA is given in Fig. 3.28. Red and blue colors indicate forward and backward operation, respectively. The DC pads of the manufactured die of the BDA are wire-bonded to a 16-pin package. Then, the package is soldered onto a PCB with bypass capacitors. Before touching the pads with RF probes, DC voltages are applied. The voltages are slowly increased in order to ensure that there are no short circuits. However, there was 9 mA of current flowing through the collector, and there seems to be a substantial amount of current flowing through the base of Q1 in the forward mode. The voltage values at the bases and collectors of the transistors could not be maintained due to the increased current flow. As a solution, resistors are used off-chip to supply the voltages for the V_{CC} pads. Still, the required voltage levels could not be maintained due to the increased current flowing through the chip. The measurement is still ongoing, and the fault in the chip is being investigated. So far, three different dies have been measured, and two more are ready to be measured. The wire-bond inductances did not cause any oscillations in the simulations, but the measurements will be repeated using DC probes to decrease these inductances.

Table 3.3 summarizes the simulated performance of the BDA and compares it with similar works in the literature. The main design specifications were achieved with the smallest area and lowest power consumption.

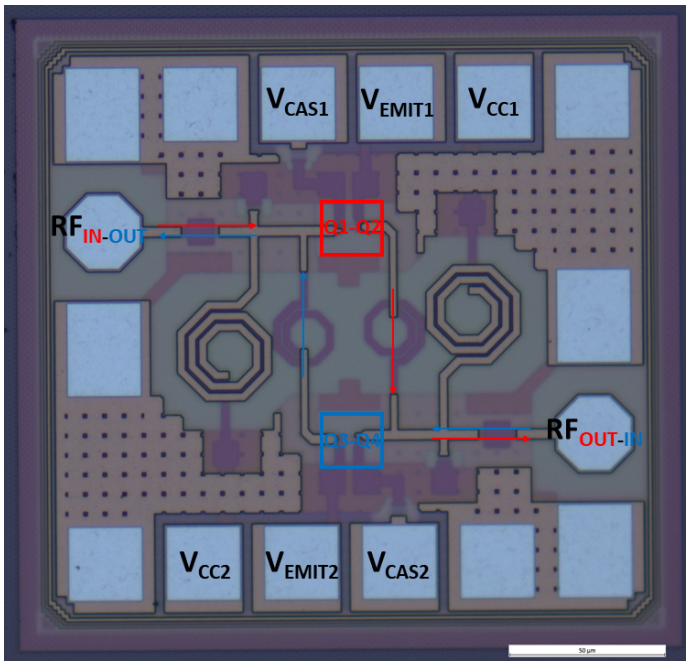


Figure 3.28 Micrograph of the BDA. Dimensions with pads are 0.62 x 0.58 mm^2.

Table 3.3 Comparison with Bidirectional Wideband Amplifiers in the Literature

Reference	(Cho et al., 2013)	(Song et al., 2016)	(Sim et al., 2013)	(Cho et al., 2016)*	(Gong et al., 2018)	**This Work***
Technology	0.13µm CMOS	0.13µm SiGe	0.13µm CMOS	0.13µm SiGe	0.13µm SiGe	**0.13µm SiGe**
Frequency	3-20 GHz	2-22 GHz	5.5-14 GHz	2-22 GHz	26-29 GHz	**8-28 GHz**
Gain	11 dB	9.6 dB	6.2 dB	6 dB	10 dB	**7.5 dB**
NF	3.2 dB	-	6	-	3.9	**7.4 dB**
OP_{1dB}	6 dBm	3.4 dBm	7.4 dBm	-1.2 dBm	6.9	**-0.5 dBm**
P_{DC}	68 mW	100 mW	43 mW	25 mW	27 mW	**15 mW**
Area	0.82 mm^2	1.3 mm^2	0.23 mm^2	1.04 mm^2	0.64 mm^2	**0.16** mm^2

*Have positive gain slope. **Area without pads.

3.7 Attenuator

The attenuator is responsible for controlling the amplitude of the signal in the common chain. Ideally, the attenuator should keep the phase constant. In an N-bit attenuator, there are 2^N attenuation states. The least significant bit (LSB) is the difference between these states, also called resolution. Resistive passive attenuator architectures are widely used in the literature due to their simple structures and wideband performances. The switching transistor is the limiting factor in these applications. When the transistor size increases, the phase error increases due to the higher parasitic capacitance. However, when a small transistor is used, the insertion loss increases. For the 8-28 GHz bidirectional common chain, a 5-bit digital step attenuator is designed. SiGe HBT switches are used because of the reliability in the manufacturing process and the decrease in the insertion loss when reverse saturated HBTs are used as shunt devices (Davulcu et al., 2020). The attenuator is planned to be added in two pieces, previously mentioned in Fig. 3.2. The first piece will contain the first two bits, and the other will contain the last three bits. The simulation results of these pieces will be given in different subsections, and the rms phase and amplitude errors will be given in a different subsection for the combined version.

3.7.1 Design and Post-Layout Simulation Results of the First Two Bits

T-type is considered for smaller attenuation steps, such as 0.5 and 1 dB. However, a more straightforward solution would yield good performance, as shown in Fig. 3.29. The shunt device in the T-type network is omitted. Only a resistor and a bypass transistor are used for both steps. When the series transistor (Q_S) is on, it forms the reference path with very low resistance, and when the transistor is off, the resistance will decrease the amplitude of the signal. Transistors are selected as 1x8, which achieves low phase error at the expense of higher insertion loss. This increase in insertion loss (IL) can be tolerable compared to the loss of the TTD. Fig. 3.29 shows the first two bits and the 10 kΩ resistors for DC isolation. Also, 8 pF capacitors are used for DC blocking purposes. Matching networks are not required, which also reduces area. Fig. 3.30 shows the layout of the first two bits. The DC block capacitors are not added to the layout yet. The area is only 0.02 mm^2, which will be the core area.

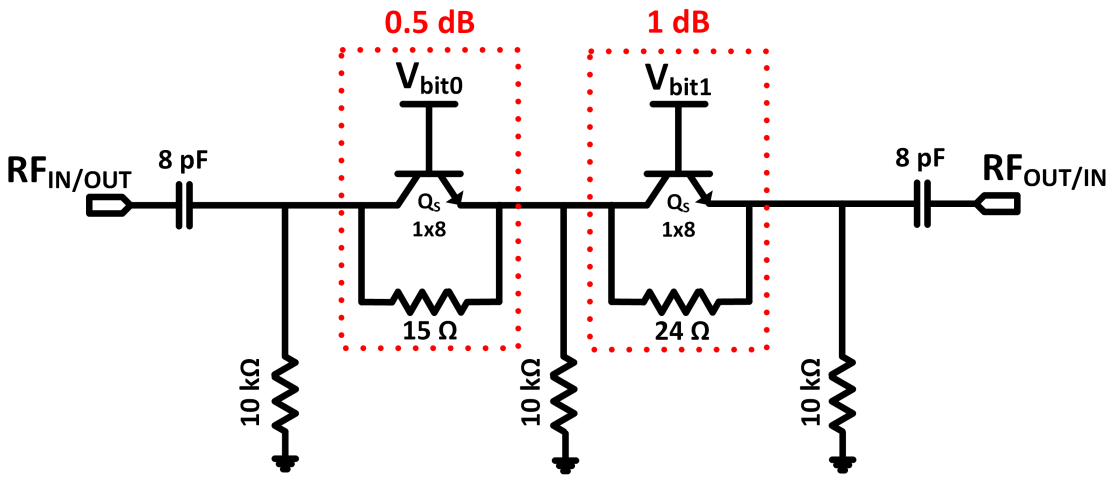


Figure 3.29 Schematic of the first two bits.

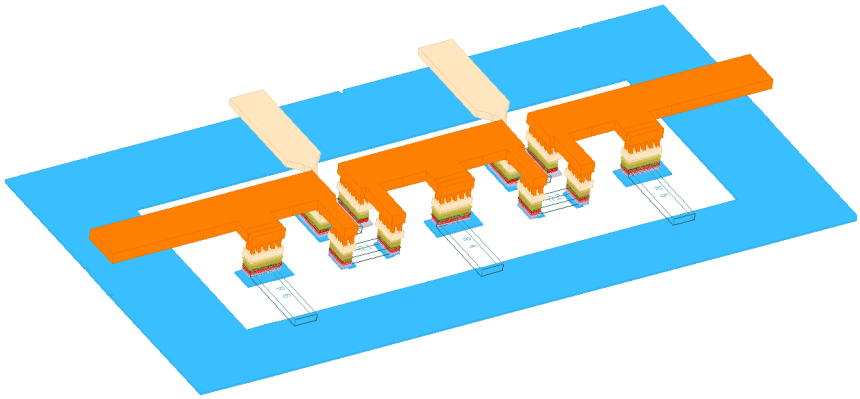
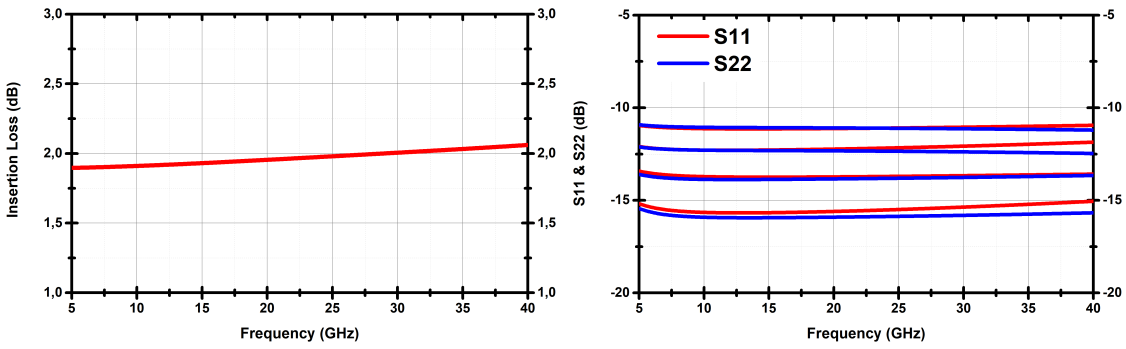


Figure 3.30 3D layout of the first two bits. Area is 0.2 x 0.1 mm^2.

The simulated results are given between 5-40 GHz. Attenuation states for the first two bits are flat with respect to frequency as given in Fig. 3.32. The input and output return losses are higher than 10 dB for all states, and the insertion loss is around 2 dB, as given in Fig. 3.31. The IP_{1dB} at 18 GHz is very high with 20 dBm due to only two cascaded bits.



(a) (b)

Figure 3.31 (a) IL and (b) input and output matchings of the first two bits.

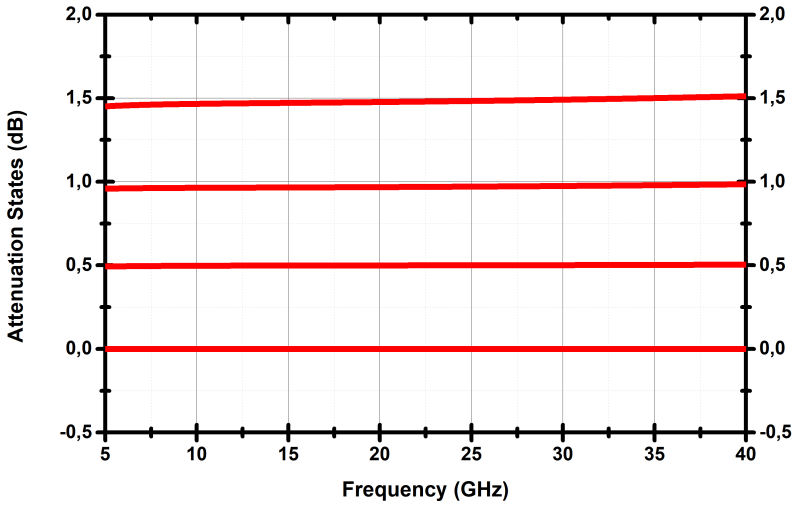


Figure 3.32 Attenuation states of the first two bits.

3.7.2 Design and Post-Layout Simulation Results of the Last Three Bits

For higher attenuation bits, shunt devices are required. Pi-type networks are utilized for the remaining 2, 4, and 8 dB attenuation steps. Fig. 3.33 shows cascaded bits. The best performance is achieved when 8 dB is in the middle. For 4 and 8 dB steps, the phase (or delay) error increased too much, so a phase correction network was implemented. This network consists of an inductor that will resonate with the parasitic capacitance of Q_S, which will lower the phase error. All the transistor sizes are equal, and Q_P is selected as 1x2 to reduce the phase error. The layout is given in Fig. 3.34 and the area is 0.07 mm^2. Fig. 3.35 shows that the IL is below 4 dB, and input and output return losses are higher than 10 dB, between 5-40 GHz. The attenuation steps are also flat with the frequency with slight variances in the higher attenuations, as shown in Fig. 3.36. The IP_{1dB} of this piece is 14 dBm at 18 GHz.

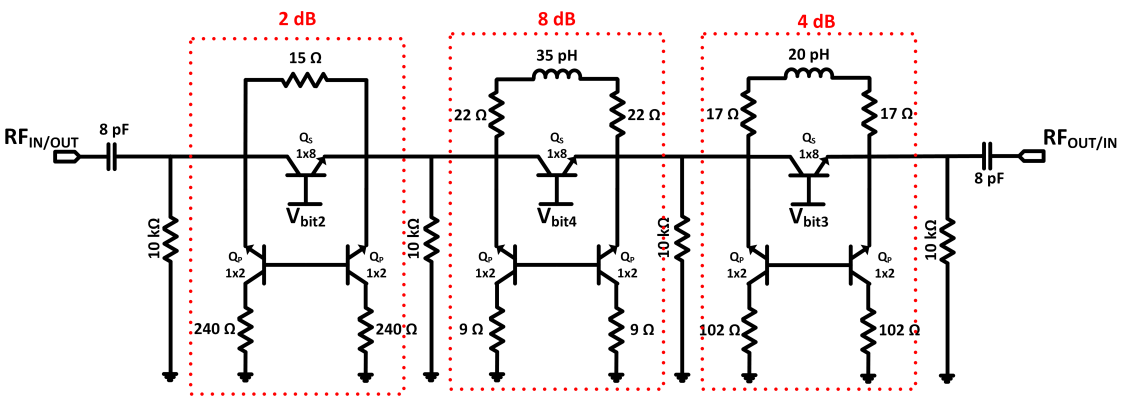


Figure 3.33 Schematic of the last three bits.

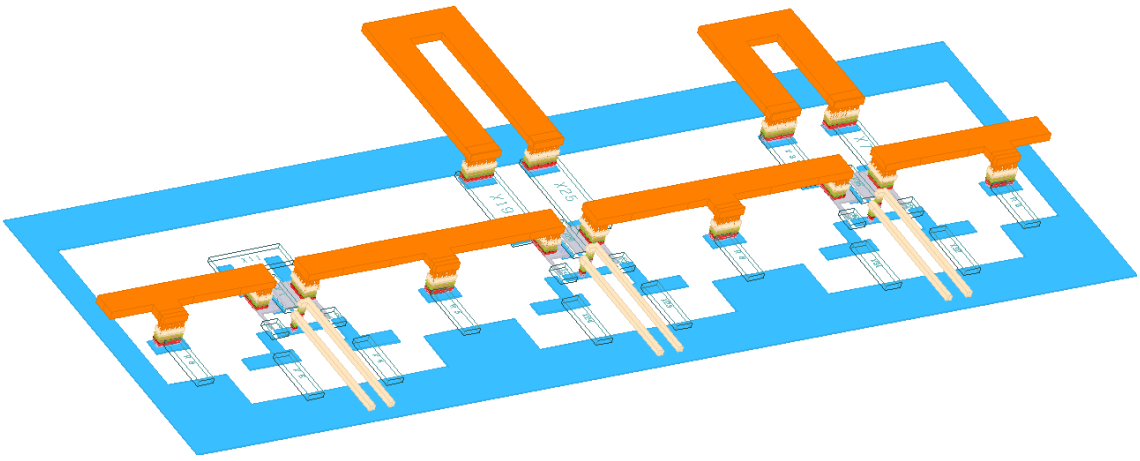
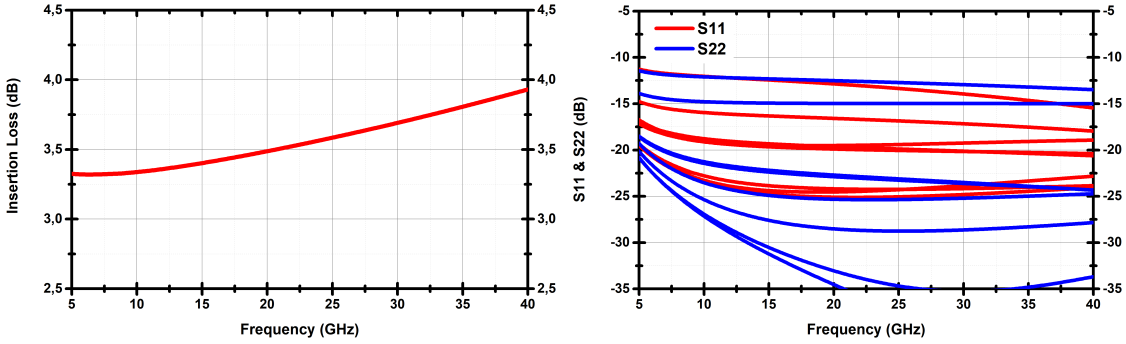


Figure 3.34 3D layout of the last three bits. Area is 0.38 x 0.19 mm^2.



(a) (b)

Figure 3.35 (a) IL and (b) input and output matchings of the last three bits.

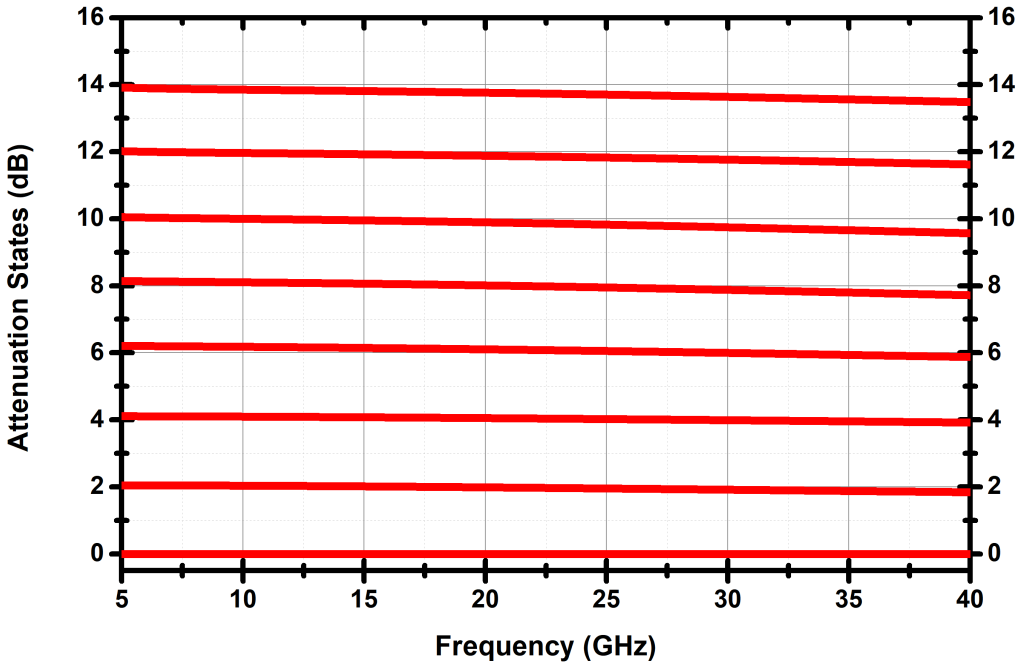


Figure 3.36 Attenuation states of the last three bits.

3.7.3 Delay, Phase and Amplitude Errors of the Attenuator

Both pieces of the attenuator are combined in a test bench to analyze delay, phase, and amplitude errors for 32 possible states. The attenuation states are given in Fig. 3.37. The states are not perfectly homogenous, but there is a clear distinction between each state, and there are no overlaps. The rms amplitude error will help quantify the deviations. Fig. 3.38 shows the rms amplitude and phase errors, as well as the insertion loss. The rms amplitude error is below 0.26 dB between 5-40 GHz, with a minimum of 0.11 dB. The rms phase error is around 1° throughout the band with a maximum of 1.15°. The insertion loss is maximum 6.2 dB at 40 GHz, and it is minimum 4.8 dB at 5 GHz. The IP_{1dB} of the cascaded stages are 13 dBm at 18 GHz. Due to the nonzero base current, the DC power consumption is 3 mW.

Since time delay is utilized in the transceiver module, the delay difference is also simulated. Fig. 3.39 shows the difference of all 32 states' delays from the reference state. The delay difference is below 0.5 ps between 8-28 GHz, which is almost a quarter of the minimum time delay (1.9 ps).

Full schematic of the proposed design is given in Fig. 3.40. Overall, the performance is solid with small size, low insertion loss and rms amplitude error, and high IP_{1dB} and small delay variation in a wide bandwidth. This design meets the specifications to be used in the common chain. The bidirectional operation is supported with very small variations in attenuation states due to the asymmetric nature of HBTs.

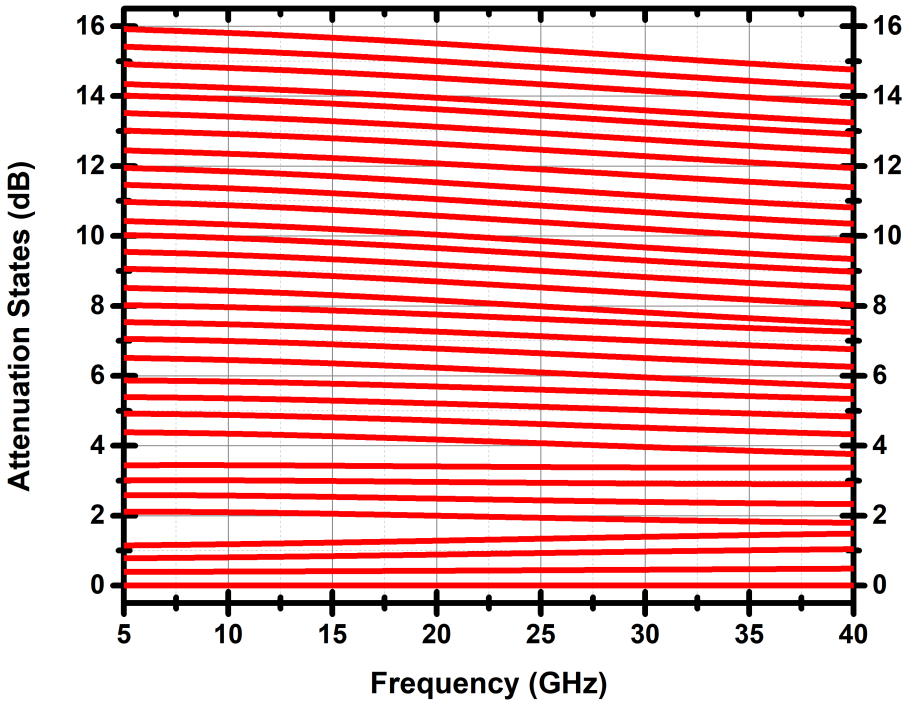


Figure 3.37 All 32 attenuation states of the attenuator.

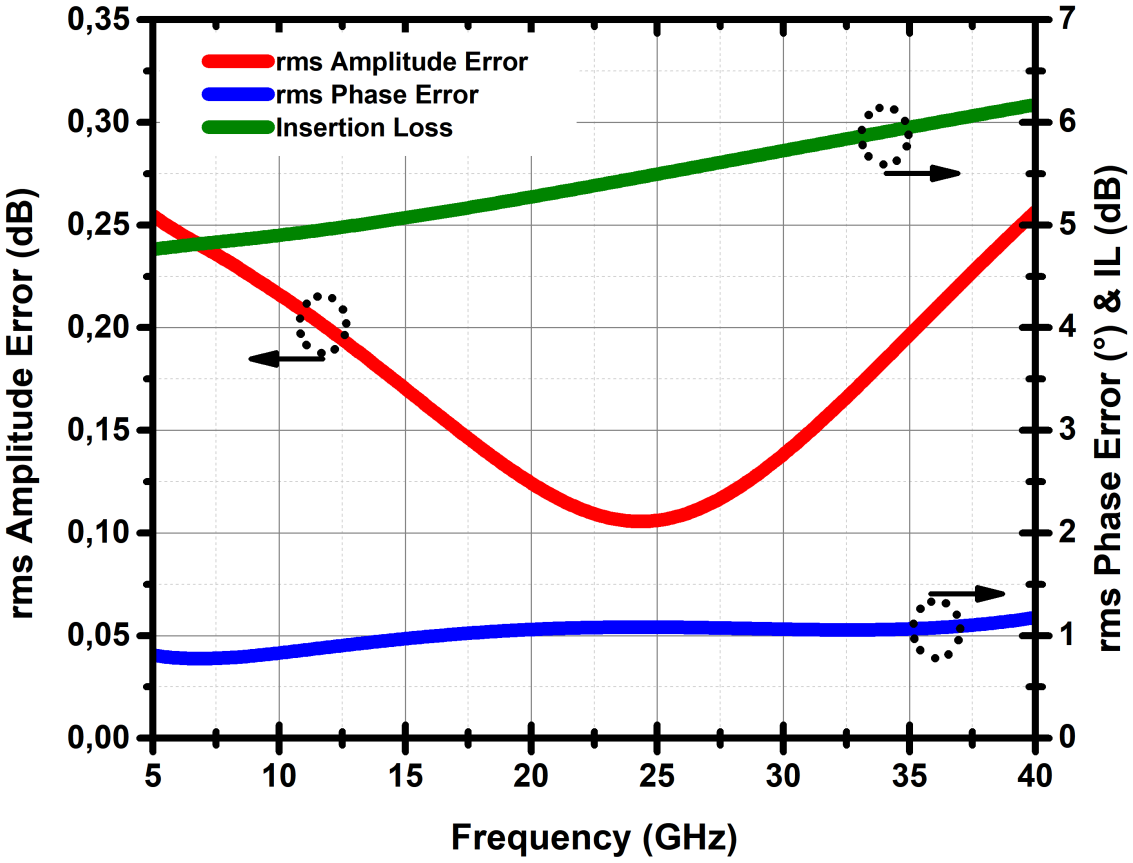


Figure 3.38 Insertion loss, rms phase error and rms amplitude error.

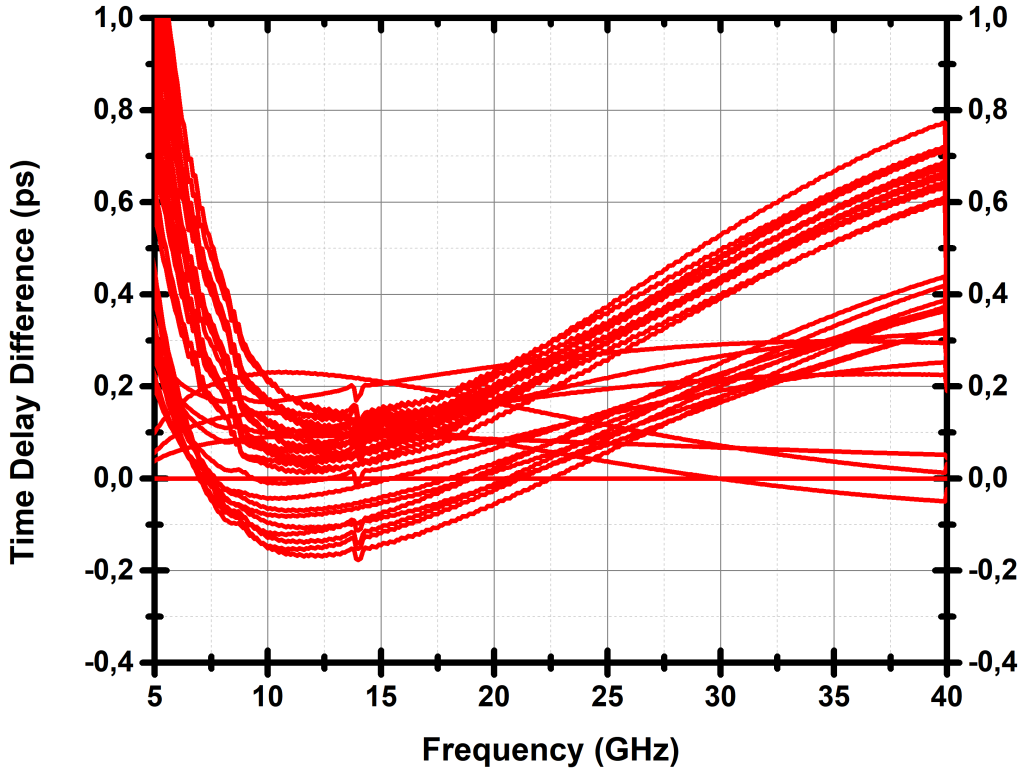


Figure 3.39 Time delays of all states, subtracted from the reference state.

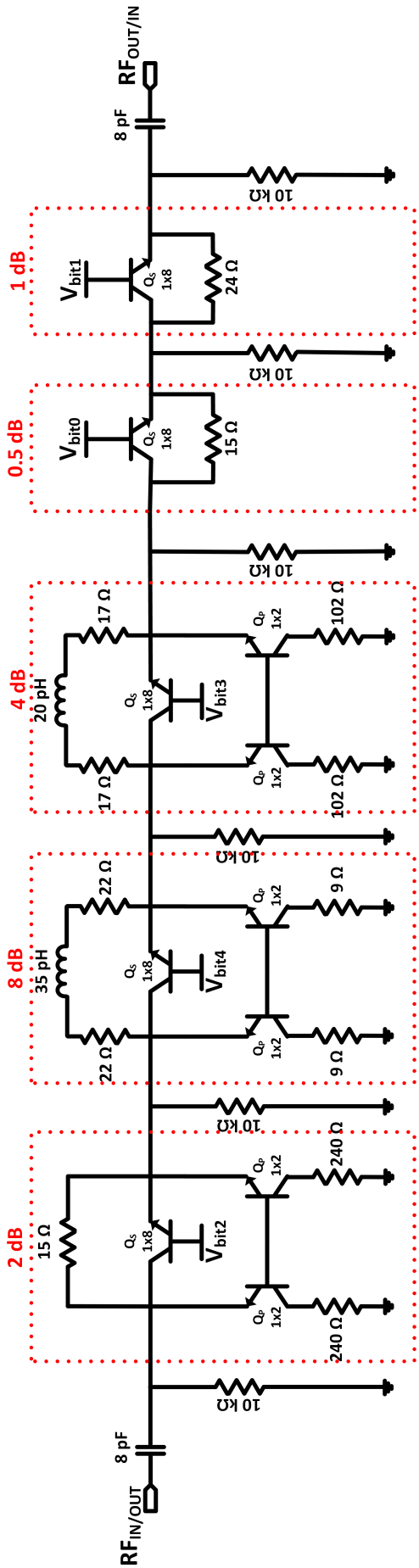
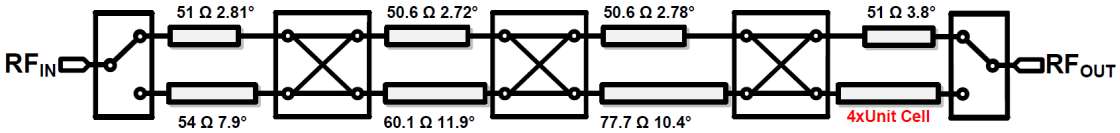


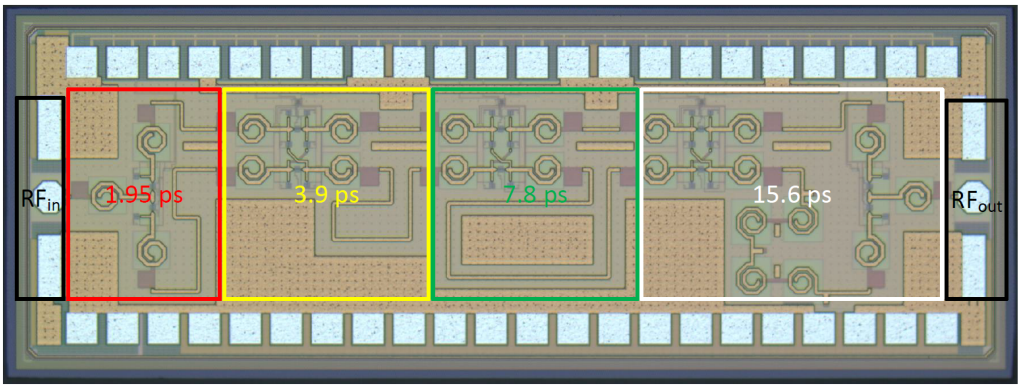
Figure 3.40 Schematic of the attenuator.

3.8 True Time Delay

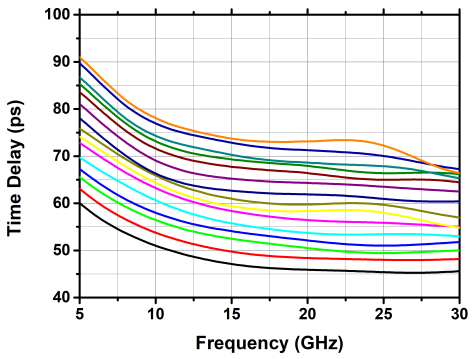
TTD is implemented in two separate chips. First block contains the first four bits. Fig. 3.41(a) and (b) shows the schematic and the micrograph of this design. First three bits are implemented with transmission lines and fourth bit employed ATLs. Unit cell is an ATL composed of two shunt 80 fF capacitors and a 220 pH series inductor which has a delay of 4.2 ps. Bits are connected using double-pole double-throw (DPDT) switches and there are SPDTs in the input and output. Fig. 3.41(c) shows the simulated time delays and the maximum difference is 29.5 ps. IL is around 10 dB and is not increasing dramatically as shown in Fig. 3.41(d).



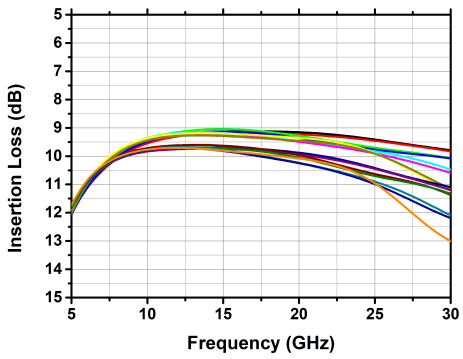
(a)



(b)



(c)

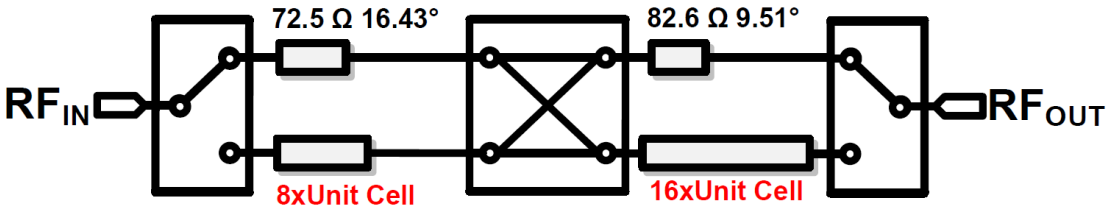


(d)

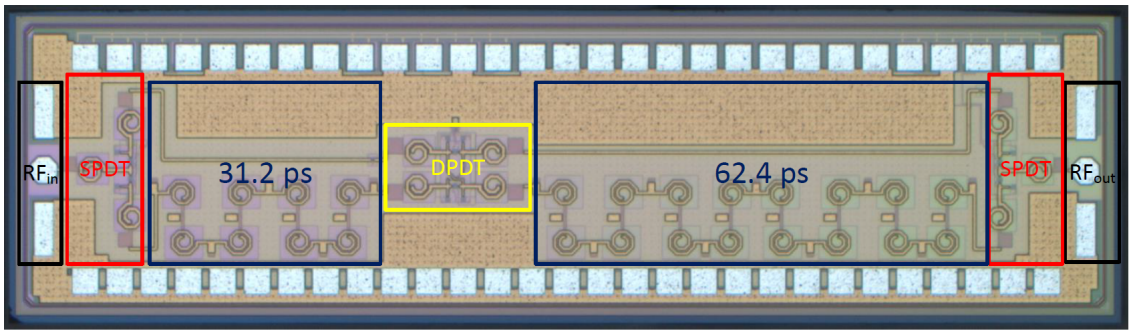
Figure 3.41 (a) Schematic, (b) micrograph, (c) simulated delay and (d) simulated IL of the first TTD block (Kana, 2022).

The second TTD block contains two higher delay bits, 31.2 ps, and 62.4 ps. ATLs are used with the same unit cell, and the schematic and micrograph are given in Fig. 3.42. The chip is measured, and the delay and IL results are shown in Fig. 3.42(c) and (d). Other than 62.4 ps bit, delays are as expected, but the 62.4 ps state is not working as it was simulated, and the reason is being investigated.

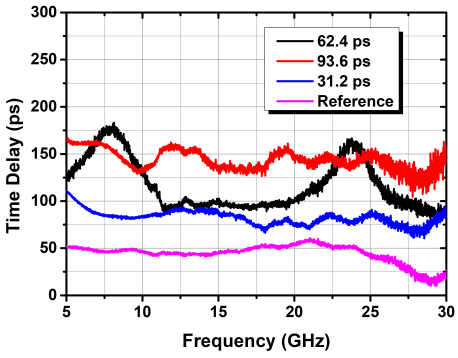
Except for the 62.4 ps delay state, the TTD is working correctly. The core area of the first and second blocks are 0.96 mm^2 and 1.42 mm^2, respectively. Insertion losses are higher than the simulated results, but this is mainly due to DPDT losses. Measurements are still in process, and more details on the TTD, DPDT, and SPDT can be found in the thesis of my colleague, Cengizhan Kana (Kana, 2022).



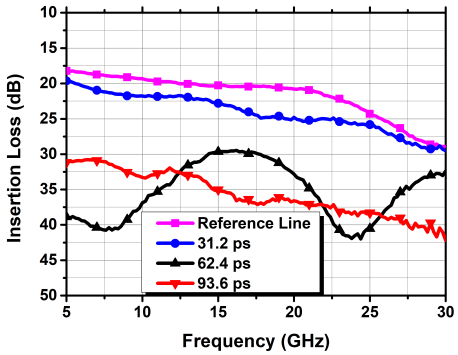
(a)



(b)



(c)



(d)

Figure 3.42 (a) Schematic, (b) micrograph, (c) measured delay and (d) measured IL of the second TTD block (Kana, 2022).

4. CONCLUSION

For next-generation phased array applications, thousands of transceiver modules are used. The area and cost of the transceiver module are as crucial as the system's performance because of the vast scale of phased arrays. The technology and architecture of the module are critical, and it defines the specifications of the sub-blocks. Various sub-blocks are used in a phased array transceiver, such as LNA, PA, SPDT, VGA, attenuator, phase shifter, and TTD. Each sub-block has a vital role to play and comes with its challenges.

First, a novel technique is presented in this thesis to reduce the amplitude and phase errors in current steering VGAs. The reason for the high phase errors in current steering VGAs is analyzed, and a technique is proposed to compensate for it. This technique is implemented in a wideband VGA and can be utilized in unidirectional transceiver architectures to control the amplitude of the signal with minimum error and high resolution. Also, low phase error, power consumption, and NF are achieved in a small chip area.

Second, a bidirectional transceiver module operating between 8 to 28 GHz is presented. The module consists of a bidirectional common chain and an RF front-end circuit. The common chain contains a TTD, attenuator, and BDA to control the amplitude and time delay of the system. The RF front-end contains a PA, LNA, and SPDT switch to transmit with high power and receive with low NF. The design and implementation of each block are given, and the combined front-end is also presented. Each sub-block has comparable or better performance with the state-of-the-art works in the literature. Table 4.1 summarizes the performance of each block. The specification is also included in parenthesis in addition to the achieved performance metric.

Table 4.1 Performance Summary (Specifications) of the Sub-Blocks for the Transceiver Module

	BDA	TTD	ATT	LNA	PA	SPDT
Gain(dB)	7.5(10)	-29(-20)	-5.8(-10)	27(20)	19.5(20)	-1.6 (-2)
OP_{1dB}(dBm)	-0.5(-2)	-	13*(-)	7(5)	15.2(15)	16.1*(0)
NF(dB)	9(10)	29(20)	5.8(10)	3(3)	-	1.6(2)
P_{DC}(mW)	13(25)	0(0)	3(0)	56(50)	171(200)	1.4(0)
Area(mm^2)	0.14(0.25)	2.4(2.5)	≈0.2(1)	0.3(0.5)	0.4(1)	0.1(0.1)
Amp. Er.(dB)	-	- (0.5)	0.25(0.5)	-	-	-
Delay Er.(ps)	-	- (1.9)	0.5(1.9)	-	-	-

*IP_{1dB}.

4.1 Future Work

For the bidirectional transceiver module, the measurement of the BDA and the TTD will be continued in the short term. The DC block capacitors will be added to the attenuator, and the design will be submitted to the next tape-out. In the long term, TTD and BDA designs can be improved if the required performance is not achieved during measurements. After the chip is manufactured, the RF front-end will be measured, and the performance will be verified. After acquiring the expected measurement results, the common chain and front-end will be combined into the transceiver module.

Further improvements to the VGA can also be made. An on-chip DAC can be implemented to control the amplitude digitally, allowing easier operation in a transceiver system.

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APPENDIX A

List of Publications

During my Master's studies, I was the author and co-author of two conference papers. Moreover, we already re-submitted two journal papers for review. You can find the list of publications in Sabanci University with SUMER group under the supervision of Prof. Yaşar GÜRBÜZ below.

A. Burak, K. Altintas, M. Yazici and Y. Gurbuz, "LNA Designs for 5G Receiver Applications," 2021 IEEE Asia-Pacific Microwave Conference (APMC), 2021, pp. 10-12, doi: 10.1109/APMC52720.2021.9661791.

K. Altintas, T. A. Ozkan, M. Yazici, M. Kaynak and Y. Gurbuz, "A 8-18 GHz Low Noise Variable Gain Amplifier with 30 dB Gain Control Range," 2022 17th European Microwave Integrated Circuits Conference (EuMIC), 2022. (Paper presentation is on 27.09.2022.)

K. Altintas, A. Burak, M. Yazici and Y. Gurbuz, "A Low Noise Variable Gain Amplifier with Low Phase Error for X-Ku-Band Phased Arrays" (Submitted to IEEE Transactions on Microwave Theory and Techniques)

K. Altintas, A. Burak, M. Yazici, M. Kaynak and Y. Gurbuz, "A Wideband Compact Distributed Power Amplifier with 33.5% Peak Power Added Efficiency" (Submitted to IEEE Microwave and Wireless Component Letters)