A 4-bit CMOS Phase Shifter Using Distributed Active Switches

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***Abstract*—This paper presents a novel 4-bit phase shifter using distributed active switches in 0.18-μm RF CMOS technology. The relative phase shift, which varies from 0° to 360° in steps of 22.5°, is achieved with a 3-bit distributed phase shifter and a 180° high-pass/low-pass phase shifter. The distributed phase shifter is implemented using distributed active switches that consist of a periodic placement of series inductors and cascode transistors, thereby obtaining linear phase shift versus frequency with a digital control. The design guideline of the distributed phase shifter is presented. The 4-bit phase shifter achieves 3.5±0.5 dB of gain, with an rms phase error of 2.6° at a center frequency of 12.1 GHz. The input and output return losses are less than −15 dB at all conditions. The chip size is 1880 μm × 915 μm including the probing pads.**

***Index Terms*—CMOS, distributed phase shifter, phase shifters, phased arrays, satellite communications.**

I. Introduction

MICROWAVE AND millimeter-wave phase shifters are essential components in a phased-array system for scanning of the radiated beam in minimal time [1]. Most of the RF phase shifters have been implemented in GaAs technology, but recently Si-based phase shifters have been extensively studied for low-cost and small-size phased-array systems.

Several design topologies using standard silicon technology have been demonstrated to realize both digital and analog monolithic microwave integrated circuit (MMIC) phase shifters. A 6-bit p-i-n diode phase shifter was realized in a silicon germanium bipolar technology [2]. Additionally, a 5-bit digital phase shifter using a MOS switch was developed over a 9–15-GHz frequency band [3]. These two digital phase shifters exhibit a high insertion loss and large chip area due to the cascade of several phase bits. In contrast, in analog phase shifters, the differential phase shift is varied in a continuous manner by the capacitance change of a varactor or by the vector sum using active devices.

A dual-band phase shifter using two variable gain amplifiers was reported for a smart antenna transceiver [4]. In order to cover the full range of 0°–360°, the phase shifter consists of a cascade of four identical phase shifters with a 90° phase range. Two K-band active phase shifters using the vector sum of orthogonal signals were recently reported in 0.18-μm CMOS technology [5]; however, using passive couplers and baluns in a bulk silicon substrate, the phase shifters have high insertion losses despite the fact that the variable gain amplifiers provide gains.

Analog phase shifters can be implemented using a varactor-loaded transmission line in which the transmission line is synthesized with lumped inductors [6]. They have been demonstrated using microelectromechanical systems (MEMS) varactors or thin-film ferroelectric barium strontium titanate (BST) [7], [8]. An 180° continuous analog phase shifter using varactors that implement a constant-impedance technique was proposed in SiGe [9]. A multiband phase shifter was designed by employing a distributed amplifier between varactor-tuned *LC* networks for active loss compensation [10]. The low quality factor of varactors and inductors in CMOS results in large insertion losses and loss variations of the conventional distributed phase shifters.

In this paper, we present a novel digital phase shifter using distributed active switches. The phase shifter consists of an 180° high-pass/low-pass phase shifter and a 3-bit distributed phase shifter, which utilizes a distributed amplifier technique. The artificial transmission line consists of a ladder network of series inductance and gate capacitance of active switches; in this manner, it becomes a constant-k transmission line. The differential phase shift, which is the phase shift between active switches along the gate line, can be obtained by selecting one of the active switches in parallel. A cascode MOSFET is used in a distributed active switch, yielding a significant improvement in gain and gain variation performances. The gain variation can be minimized by adjusting the transconductance of each active switch. All microstrip lines with the first metal ground are simulated using ADS Momentum for planar electromagnetic simulations to take into account the coupling between adjacent microstrip lines. The proposed novel 4-bit phase shifter exhibits low phase and gain variations with a relatively low level of power consumption.

II. Analysis

A. Artificial Transmission Lines

A transmission line can be modeled as a distributed network circuit consisting of inductors, capacitors, and resistors. In a lossless line, transmission lines have been traditionally modeled with the equivalent circuit shown in Fig. 1. The artificial transmission line exhibits a low-pass filter behavior with an equivalent line impedance Z_c given by [11]

$$Z_c = \sqrt{\frac{L}{C}}\sqrt{1-\frac{\omega^2 LC}{4}} = \sqrt{\frac{L}{C}}\sqrt{1-\frac{\omega^2}{\omega_B^2}}. \qquad (1)$$

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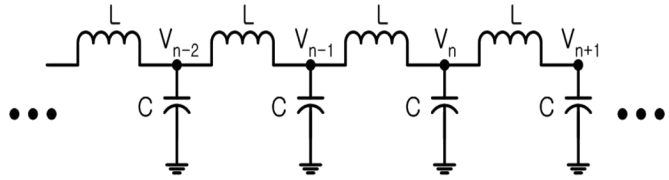


Fig. 1. Ideal artificial transmission line.

where ω is the operation frequency and ω_B is the Bragg frequency given by [12]

$$\omega_B = \frac{2}{\sqrt{LC}}. \tag{2}$$

At a sufficiently low frequency, the characteristic impedance is real and a signal power can be propagated along the line from a matched generator to a matched load. However, as the frequency increases above the Bragg frequency, the line impedance is imaginary, and no power can be delivered to the line. At frequency ω, waves propagate according to [13]

$$V_n = V_{n-1}e^{-\gamma_T} = V_{n-1}e^{-(\alpha+j\beta)}. \tag{3}$$

where γ_T is a complex propagation constant, which is a function of the frequency. α is an attenuation constant and β is a phase constant.

In the case of a lossless line, the per-section phase shift $\Delta\phi$ of the artificial transmission line is equal to the phase constant and can be derived as in [12]

$$\Delta\phi = \cos^{-1}\left(1 - \frac{2\omega^2}{\omega_B^2}\right) \approx \omega\sqrt{LC}\left(1 + \frac{\omega^2}{6\omega_B^2} + \cdots\right). \tag{4}$$

At frequencies well below the Bragg frequency, the characteristic impedance and per-section phase shift are

$$\begin{aligned} Z_c &\approx \sqrt{L/C} \\ \Delta\phi &\approx \omega\sqrt{LC}. \end{aligned} \tag{5}$$

A conventional distributed analog phase shifter has been developed by changing the shunt capacitance [14]. By applying a single bias voltage to either varactors or MEMS bridges, the effective distributed capacitance of the artificial transmission line can be changed, which, in turn, changes the phase velocity, and thus, the associated time delay through the line. However, there is tradeoff between the bandwidth and phase tuning range in the number of T-section networks. Hence, by tailoring the voltage across each capacitor separately, the desired phase shift can be achieved with good impedance-matching performances.

B. Digital Distributed Phase Shifter

Fig. 2 shows the proposed phase-shifter topology using distributed active switches. The operation of the phase shifter is very similar to that of a traveling-wave amplifier. However, the circuit is associated with only one input artificial transmission line, unlike a conventional traveling-wave amplifier, which consists of input and output lines. The input line consists of a cascaded ladder network with series inductances and shunt capacitances. The shunt capacitors of the gate line are supplied by the

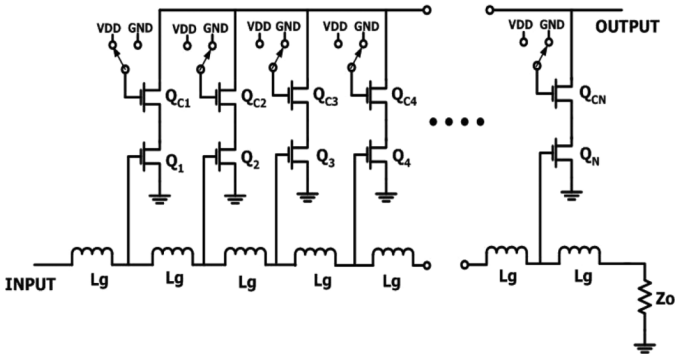


Fig. 2. Proposed circuit topology using distributed active switches.

gate capacitance $C_{\rm gs}$ of common source MOSFETs. The capacitance of transistors is related with the per-section phase shift and bandwidth. A low gate capacitance of transistors results in the high Bragg frequency and the low per-section phase shift. It is beneficial to design high-frequency phase shifters as long as the f_T of transistors is sufficiently high. A cascode design is chosen for the individual gain cells of the phase shifter. The cascode arrangement of two MOSFETs provides high gain, high output resistance, and high reverse isolation. In addition, the cascode MOSFET operates as active switch, as the gate bias of the common gate MOSFET can be used as an effective means of switching between VDD and GND. This enables the distributed phase shifter to be controlled digitally.

The input signal propagates through the gate line, tapping off some of the input power before being absorbed by a terminating resistor. The input signal sampled by the gate circuits at different phases is transferred to the output through each activated cascode cell. By switching the common gate MOSFETs in succession, the phase shift can be incremented by the steps of the phase constant of the input artificial transmission line. Therefore, the smallest phase shift is the unit phase shift of $\Delta\phi$ and the largest phase shift is $(N-1)\Delta\phi$.

An important parameter in phase shifters is the rms phase-shift error. Most MMIC phase shifters exhibit a phase shift error due to manufacturing process variations and modeling inaccuracies of the circuit elements. For the proposed distributed phase shifter, the transistor capacitance variation $C'_{\rm gs}$ or the series inductance variation L'_g results in the unit phase variation $\Delta\phi'$. The rms phase error $S_{\rm rms}$ can be obtained in terms of the unit phase mismatch $\Delta\phi_{\rm err} = |\Delta\phi - \Delta\phi'|$. It can be computed as

$$\begin{aligned} S_{\rm rms} &= \sqrt{\frac{(\Delta\phi_{\rm err})^2 + (2\Delta\phi_{\rm err})^2 + \cdots ((N-1)\Delta\phi_{\rm err})^2}{N-1}} \\ &= \sqrt{\frac{N(2N-1)}{6}}\Delta\phi_{\rm err}. \end{aligned} \tag{6}$$

In addition, the unit phase mismatch can be a function of the number of stages N needed for a required phase shift range. For a given gate capacitance or series inductance variation α, which is defined as $C'_{\rm gs}/C_{\rm gs}$ or L'_g/L_g, the unit phase mismatch can be expressed by

$$\Delta\phi_{\rm err} = \frac{\phi_{\max}}{N-1}|1 - \sqrt{\alpha}| \tag{7}$$

where $\phi_{\max}$ is the maximum differential phase shift.

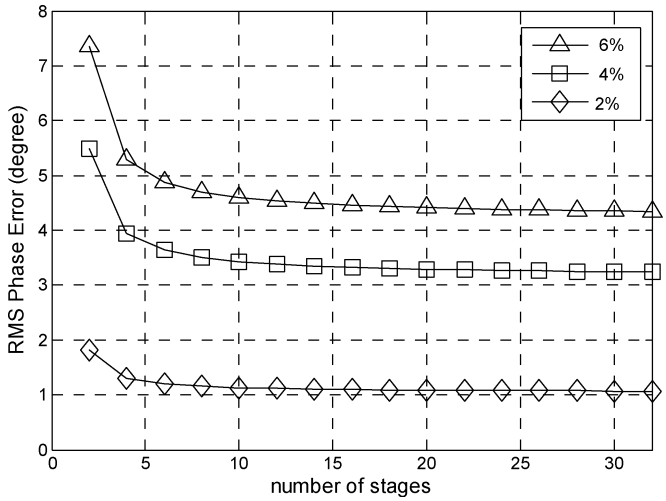


Fig. 3. Calculated rms phase error versus the number of stages as the gate capacitance or series inductance varies.

Using (6) and (7), the rms phase error can be calculated as

$$S_{\rm rms} = \sqrt{\frac{N(2N-1)}{6}}\frac{|1-\sqrt{\alpha}|\phi_{\max}}{N-1}. \tag{8}$$

Fig. 3 shows the calculated rms phase error with the gate capacitance or series inductance variation for a maximum differential phase shift of 180°. The rms phase error is not reduced significantly when more than eight sections are used.

Another important parameter of the phase shifter is the state-to-state variation of the insertion loss or gain. In practice, the gate voltage wave traveling throughout the gate artificial line will unequally excite the gates of common source MOSFETs due to the loss present in the gate artificial transmission line. Each successive common source MOSFET receives less signal voltage as the signal travels down the gate line. Hence, the current generators from the drains have different magnitudes. This results in a significant gain variation of the phase shifter. In order to equalize the current generators, it is necessary to change the transconductance of each cascode cell by adjusting the size of the common gate MOSFET. The magnitude of each current generator decreases as the differential phase shift increases, thereby increasing the size of the common gate MOSFET.

Fig. 4(a) shows a simplified equivalent circuit for the gate line of the distributed phase shifter. The input voltage wave propagating the gate line produces voltages $V_1, V_2, V_3, \ldots, V_n$ across each gate capacitance $C_{\rm gs}$. The voltage at the kth tap of the gate line is related to the gate line's segment length ℓ_g and complex propagation constant γ_g. If the voltage across the input terminal of the distributed phase shifter is $V_{\rm in}$, then

$$V_1 = V_{\rm in}e^{-\gamma_g\ell_g}, V_2 = V_{\rm in}e^{-2\gamma_g\ell_g}, \ldots, V_n = V_{\rm in}e^{-n\gamma_g\ell_g}. \tag{9}$$

Fig. 4(b) shows a simplified small-signal equivalent circuit of a single cascode unit cell. The current generator of each cascode cell can be expressed as

$$I_{o,1} = G_{m,1}V_1, I_{o,2} = G_{m,2}V_2, \ldots, I_{o,n} = G_{m,n}V_n \tag{10}$$

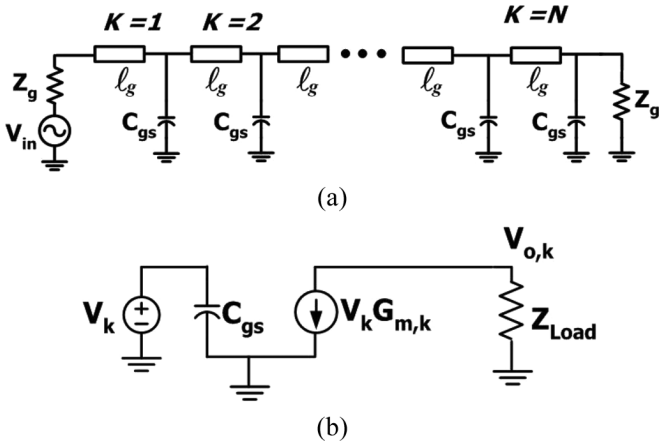


Fig. 4. (a) Transmission line circuit for the gate of the distributed phase shifter. (b) Simplified small-signal equivalent circuit of a single cascode cell.

where $G_{m,k}$ is the effective small-signal transconductance of each cascode cell.

The available gain of each phase state is given by

$$\begin{aligned} G_k &= \frac{\frac{1}{2}|I_{o,k}|^2 Z_{\rm Load}}{\frac{1}{2}|V_{\rm in}|^2/Z_g} \\ &= |e^{-k\gamma_g\ell_g}|^2 G_{m,k}^2 Z_{\rm Load} Z_g \\ &= e^{-2k\alpha_g\ell_g} G_{m,k}^2 Z_{\rm Load} Z_g \end{aligned} \tag{11}$$

where $\gamma_g = \alpha_g + j\beta_g$, in which α_g and β_g are the attenuation and phase constant of the gate line, respectively.

The following general condition for the amplitude equalization of the distributed phase shifter is then obtained:

$$\begin{aligned} G_{m,2} &= e^{\alpha_g\ell_g} G_{m,1} \\ G_{m,3} &= e^{2\alpha_g\ell_g} G_{m,1} \\ &\vdots \\ G_{m,k} &= e^{(k-1)\alpha_g\ell_g} G_{m,1}. \end{aligned} \tag{12}$$

In general, the transconductance of an MOSFET is directly proportional to the width-to-length ratio. The effective transconductance of a cascode cell can be changed by varying the size of common gate MOSFET. Hence, the width of the common gate MOSFET is given by

$$\begin{aligned} W_{c,2} &= e^{\alpha_g\ell_g} W_{c,1} \\ W_{c,3} &= e^{2\alpha_g\ell_g} W_{c,1} \\ &\vdots \\ W_{c,k} &= e^{(k-1)\alpha_g\ell_g} W_{c,1}. \end{aligned} \tag{13}$$

Equation (13) indicates that the width of a common gate MOSFET increases as an exponential function of the attenuation constant assuming that other parasitic losses are not considered. This is explained by the fact that the input voltage on the gate line decays exponentially.

Process variation can affect the gain of the distributed phase shifter. If the transconductance of each cascode cell is changed at the same ratio by the process variation, there is no change of

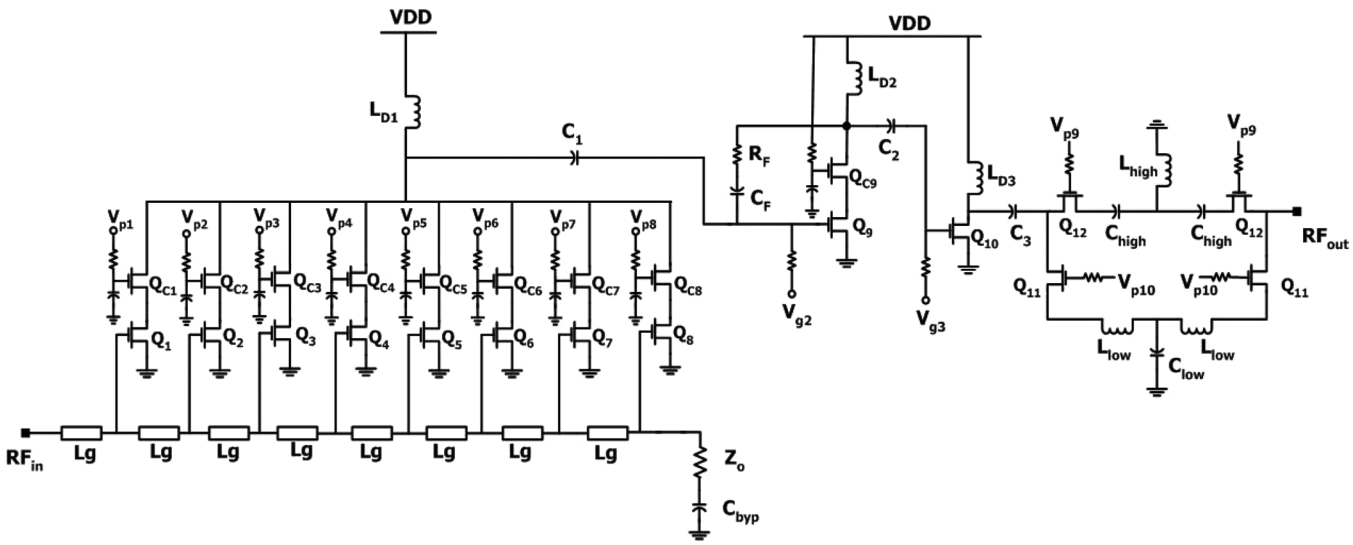


Fig. 5. Schematic of the 4-bit CMOS phase shifter using distributed active switches.

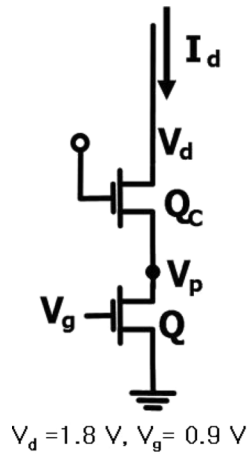
the gain deviation from (11) and (12). The absolute gain value of each phase state can be higher or lower.

III. Circuit Design

The proposed 4-bit phase shifter consists of a 3-bit distributed phase shifter, a feedback amplifier, and an 180° high-pass/low-pass phase shifter, as shown in Fig. 5. The 3-bit distributed phase shifter, in which eight cascode cells are connected in parallel, ranges from 0° to 157.5° in steps of 22.5°. The basic design of the distributed phase shifter can be carried out easily using (5). For a 50-Ω port impedance and a center frequency of 12 GHz, $C_{\rm gs}$ and L_g were determined as 0.104 pF and 0.26 nH, respectively. A common source MOSFET with a 45-μm gatewidth was selected, which corresponds to an input gate capacitance of 0.104 pF. The Bragg frequency can be calculated to be approximately 62.4 GHz. The size of the common gate MOSFET was increased from 19 to 50 μm in order to minimize the gain deviations of each phase state. It was designed with different size from 19, 20, 25, 30, 32, 33, 37, and 50 μm, respectively. The size was slightly optimized due to other parasitic components and the losses of the connecting lines at the output of the each cascode cell.

The 4-bit phase shifter was designed at 12 GHz for a satellite phased-array system. Hence, the output of the distributed phase shifter is loaded with a high-pass combination of L_{D1} and C_1 to provide parallel resonance, thereby increasing the gain at the design frequency. The connecting lines of the distributed phase shifter are negligible for the phase performance and bandwidth because the phase performance is mainly dependent on the input artificial transmission line and the output load affects the bandwidth. The connecting lines can have an influence on changing the loss of each state.

Fig. 6 shows the simulated operation conditions of a 3-bit distributed phase shifter. Sizing up the common gate MOSFET increases the drain voltage (V_p) of the common source MOSFET, thereby increasing the drain current. This results in varying the effective transconductance of the each cascode cell.



	V_p (V)	I_d (mA)
State1	0.58	5.7
State2	0.6	5.73
State3	0.7	5.85
State4	0.77	5.93
State5	0.8	5.95
State6	0.8	5.95
State7	0.85	6
State8	0.93	6.06

Fig. 6. Operation conditions of 3-bit distributed phase shifter.

A two-stage amplifier followed by the distributed phase shifter is used to flatten the gain over a wider bandwidth of frequencies. The second stage is realized as a cascode amplifier with resistive shunt feedback. Resistor R_F forms the feedback, and C_F is used for independent biasing of the gate and drain. The capacitance of C_F is normally large in order to function as a short circuit over the frequency of interest. The resistive feedback provides better stability, gain flatness, and bandwidth. The inter-stage matching network is a high-pass combination of L_{D2} and C_2 in order to obtain conjugate matching between the drain of Q_{C9} and the gate of Q_{10}.

The third stage is a common source amplifier used to enhance the overall gain. The output of the third stage is loaded with a shunt inductor L_{D3} and a series capacitor C_3. This impedance matching network improves the output return loss of the amplifier stage, thereby minimizing the interactions between the output of the third stage and the input of the 180° phase shifter.

Fig. 7 shows the simulated gain responses of sub-circuits. The losses of the distributed phase shifter are approximately −4 dB. The two-stage amplifier provides 13–14-dB gain over a frequency range. The overall gain of active circuits varies from

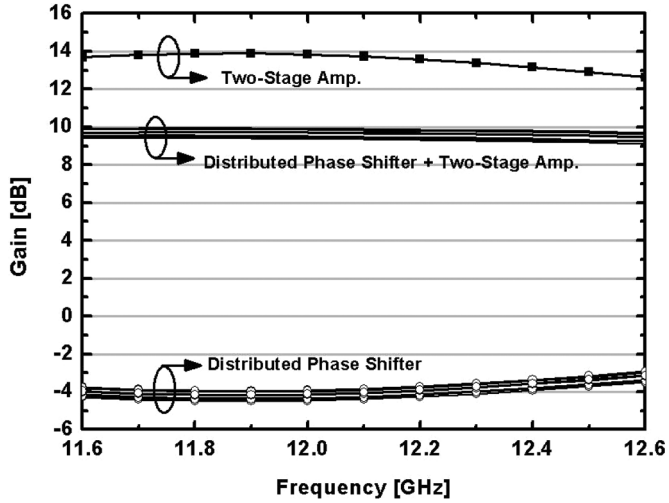


Fig. 7. Simulated gain responses of active sub-circuits.

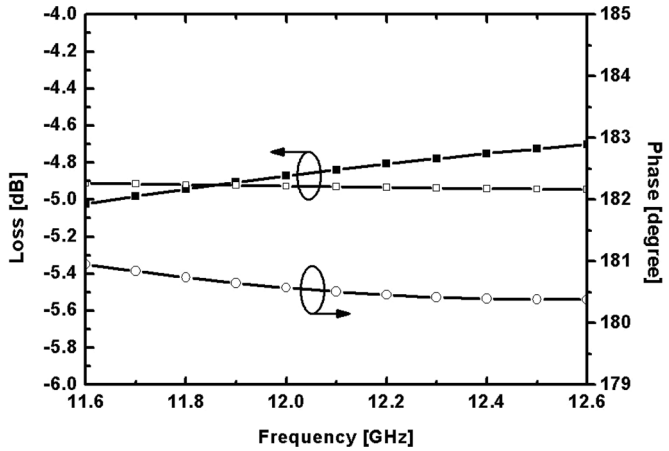


Fig. 8. Simulated losses and phase response of 180° phase shifter.

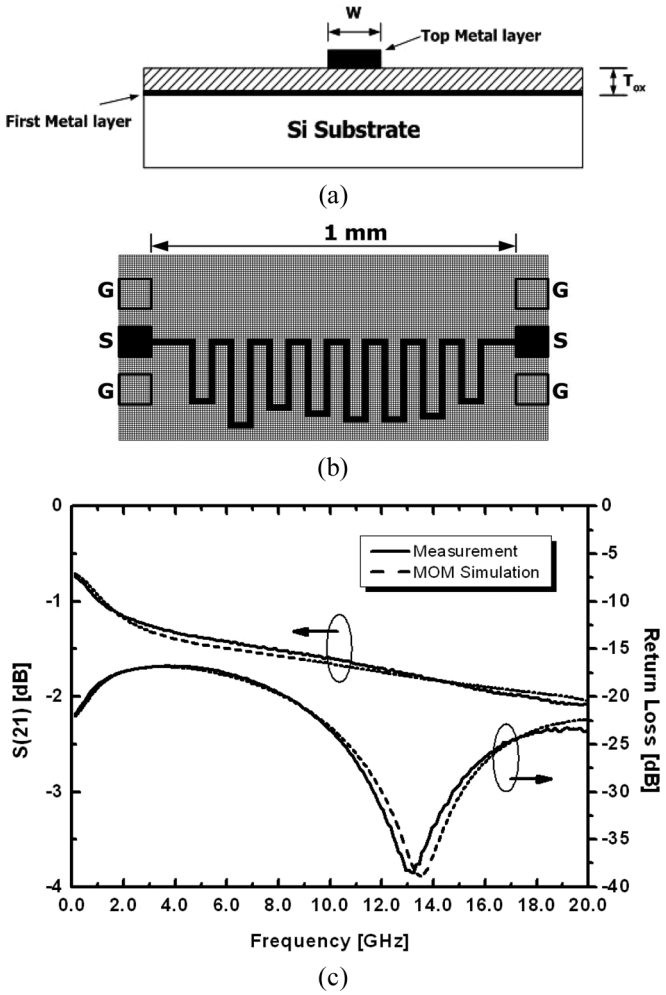


Fig. 9. (a) Cross-sectional view of a microstrip line. (b) Meandered microstrip line pattern. (c) Simulated and measured S-parameter results of the meandered line pattern.

9 to 10 dB for different phase conditions. The simulated input 1-dB compression point of the phase shifter is -8 dBm.

The 180° phase shifter switches a T-type high-pass/low-pass phase-shift network using two SPDT MOSFET switches [3]. The gatewidth of each switch is 40 μm. The on resistance and off capacitances are approximately 14 Ω and 0.03 pF, respectively. The isolation of the switch is approximately -14 dB at 12 GHz. It is designed to have a characteristic impedance of 50 Ω. A shunt capacitor $C_{\rm low}$ and a series capacitor $C_{\rm high}$ are implemented as metal–insulator–metal (MIM) capacitors. In both networks, the inductors are implemented using a microstrip line structure with a first metal ground plane because the relative phase shift of the 180° phase shifter is sensitive to the inductance value of the high- or low-pass filter. Fig. 8 shows the simulated insertion losses and phase difference of the 180° phase shifter. The insertion losses of the high- and low-pass state are better than -5 dB with an amplitude imbalance of within 0.3 dB and a phase error of within 1°.

Fig. 9(a) illustrates a typical microstrip configuration using CMOS technology. The microstrip line is realized through the use of the top metal as a signal line and the bottom metal as a ground with a thick SiO_2 layer as a substrate. The top metal and bottom metal are fabricated with 2- and 0.5-μm-thick Al metals, respectively. The metals are separated by an oxide layer approximately 6.5-μm thick. In the microstrip structure, most of the electric fields are confined in a silicon–oxide layer due to the ground-plane shielding. Thus, the loss associated with a silicon substrate can be reduced and the coupling effect with the adjacent signal line is minimized. For a compact circuit size, meandered microstrip lines are adopted for the distributed phase shifter and 180° phase bit. Moreover, all microstrip lines including interconnect effects are simulated by a full-wave EM simulator (ADS Momentum). The microstrip line has a simulated quality factor of approximately 5–6 at 12 GHz. Fig. 9(b) shows the meandered microstrip line test pattern that can form the artificial transmission line of the distributed phase shifter. After the momentum condition was verified by the test pattern at the first tape-out, we designed the 4-bit phase shifter at the second tape-out for accurate phase responses. The length of each section can be optimized to be in line with the linear phase response because of different electrical delay according to the different size of the common gate MOSFET in the cascode cell. The linewidth and spacing are 8 and 20 μm, respectively. The meandered line was measured using an on-wafer

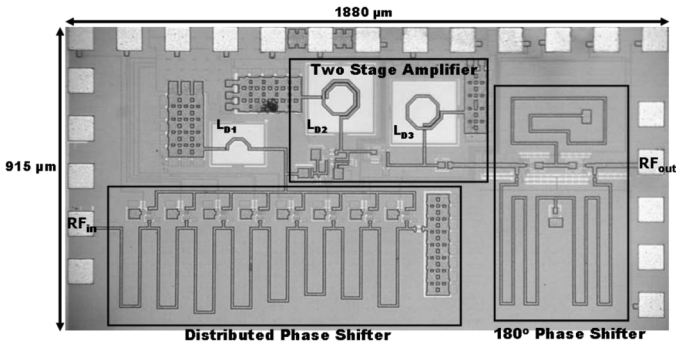


Fig. 10. Chip photograph of the fabricated phase shifter.

probing system. Fig. 9(c) shows the simulated and measured results of the standalone meandered microstrip line pattern. There is a good agreement between the simulation and measurement results.

IV. Measurement Results

The proposed 4-bit phase shifter was fabricated using TSMC's 0.18-μm CMOS technology, which provides one poly layer for the gate of the MOSFET and six metal layers for inter-connection. The active device models are based on standard BSIM3 model provided by TSMC. The circuit draws a maximum 14.8-mA dc current from a 1.8-V power supply; thus, the maximum power consumption is 26.6 mW. The 3-bit distributed phase shifter is biased at $V_g = 0.9$ V with the drain current varying from 5.7 to 6.0 mA. The power consumption of the 3-bit distributed phase shifter itself is 10.8 mW. The gate bias (V_{p1} to V_{p8}) of the common gate MOSFET is toggled between 0–1.8 V. In the two-stage amplifier, the bias voltages are chosen as $V_{g2} = 0.64$ V and $V_{g3} = 0.58$ V, resulting in dc currents of 5.2 and 3.6 mA for the second and third stages, respectively. The 180° phase shifter using passive MOSFET switches requires two control bias inputs of 0 and 1.8 V, but does not consume any current.

Fig. 10 shows a die photograph of the proposed 4-bit phase shifter. The chip size, including the pads, is 1880 μm $\times$ 915 μm. The phase shifter was measured using RF probes and a short-open-line-thru (SOLT) calibration up to the probe tips to measure the S-parameter. It was measured with an Agilent 8510C vector network analyzer and a Cascade Microtech probe station. Fig. 11 shows the measured relative phase shifts of 16 phases over 11.6–12.6 GHz. The relative phase shifts can be obtained by the phase difference of each transmission coefficient (S_{21}) between the phase and reference states. The phase shift at the designed center frequency of 12.1 GHz is incremented in the steps of 22.5°. A phase shift of 0°–157.5° is achieved with the 3-bit distributed phase shifter and, as expected, increases linearly with the frequency. These time-delay characteristics enable frequency-independent beam steering, which permits the realization of a wideband phased-array system. In the case of an 180° bit, the relative phase shift is constant and flat to within $\pm$0.5° over more than 2 GHz of bandwidth. Fig. 12 shows the measured gain responses for the 16 states. The overall gain of the phase shifter is measured to be 3.5$\pm$0.5 dB at 12.1 GHz. From 11.6 to 12.6 GHz, the gain varies by less then $\pm$0.5 dB.

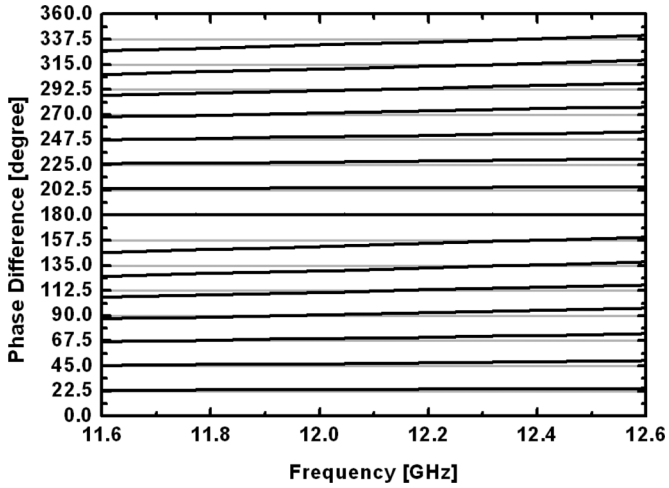


Fig. 11. Measured relative phase shift for all 16 states.

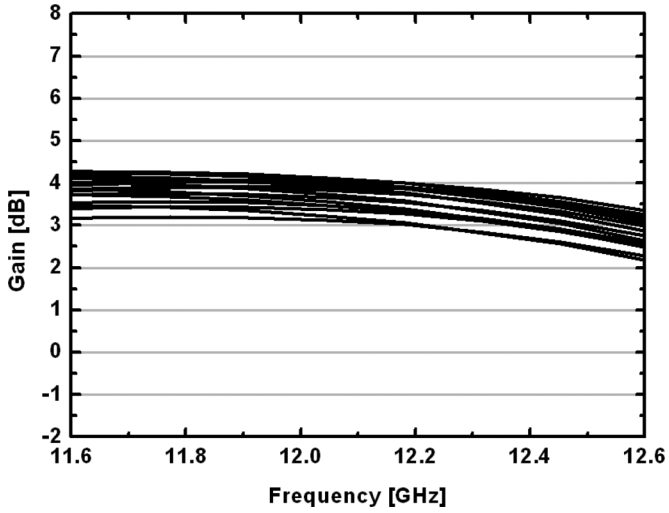
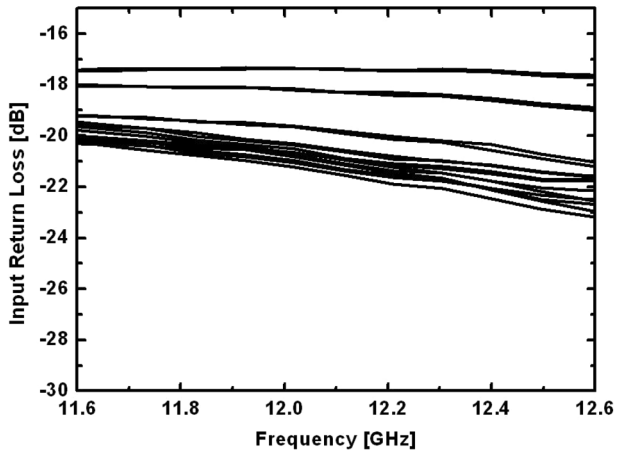
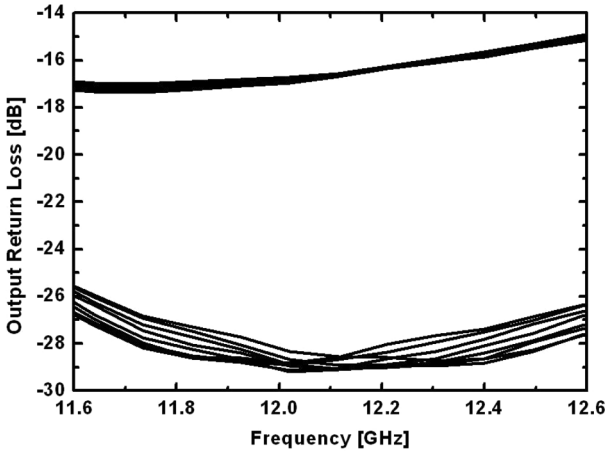


Fig. 12. Measured small-signal gain.

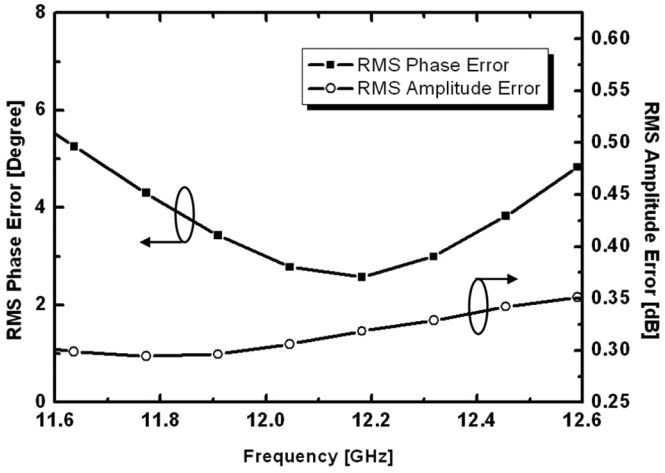
As designed, the distributed phase shifter and the two-stage amplifier provide 9–10-dB gain and the insertion loss of the 180° phase shifter is approximately 5 dB. Hence, the measured gain agrees well with the simulated value. The measured input and output return losses are plotted in Fig. 13(a) and (b), respectively. Both the input and output return losses are better than -15 dB over the band of interest. The output return loss exhibits different characteristics according to the control of the 180° phase shifter. These differences are due to impedance imbalance between the high- and the low-pass path. Due to the isolation of the amplifier, the input return loss is only related to the input artificial transmission line. Fig. 13(c) shows the measured rms phase and rms amplitude error. The rms of the phase error can be calculated from all measured phase shifts using (6). The phase shifter exhibits a maximum rms phase error of 5.5° and a maximum amplitude error of 0.35 dB with 1-GHz bandwidth. The rms phase error is minimized at 2.6° near the designed frequency of 12.1 GHz. The gain variation of the phase shifter can be more reduced by adaptively adjusting the gate bias (V_{g2}) of the shunt feedback amplifier. Fig. 14(a) shows the measured gain response after a gain calibration. It is found that the



(a)

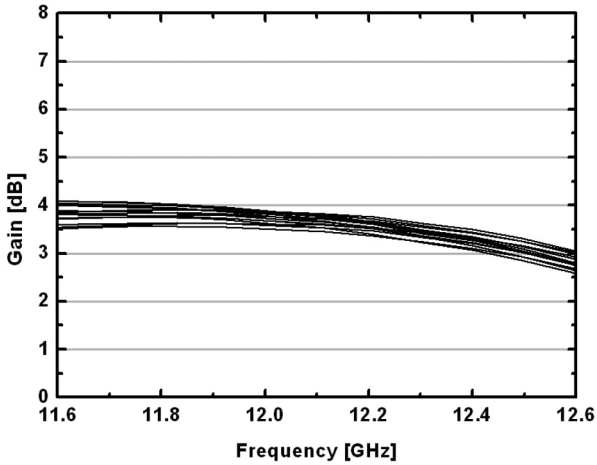


(b)

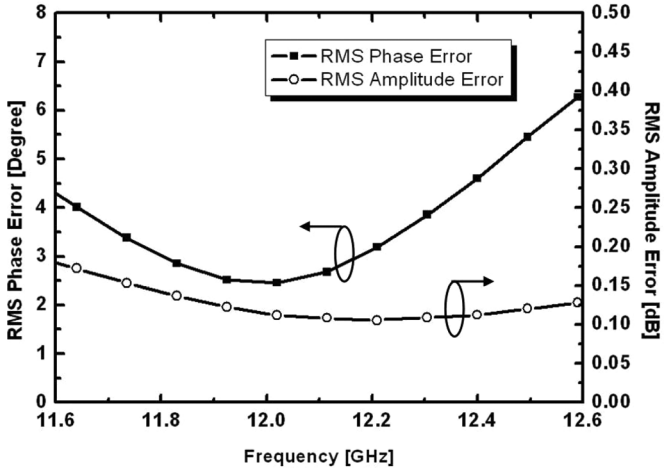


(c)

Fig. 13. (a) Measured input return loss. (b) Measured output return loss. (c) Measured rms phase and amplitude error.



(a)



(b)

Fig. 14. Measured results after gain calibration. (a) Small-signal gain. (b) rms phase and rms amplitude errors.

TABLE I
COMPARISON OF SILICON PHASE SHIFTERS

Process	Freq. (GHz)	Phase error (^{o})	Gain (dB)	Phase range	Area (mm^2)	DC Power (mW)	Ref.
SiGe p-i-n	8-11	N/A	-11	360^o (6-bit)	14.44	45	[2]
0.18 μm CMOS	11.7 - 12.8	7	-14	360^o (5-bit)	5.1	-	[3]
0.18 μm CMOS	15-20	0*	-5 ±5	360^o (analog)	0.72	>100#	[5]
SiGe HBT	11-12	18	3.7 ±1.2	360^o (analog)	1.5	50	[9]
0.18 μm CMOS	3.4-5.8	0*	-4.5 to 2.1	360^o (analog)	2.76	45	[10]
0.18 μm CMOS	11.6-12.6	5.5	3.5 ±0.5	360^o (4-bit)	1.7	26.6	This work

* Continuous phase shift.
# Estimated from VGA

gain ripple within the same bandwidth is less than ±0.25 dB. Hence, a maximum rms amplitude error of 0.19 dB is achieved, as shown in Fig. 14(b). On the other side, the rms phase error slightly changes by approximately 1° through the calibration process.

Table I compares the recently reported phase shifters in the silicon process. Switching-type phase shifters [2], [3] using passive switches exhibit large insertion loss and chip area because each sub-bit is cascaded for multibit operation. On the other hand, active phase shifters [5], [9], [10] show significant

state-to-state gain variation with analog control. This work operates with digital control and achieves lower gain deviation and lower power consumption with competitive gain and size compared to other active phase shifters.

V. Conclusion

This paper has presented the development of a 4-bit phase shifter in 0.18-μm CMOS technology. The phase shifter consists of a 3-bit distributed phase shifter, a two-stage amplifier, and a 180° high-pass/low-pass phase shifter. The novel 3-bit phase shifter provides a true time-delay phase shift through the use of a distributed active switch that is comprised of the periodic placement of a series inductor and a cascode MOSFET. The distributed approach operates digitally with a small chip area and a low gain variation compared to conventional distributed phase shifters. The two-stage amplifier exhibits a flat gain response over the frequency of interest. The 4-bit phase shifter has a measured gain of 3.5 ± 0.5 dB at 12.1 GHz with a dc power consumption of 26.6 mW. The input and output return losses are better than -15 dB, as the artificial transmission line is on the input port and the high-pass/low-pass network is on the output port. The rms phase error is less than 5.5° over 1 GHz of bandwidth. The low phase deviation makes the phase shifter suitable for modern communication systems that require the phase flatness over an operating frequency band. In addition, the phase shifter can be used for a wideband phased-array system due to the time-delay nature of the distributed phase shifter.

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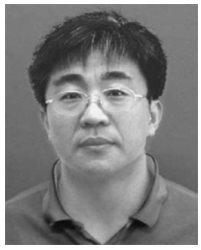

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