# FPGAs for Improved Energy Efficiency in Processor Based Systems

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**Abstract.** Processor based embedded systems often need to apply simple filter functions to input data. In this paper we examine the relative energy efficiency of microprocessor and Field Programmable Gate Array (FPGA) implementations of these functions. We show that considerable savings can be achieved by adding an FPGA to a microprocessor based systems and propose a strategy to reduce the impact of the excessive leakage energy overhead in low data rate applications.

## 1 Introduction

Processor based embedded systems are used to collect data in a wide range of applications. The first stage of processing this data is often the application of finite or infinite impulse response filters to remove noise and constrain the frequency range of the input [1]. Where the input data rate or the filter order is high, the use of reconfigurable logic such as Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) within processor based embedded systems is often justified on the basis of performance. There is a clear case for inclusion of such technologies in order to meet system design requirements where input data rates are higher than the processor can cope with on its own.

There are, however, many applications in which speed of operation is within reach of a microprocessor and reducing power consumption is the dominant design aim. In these applications, FPGAs and CPLDs are usually excluded from the system design as it is assumed that adding these components will increase power consumption. It is clear that the inclusion of one of these devices can allow the processor clock frequency to be reduced and we have investigated the trade-offs of including a programmable logic device within the system when power reduction for a fixed required performance level is the designers aim.

In this paper we show that the power savings achieved more than offset the power consumed by the gate array. We also examine the impact of the variation in the ratio of static to dynamic power consumption caused by increased leakage currents in deep sub-micron processes [2]. The results of this investigation are used to propose a strategy for maximising energy efficiency of filtering operations in low rate data systems making use of switched power supplies for memories and logic arrays. We show that increased configuration energy requirements in power switched FPGAs can be less than the reduction in leakage energy achieved by that power switching.

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## 2 Basis of Comparison

In order to compare processor and FPGA based filtering operations it is necessary to set clear criteria for the filtering operations. In this paper we consider a range of different filters sizes but all filters considered have both 16 bit data and coefficients. All filters are constructed using a number of identical second order stages. Each stage is generated on the FPGA using a fully parallel single cycle filter stage implementation. On the processor, a C implementation provided an almost identical design complexity making the two designs comparable in terms of the filter quality vs. designer effort. Table 1 compares the core filter code for the C and VHDL implementations. For the sake of clarity, sign extension and bit selection has been omitted from the VHDL code sample.

The tools used to convert the FIR filter code into an implementation were the freely available design tools published by the silicon vendor. In the case of the micro-controller this was the NEC V800 series evaluation kit compiler and in the case of the FPGA the tools used was Xilinx ISE.

The leakage energy is a significant issue as the devices considered range over a number of process technologies. For this reason, the current flow into both FPGAs and processors is measured when the clock speed for the device has been set to give exactly the sample rate required. This leads to a higher leakage overhead being associated with filtering operations at a low rate as leakage is not related to the clock frequency.

**Table 1.** A comparison of the core FIR filter code used on the processor and FPGA

| C | VHDL |
|---|---|
| `d_x[2] = d_x[1];`<br>`d_x[1] = d_x[0];`<br>`d_x[0] = x;`<br><br>`for(i=0 ; i<3 ; i++)`<br>`  y += b[i]*d_x[i];` | `if rising_edge(clk) then`<br>`  x (2) <= x (1);`<br>`  x (1) <= x (0);`<br>`  x (0) <= x_in;`<br>`  for i in 0 to 2 loop`<br>`  p(i) := x(i)*b(i);`<br>`  end loop;`<br>`  y <= p(0)+p(1)+p(2);`<br>`end if;` |

When comparing the energy and power values, it is necessary to allow for all the components in a minimum system. In the processor case, the power consumption is measured including the necessary memory and interface circuits as this represents a minimum usable system. In the case of the FPGA, external memories are not required so the only the total FPGA power is considered.