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Fabrication and characterization of silicon-on-insulator wafers

Taeyeong Kim[1] and Jungchul Lee[1*]

Abstract

Silicon-on-insulator (SOI) wafers offer significant advantages for both Integrated circuits (ICs) and microelectromechanical systems (MEMS) devices with their buried oxide layer improving electrical isolation and etch stop function. For past a few decades, various approaches have been investigated to make SOI wafers and they tend to exhibit strength and weakness. In this review, we aim to overview different manufacturing routes for SOI wafers with specific focus on advantages and inherent challenges. Then, we look into how SOI wafers are characterized for quality assessment and control. We also provide insights towards potential future directions of SOI technology to further accelerate ever-growing IC and MEMS industries.

Introduction

Silicon-on-insulator (SOI) wafer consists of a single-crystalline silicon, known as the device layer, positioned atop the insulating Buried OXide (BOX) layer (Fig. 1a). This structure effectively isolates the device layer from the bulk silicon, offering advantages that make SOI wafers particularly appealing for both mainstream and specialized applications. Firstly, SOI wafers enable lower parasitic device capacitance because of their isolation from the bulk silicon substrate. This isolation significantly contributes to reduced power consumption, a vital requirement in today's power-conscious technology environment. Secondly, the complete isolation of the n- and p-well devices in SOI wafers allows for the fabrication of higher speed devices while avoiding latch-up effects, a notable issue in conventional CMOS structures. Finally, the robust structure of SOI wafers offers radiation-hardening properties, making them particularly suitable for sensitive applications where radiation tolerance is paramount. Given these advantages, SOI technology has found broad applicability [1, 4–6]. Their low power consumption makes them highly attractive for portable electronic devices and power-sensitive applications, while their enhanced processing speeds are used in high-performance computing and telecommunication systems. The radiation-hardening characteristics of SOI wafers have made them a favored selection for their use in space technologies, nuclear research, and high-energy physics experiments. Moreover, the single-crystalline nature of the device layer on the BOX layer is facilitating the fabrication of optoelectronic and MEMS devices due to its etch stop (Fig. 1b) [2, 3, 7, 8]. In each case, the unique benefits of SOI wafers are utilized to fabricate more robust, efficient, and high-performing systems.

In this review, we aim to overview the fabrication technology of SOI wafers with their advantages and challenges. Then, we look into the structural, electrical characterization method of fabricated SOI wafers. We also offer insights into the future directions of SOI wafer technology.

Fabrication

SIMOX

Fabrication method and history

The Separation by IMplantation of OXygen (SIMOX) method, developed in the 1970s, introduced an approach for the fabrication of SOI wafers without bonding [14].

*Correspondence:
Jungchul Lee
jungchullee@kaist.ac.kr
[1] Department of Mechanical Engineering, Korea Advanced Institute of Science and Technology, 291 Daehak-ro, Daejeon 34141, Republic of Korea

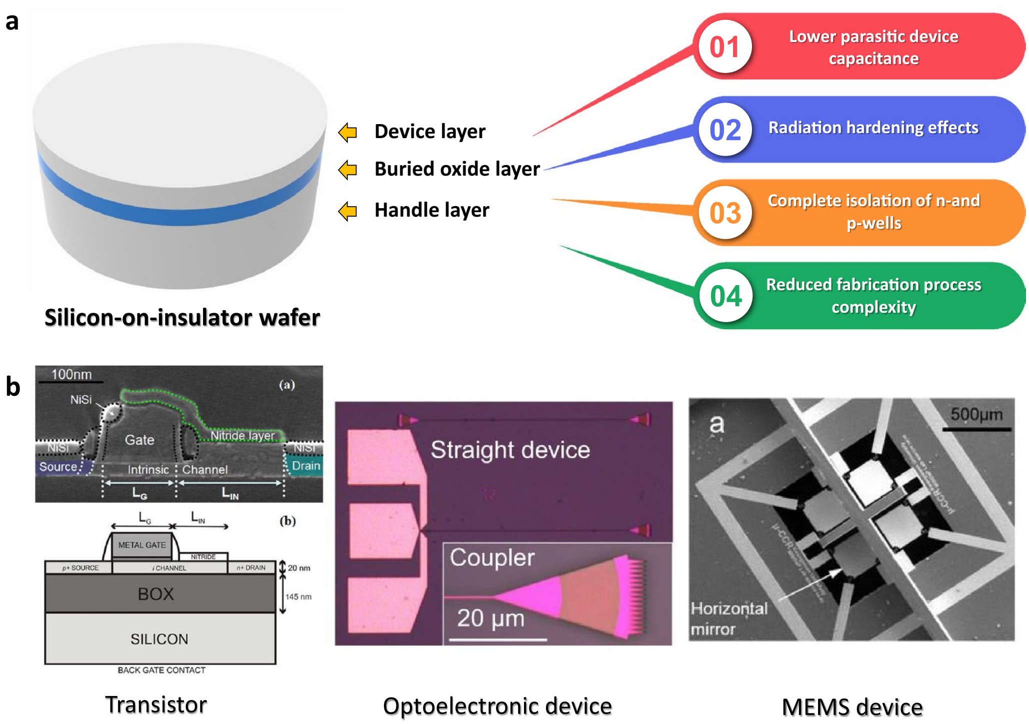

Fig. 1 **a** Schematic presentation of SOI wafer structure and its advantages. **b** Devices primarily fabricated using SOI wafers. (left) Reprinted from [1] with permission from AIP Publishing. (center) Reprinted from [2] (CC BY 4.0). (right) Reprinted from [3] (CC BY 2.0)

In the SIMOX process, a high dose of oxygen ions is implanted into a silicon wafer (Fig. 2a). This implantation stage is succeeded by a high-temperature annealing process, during which the implanted oxygen undergoes a chemical reaction with silicon to form a uniform layer of silicon dioxide (SiO_2) (Fig. 2b) [9, 15]. The resulting SiO_2 layer is embedded within the silicon substrate, giving rise to the characteristic SOI structure. This development provided a means to effectively control the thickness of the embedded insulator layer. Using this technology, SOI wafers can be fabricated up to a size of 300 mm.

In the early stages of SIMOX technology, achieving a 200 nm device layer atop a continuous, stoichiometric BOX layer of 400 nm required an ion energy of 200 keV and a dose of 2×10^{18} cm^{-2} [15]. This dose, however, significantly surpassed the quantities used in device fabrication, exceeding it by more than a hundredfold and thereby leading to the induction of defects within the crystalline lattice [16]. To preserve the crystallographic integrity at the surface—where the ion energy was at its highest—the ion implantation process was conducted at elevated temperatures, specifically above 500 °C [17]. This approach served to mitigate the onset of displacement damage. At the onset, threading dislocations permeating the device layer were observed to be at the level of 10^{10} cm^{-2} [18]. This value was effectively reduced to 10^6 cm^{-2} when ion implantation was carried out at 600 °C [16]. Post-implantation, a high-temperature annealing process was employed to form the BOX layer [19]. Theoretically, it is possible to eliminate internal precipitates at temperatures exceeding 1300 °C. Throughout the actual fabrication process, it was confirmed that an atomically sharp and planar interface could be realized between the device and BOX layers [20].

As the implantation dose increases, so does the process cost [21]. Therefore, modifications to ion implantation and annealing conditions have enabled the formation of the BOX layer at an order of magnitude lower dose than the initial 2×10^{18} cm^{-2}, specifically at 10^{17} cm^2 [15]. SOI wafers produced with this method generally have a BOX layer of less than 100 nm, with reports of achieving layers as thin as 56 nm [22]. The reduced implantation dose also helped decrease the defects caused by the ions. However, the presence of such thin BOX layers increased the probability of the formation of silicon pipes, which can create electrical shorts across the layer. Upon oxidizing the SOI wafer at higher than 1300 °C, some oxygen passes through the surface oxide and the device layer, reacting at the Si/SiO_2 interface [10, 23]. This process is referred to as Internal Thermal OXidation (ITOX) (Fig. 2c). Although this slightly increases the thickness of the BOX

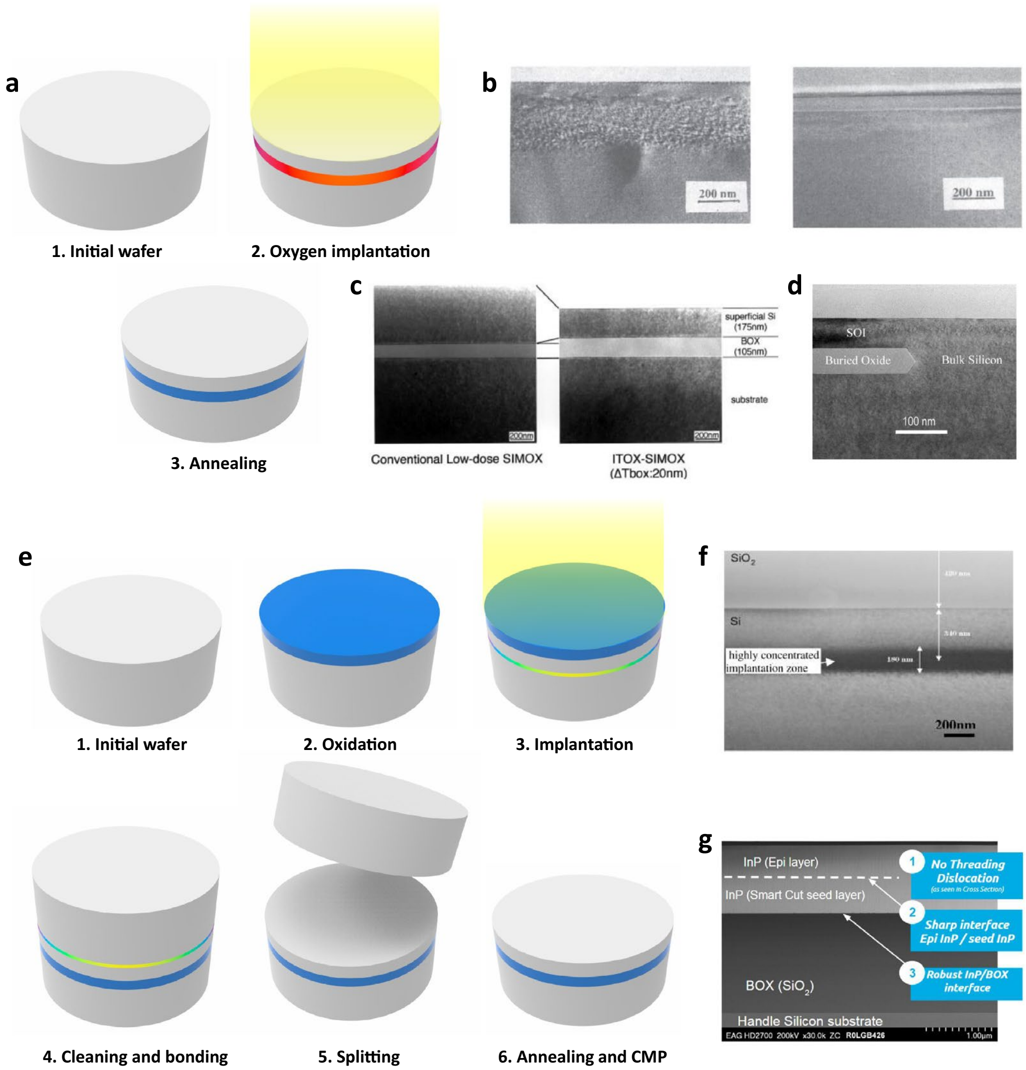

Fig. 2 **a** 3D schematic illustrating the fabrication of SOI wafers through the SIMOX technology. **b** Cross-sectional TEM images of (left) the as-implanted sample and (right) the annealed high-quality low-dose SIMOX with a 60 nm-thick buried oxide layer. Reprinted from [9] with permission from Springer Nature. **c** Cross-sectional TEM image of both conventional low-dose SIMOX and ITOX SIMOX wafers following the removal of the surface oxide layer. Reprinted from [10] with permission from Springer Nature. **d** Cross-sectional XTEM image of the annealed wafer partially subjected to an oxygen ions. Reprinted from [11] with permission from Elsevier. **e** 3D schematic illustrating the fabrication of SOI wafers through the Smart Cut™ technology. **f** Cross-sectional TEM image of the implanted zone. Reprinted from [12] with permission from Elsevier. **g** Cross-sectional TEM image of a 100 mm InP-on-silicon substrate after ~0.5 μm InP film overgrowth by MOCVD. Reprinted from [13] with permission from John Wiley and Sons

layer, it eliminates the silicon pipes, thus improving the stoichiometry of the BOX layer.

Advantages

A prominent merit of this method is the superior control it offers over the thickness of the buried oxide layer, facilitating the production of consistent and high-quality SOI wafers [9]. Another notable feature of the SIMOX process is its inherent simplicity [24]. It is primarily a three-step process: implantation, annealing, and polishing, with the dose of implantation offering a straightforward means to regulate the thickness of both the device layer and the BOX layer. This ability to adjust layer thickness by merely altering the implantation dose contributes significantly to the process's ease and flexibility. In addition to the thickness control, the SIMOX process allows the selective fabrication of oxide in specific areas via masking (Fig. 2d) [11, 25]. This capacity for localized oxide fabrication further emphasizes the versatility of SIMOX, enabling more complex device structures and broadening the range of potential applications.

Challenges

Despite its considerable advantages, the SIMOX technology does present certain challenges, particularly in the domains of cost and defect management. The necessity of high energy ion implantation equipment and an extended annealing process contribute to a higher cost of production compared to other SOI fabrication methods [21]. Moreover, ion implantation inevitably leads to lattice defects in the device layer, which cannot be reduced beyond a specific level [26]. This phenomenon can adversely impact the performance characteristics of the final device. Further complicating matters are the device layer's oxide precipitates and the silicon pipes in the BOX layer. These occurrences can prove detrimental during device fabrication. While certain mitigations, such as the use of an ITOX process, can somewhat alleviate these issues, advanced process refinement is required.

Smart Cut™

Fabrication method and history

The implantation of hydrogen ions at a dose higher than 5×10^6 cm^{-2} leads to the formation of microcavities within the silicon wafer [27]. Some of these hydrogen ions form dangling bonds with silicon, while the remainder inhabit the cavity interiors. During the annealing process, the pressure exerted by the segregation of hydrogen in its molecular form causes a thin silicon film to blister from the wafer [28]. Michel Bruel exploited these detrimental effects to control the thickness of the separated silicon films. To prevent blistering, a thick, rigid substrate was bonded to the surface of the wafer where the microcavities were formed through ion implantation. This procedure induced the microcavities, initially formed in a vertical orientation, to evolve laterally [29]. This innovative approach has been applied to the Smart Cut™ technology.

The Smart Cut™ technology is a layer transfer process that has significantly influenced the silicon wafer industry by facilitating the production of SOI wafers. The Smart Cut™ process proceeds through a series of steps: ion implantation, wafer bonding, layer splitting, and surface finishing (Fig. 2e) [30]. First, ions (typically hydrogen ions, but helium can also be used) are implanted into a single-crystal silicon donor wafer [31]. The ions are implanted at a specific depth, which determines the thickness of the layer to be transferred (Fig. 2f) [12, 32]. Next, the donor wafer is bonded to a handle wafer, which can be another silicon wafer. Often, an oxide layer is grown on one or both wafers before bonding, which results in an insulating layer in the final SOI structure. The bonded wafer pair then undergoes a thermal annealing process, which causes the implanted ions to form microbubbles and exert pressure on the surrounding silicon [33]. This results in a controlled fracture that effectively splits the donor wafer, transferring a thin layer of silicon onto the handle wafer. Finally, the transferred layer is polished to provide a smooth surface for subsequent device fabrication. Using this technology, SOI wafers can be fabricated up to a size of 300 mm.

In the case where the implantation dose falls below 3×10^{16} cm^{-2}, the hydrogen quantity is insufficient to induce the formation of lateral cracks within the voids [34]. As a result, these voids dissolve, and hydrogen diffuses away from the targeted region. Therefore, maintaining an implantation dose of no less than 3×10^{16} cm^{-2} is crucial to enable the silicon layer's splitting during the annealing. Ions of hydrogen or helium are typically favored for this process, owing to their minimal size and high mobility. Hydrogen is frequently used for this purpose due to its superior reactivity with the internal surface of the semiconductor [35]. Under identical implantation and annealing conditions, the dose needed for film separation is 2×10^{17} cm^{-2} for helium, substantially higher than the 6×10^{16} cm^{-2} required for hydrogen ions [36]. Another significant aspect in the Smart Cut™ process is the annealing temperature. Annealing is conducted in two steps. In the first step, annealing is done within a temperature range of 400–600 °C to split the single-crystal silicon layer. In the second step, annealing near 1100 °C is carried out to enhance the bonding strength [29].

Advantages

The Smart Cut™ technology enables unparalleled precision in controlling the thickness of the transferred silicon layer on the handle wafer, which can be controlled based on the energy of ion implantation. Additionally, by manipulating the oxidation time and polishing steps, the thickness of both the device layer and the BOX layer can be varied across a broad spectrum with high uniformity [37]. This technology permits the device layer thickness to range from as little as 4 nm to as much as 1.5 μm, and the BOX layer thickness can vary from 5 nm up to 5 μm [29, 38, 39]. Furthermore, the process's flexible design allows the utilization of high-quality seed wafers for the device layer, while less expensive, lower-quality wafers can be employed as handle wafers due to their supportive role. This not only provides a cost advantage but also a quality advantage. Adding to its economic benefits, the seed wafer can be reused in subsequent processes, reducing the overall material costs [40]. Moreover, the Smart Cut™ technology grants the ability to change the type of device layer (germanium, silicon carbide, indium phosphate etc.) and handle wafer (sapphire etc.), extending the versatility of this process (Fig. 2g) [13, 41–43]. This flexibility can be crucial when optimizing for different applications or device requirements, demonstrating another significant advantage of the Smart Cut™ method.

Challenges

Despite its significant advantages in fabrication, the Smart Cut™ process does have certain challenges that need to be addressed. For the Smart Cut™ process, the defect density has been minimized to a few per cm^2, but an optimized high-level technology is required to achieve a defect-free SOI wafer [44]. Another hurdle comes from the wafer bonding process. The bonding quality significantly influences the final product's performance. Surface cleanliness, flatness, and roughness of both the donor and handle wafers must be controlled meticulously, as any imperfections can lead to incomplete bonding, causing defects or voids in the final SOI structure [45]. In addition, the Smart Cut™ process involves several complex steps, each of which requires specialized equipment and careful control of process parameters. This can make the process expensive and time-consuming, particularly for large-scale manufacturing. Each step adds complexity and requires precise control to ensure a high-quality final product.

Eltran®

Fabrication method and history

The Eltran® (Epitaxial Layer TRANsfer) process, developed by Canon in the 1990s, is a method for fabricating SOI wafers (Fig. 3a) [46]. The process initiates by forming a porous structure with a high surface-to-volume ratio (~200 m^2 cm^{-3}) on the surface of a silicon seed wafer through electrochemical reactions [48]. This is followed by the growth of silicon via epitaxy on this structure [49]. An high-quality oxide layer is then grown by thermally oxidizing the porous silicon structure, which will serve as the BOX layer. Following the bonding of this prepared wafer to a handle wafer, the donor wafer is detached. This detachment is facilitated by the mechanically weak nature of the porous structure, thereby resulting in the formation of an SOI wafer. Using this technology, SOI wafers can be fabricated up to a size of 300 mm.

Efforts have been made to form two layers of porous structures with distinct pore morphologies in the donor

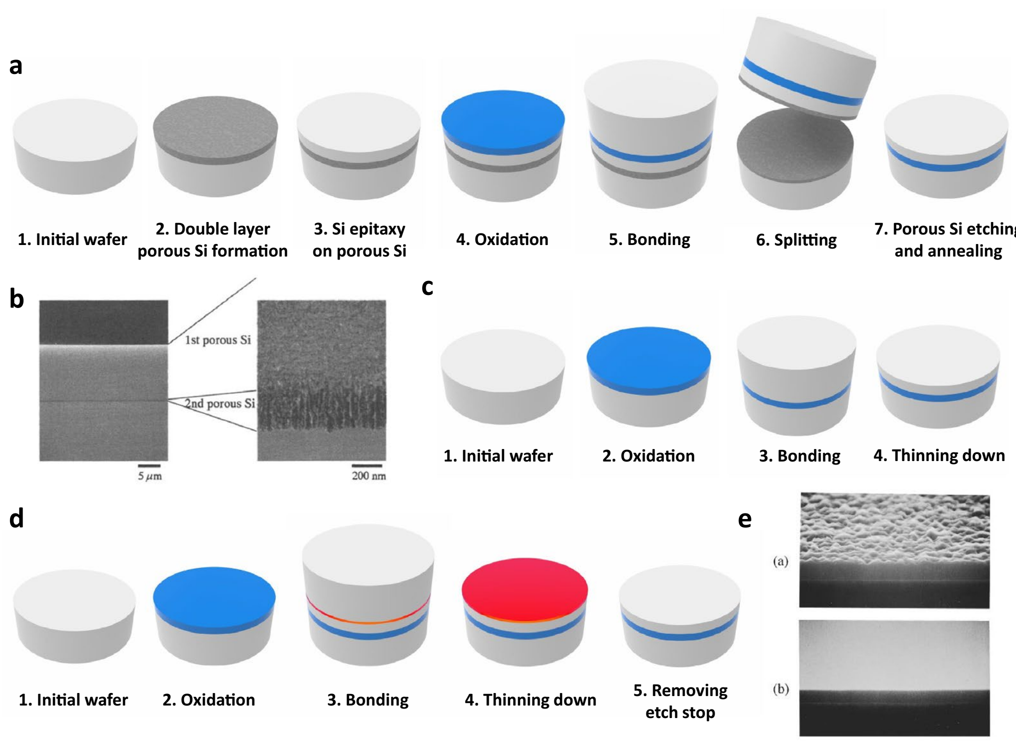

Fig. 3 **a** 3D schematic illustrating the fabrication of SOI wafers through the Eltran® technology. **b** Cross-sectional images of double layered porous Si formed by changing an anodic current. Reprinted from [46] with permission from Springer Nature. 3D schematic illustrating the fabrication of SOI wafers through the **c** BSOI and **d** BESOI technology. **e** Cross-sectional SEM images of the (top) as-etched BESOI and (bottom) the H_2 annealed BESOI The annealing condition is 1150 °C, 80 torr, 1 h in H_2. Reprinted from [47] with permission from AIP Publishing

wafer, aiming to facilitate the detachment process in the Eltran® method [50, 51]. By controlling the current flow, fine pores are first formed, followed by the formation of coarser pores deeper within the structure (Fig. 3b) [46]. The boundary between these two layers experiences substantial interfacial stress, enabling a more uniform cleavage when a water jet is used. After the formation of the SOI wafer, the surface's porous silicon is removed, and hydrogen annealing is implemented to yield an atomically flat surface [46].

Advantages

Crystal Originated Particles (COPs) are actually octahedral voids that form within the silicon boule during the Czochralski (CZ) crystal growth process, via a phenomenon known as void condensation [38, 52]. The COPs are typically found in SOI wafers that are produced using wafers fabricated by the CZ crystal growth method. However, the Eltran® method, by virtue of fabricating the device layer through epitaxial growth, avoids the occurrence of COPs [15]. Additionally, the absence of an ion implantation process contributes to maintaining a high-quality device layer in the Eltran® method. The Eltran® method also offers advantages, notably its ability to form a device layer ranging widely in thickness from several nanometers to micrometers, depending on the growth of silicon on the porous structure [53]. Furthermore, since oxidation occurs on the epitaxially grown silicon surface, the thickness of the BOX layer can also be adjusted over a wide range.

Challenges

The Eltran® process, which involves the epitaxial growth of a silicon layer on a rough, porous structure, inherently reflects this roughness in the resultant silicon layer [46]. To achieve the same level of smoothness as bulk wafers, surface planarization processes are necessary. However, these can lead to a reduction in film thickness and degradation of in-plane uniformity. Moreover, during the epitaxy process, the occurrence of stacking faults can compromise the quality of the device layer, necessitating process fine-tuning [51]. The fabrication of a double-layer porous structure, designed to facilitate transfer, also requires careful process fine-tuning. These factors combine to form a complex series of steps, each of which necessitates its own fine-tuning and thus further complicates the whole process Hence, the Eltran® method, with its requisite multiple process steps and inherent complexity, brings about issues related to high costs and low yield. Due to these challenges, the production of SOI wafers utilizing the Eltran® method has largely been discontinued.

BSOI/BESOI

Fabrication method and history

The Bonded SOI (BSOI) process was developed in the 1980 s. This technique involves forming a thermally grown or deposited oxide on one or both wafers, and these wafers, possessing hydrophilic oxide surfaces, are then directly bonded to fabricate an SOI wafer (Fig. 3c) [54]. The adhesion between the two is manipulated through annealing of the SOI wafer. The thinning down for the formation of the device layer is achieved through grinding, wet or dry chemical processes [55]. The BSOI method is predominantly employed to fabricate device layers with a thickness between 10 to 100 μm [56]. However, it presented a deterioration in uniformity when utilized for the fabrication of thinner device layers.

The Bonded Etch-Back SOI (BESOI) process enables the formation of a uniformly thin device layer during thinning down processes such as chemical etching by establishing an etch stop prior to bonding (Fig. 3d) [57]. This is commonly achieved by injecting a high dose of boron into the wafer to form an etch stop, or by forming a device layer on a boron (B) doped surface through epitaxy [38]. The etch stop is also established by Germanium (Ge) or combination of Ge and B [47]. After bonding the wafer, thinning down is done, followed by a selective etch to remove silicon up to the etch stop. Finally, the etch stop is removed to fabricate the SOI wafer. The as-etched BESOI reflects the roughness of the etch stop. Therefore, methods like hydrogen annealing are employed to smoothen it (Fig. 3e) [47]. Using these technologies, SOI wafers can be fabricated up to a size of 300 mm [58].

Advantages

As the device layer is fabricated from the silicon wafer in the BSOI process, it possesses a relatively lower defect density and higher quality. Additionally, because the wafer is thinned down in fabrication, it proves advantageous for manufacturing SOI wafers with a device layer much thicker than 10 μm. Both BSOI and BESOI processes can produce large diameter wafers with a single-crystalline device layer at an industrial-scale volume.

Challenges

Both the BSOI and BESOI processes involve substantial material wastage due to the thinning down of silicon after bonding. As a result, while other SOI wafer fabrication methods allow for the reuse of the donor wafer, the BSOI and BESOI processes do not afford this capability for wafer reuse. In the case of BSOI, there are instances of damage during the mechanical grinding process.

The advantages and limitations of each fabrication method explained previously are summarized in Table 1.

Table 1 Advantages and challenges of SOI wafer fabrication method

Method	Advantages	Challenges
SIMOX	Precision in controlling BOX layer	Cost and defect management
	Simplicity of the process	Lattice defect of device layer
	Localized BOX layer formation in wafer	Oxide precipitates in device layer and silicon pipe in BOX layer
Smart Cut™	Precision in controlling device layer	Limitations in defect-free SOI wafer
	Uniform device layer and BOX layer from nm to µm	Increased process complexity and cost due to the multiple process steps
	Reuse of high-quality seed wafers	Requirement of high bonding quality
	Ability to change the materials of the device layer and handle layer	
Eltran®	Absence of COP occurrence in the device layer	Reflection of the porous silicon roughness
	High quality device layer due to absence of ion implantation	Occurrence of stacking faults in epitaxy process
	Device layer and BOX layer from nm to µm	High cost and low yield due to multiple process steps and inherent complexity
BSOI/BESOI	Device layer with a thickness more than 10 µm	Material wastage due to thinning down
	Lower defect density	Damage during the mechanical grinding process

Table 2 Comparison of SOI wafer fabrication methods

Method	Implanted ion	Bonding	Post processing
SIMOX	Oxygen	X	Annealing, ITOX
Smart cut	Hydrogen, helium	O	Annealing, splitting, polishing
Eltran	X	O	Splitting, planarization
BSOI/BESOI	X	O	Thinning, planarization

Current SOI wafer production predominantly relies on ion implantation, bonding, and post processing. Based on this, Table 2 provides an overview of the necessary processes for each method. While a precise cost comparison for each fabrication method's processes is challenging, the number of processes required for each method can provide an indirect estimation of the associated costs.

The SOI wafer can be processed largely in the same manner as conventional silicon wafers. However, considerations about doping process become important due to the presence of the thin device layer on the BOX layer. Specifically, the SOI wafer demands precise control over doping depth and profile [59]. Additionally, factors such as transistor isolation through Shallow Trench Isolation (STI) technology and differences in thermal conductivity during thermal treatments significantly influence the optimization of the doping process. Such considerations are essential in ensuring uniformity and efficiency when doping an SOI wafer.

Characterization

Structural characterization

In SOI wafers, characterization of SOI structure is essential, as they significantly influence device fabrication. Typically, optical methods such as reflectometry and ellipsometry are employed for these measurements [63–65]. These techniques rely on fitting the measured data to a pre-calculated multilayer model to extract the thicknesses. They are especially effective for SOI wafers with well-characterized optical constants and atomically sharp, smooth interfaces. Besides the importance of measuring the thickness of the device and BOX layers, characterizing defects is equally critical, as they can adversely impact the performance and yield of devices. Defects in the device layer, often spanning several tens of micrometers and penetrating through the layer, can occur due to the condensation of silicon vacancies [66]. Such defects lead to the etching of the underlying BOX layer through a process known as HF etching, resulting in the formation of HF defects (Fig. 4a) [60, 67]. Evaluating these HF defects is paramount since they can significantly affect the fabricated device. Additionally, the Secco etch technique ($K_2Cr_2O_7$:H_2O:HF) can be utilized to assess the quality of the device layer [61, 68]. Stress arising from defects in the silicon network promotes localized etching, thereby forming etch pits (Fig. 4b). With increased etching time, these pits enlarge and traverse through the device layer. Analogous to the process with HF defects, the BOX layer beneath is etched using HF etching (Fig. 4c). These pits are then optically measured to ascertain the density of Secco defects within the wafer.

The residual stress in device layer is influencing the performance of ICs and MEMS devices. This residual stress is predominantly measured based on deformation. First, the residual stress of the device layer can be determined by applying the curvature measured using a profilometer to Stoney's equation [69]. Similarly, by backside etching the SOI wafer to release the device layer and then measuring the deformation with a white light interferometer,

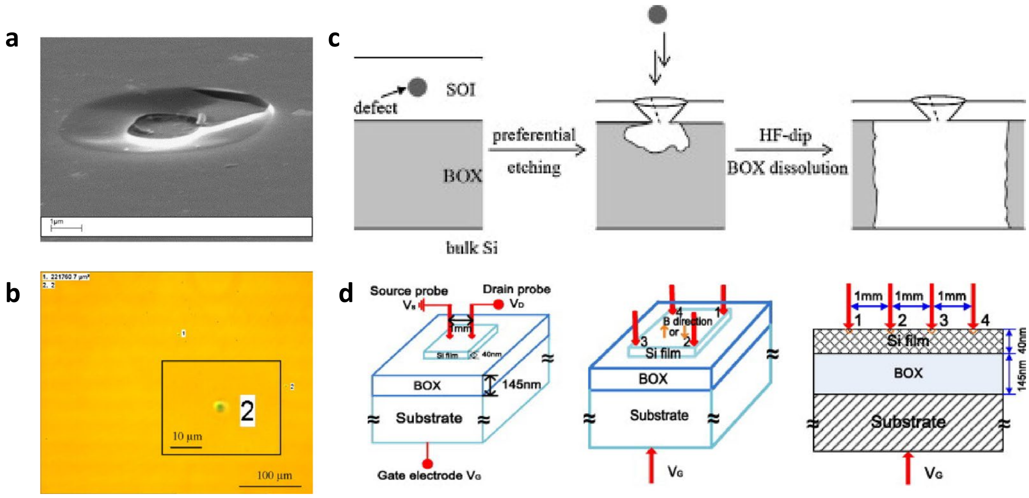

Fig. 4 **a** Tilted SEM image of HF defect for 23 nm Cz-SOI wafer. Reprinted from [60] with permission from Elsevier. **b** Optical image of the Secco defects on the SOI wafer. **c** Sketch of the defect delineation process in SOI: (left) initial position of the defect; (center) preferential etching at the defect site by the defect etching solution; (right) following immersion in HF, dissolution of the BOX beneath the defect. Reprinted from [61] with permission from Elsevier. **d** Schematic configuration for: (left) pseudo-MOSFET, (center) Hall effect and (right) 4-point probe. Reprinted from [62] with permission from Elsevier

the residual stress can be characterized by comparing it with theoretical formulas [70]. Recently, residual stress characterization has been achieved by fabricating MEMS cantilevers and measuring their deformation, subsequently comparing it with theoretical predictions [71]. For SOI wafers, surface roughness is also important for micro and nano-fabrication process. Surface roughness is typically determined using Atomic Force Microscopy (AFM), where a random area of several μm^2 is imaged [69]. The Root Mean Square (RMS) roughness is then derived from the image. Commercially available SOI wafers exhibit an RMS roughness of about 0.2 nm, comparable to that of standard silicon wafers.

Electrical characterization

A prominent method for the electrical characterization of ultra thin device layer is the pseudo-MOSFET technique [72–74]. This technique utilizes the inverted MOS structure of the SOI wafer, where the silicon substrate acts as the gate terminal and the BOX layer serves as the gate oxide (left of Fig. 4d). The device layer is selectively etched to form an island, and two probes are used to establish the source and drain. It's imperative that these probes are sufficiently distant from the ends of the island and have a diameter much smaller than the channel length. One of the notable advantages of this approach is the ability to operate and analyze the MOSFET characteristics without requiring manufacturing processes like doping or thermal treatments. Pseudo-MOSFET operates similarly to a fully-processed back-channel MOSFET. Thus, standard parameter extraction methods can be used to determine material parameters such as threshold and flat band voltages, electron and hole mobilities, interface traps, and oxide charges [75]. Consequently, it is capable of characterizing intrinsic properties of SOI with device layers ranging from 10 nm to several micrometers in thickness.

The Hall effect can be used to extract mobility and doping concentration [62]. Four probes are connected to the silicon island of the SOI wafer where the pseudo-MOSFET was measured (center of Fig. 4d). When a magnetic field is applied perpendicular to the SOI wafer, a current is passed through two of the probes, and the voltage is measured across the other two. From the measured voltages, the Hall voltage, which allows us to determine the Hall coefficient and Hall mobility, can be derived. Using these parameters, both the mobility and doping concentration can be extracted. While the Hall effect allows for the independent extraction of mobility and doping concentration, the 4-point probe can only determine the volume mobility when the activated doping concentration is known. For measurements, the probes are arranged at consistent intervals (right of Fig. 4d). When a current is applied to the two outer probes, the voltage drop between the inner two probes is measured, eliminating the series resistance. This enables the measurement of sheet resistance, and with a known doping concentration, the volume mobility can be derived. The previously mentioned methods, which utilized probes, are distinct from the microwave-reflectance photoconductivity decay technique that characterizes the carrier lifetime in a non-contact manner [76]. When light is irradiated on to the SOI wafer, charge carriers are generated. Concurrently irradiating with microwaves leads to a change in microwave reflection due to these generated charge carriers. As time progresses, the charge carriers produced by the light recombine with impurities or defects, leading to a temporal change in the intensity of the reflected microwaves. The generation efficiency of charge carriers and the changes in microwave reflection depend on the internal optical and electrical properties of the SOI wafer, especially on the density and mobility of the charge carriers. Additionally, as time progresses, the charge carriers generated by light recombine with impurities or defects. The rate of this recombination is directly tied to the electrical characteristics of the semiconductor and provides crucial information about the presence and distribution of impurities or defects.

Discussion

The SOI wafer, with its ability to streamline process steps and enhance device performance, still remains a viable option for future ICs or MEMS fabrication. However, despite its numerous advantages, the current production approach for SOI wafers still have room for improvement. The cost of SOI wafers is approximately 10 to 20 times higher than that of generic silicon wafers. This cost difference largely stems from the fact that most manufacturing methods involve multiple steps such as ion implantation, bonding, and post-processing. Additionally, processes like bonding and thinning down are typically applied to individual wafers. There's a pressing need for new SOI wafer production methods that can minimize or bypass individually applied steps and allow for the majority of the processes to be carried out via batch fabrication. Another critical consideration is the development of technology capable of producing SOI wafers with multiple alternating device and BOX layers. As of now, to fabricate a multi-layered SOI wafer, the process for producing a single SOI wafer should be repeated multiple times. This repetitive process significantly drives up the cost of multi-layered SOI wafers, complicating their practical application in actual devices. If a novel production method, different from merely repeating conventional technologies, is developed for crafting multi-layered SOI wafers, it could broaden the spectrum of devices that can be manufactured.

Conclusion

In this review, we aim to overview SOI wafer technology. We focuses on the fabrication methods of SOI wafers, emphasizing their advantages and challenges. We also look into the structural and electrical characterization techniques applied to fabricated SOI wafers. While SOI wafers are widely utilized in ICs and MEMS devices due to their inherent benefits, there remain room for improvement, particularly in cost minimization and the fabrication of multi-layer SOI wafers. Advancements in SOI wafer will undoubtedly pave the way for enhancements in device fabrication.

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Author contributions

TK: conceptualization, visualization, writing, editing. JL: supervision, writing, editing. Both authors read and approved the final manuscript.

Declarations

Competing interests

JL is the editor-in-chief of Micro and Nano Systems Letters. TK has no conflicts of interest to disclose.

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