A Comprehensive Survey on Hardware-Software co-Protection against Invasive, Non-Invasive and Interactive Security Threats

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***Abstract*—In the face of escalating security threats in modern computing systems, there is an urgent need for comprehensive defense mechanisms that can effectively mitigate invasive, non-invasive and interactive security vulnerabilities in hardware and software domains. Individually, hardware and software weaknesses and probable remedies have been practiced but protecting a combined system has not yet been discussed in detail. This survey paper provides a comprehensive overview of the emerging field of Hardware-Software co-Protection against Invasive and Non-Invasive Security Threats. We systematically review state-of-the-art research and developments in hardware and software security techniques, focusing on their integration to create synergistic defense mechanisms. The survey covers a wide range of security threats, including physical attacks, side-channel attacks, and malware exploits, and explores the diverse strategies employed to counter them. Our survey meticulously examines the landscape of security vulnerabilities, encompassing both physical and software-based attack vectors, and explores the intricate interplay between hardware and software defenses in mitigating these threats.Furthermore, we discuss the challenges and opportunities associated with Hardware-Software co-Protection and identify future research directions to advance the field. Through this survey, we aim to provide researchers, practitioners, and policymakers with valuable insights into the latest advancements and best practices for defending against complex security threats in modern computing environments.**

***Index Terms*—Hardware-Software co-Protection, Non-Invasive Attacks, Invasive Attacks, Hardware-Software Interaction, IC Security, Hardware Security**

I. Introduction

In an era characterized by ubiquitous computing and interconnected systems, ensuring the security and integrity of computing environments [1], [2], [3] has emerged as a paramount concern. The pervasive nature of modern computing infrastructures exposes them to an increasingly diverse array of security threats [4], [5], ranging from physical attacks [6], [7] on hardware components (e.g. Invasive and non-Invasive attacks [8]) to sophisticated software exploits [9], [10] targeting system vulnerabilities. In response to these multifaceted threats, researchers and practitioners have turned to a synergistic approach known as Hardware-Software co-Protection [11], [12] to fortify computing systems against both invasive and non-invasive security vulnerabilities. The abstraction layers of hardware and software are displayed in Figure 1

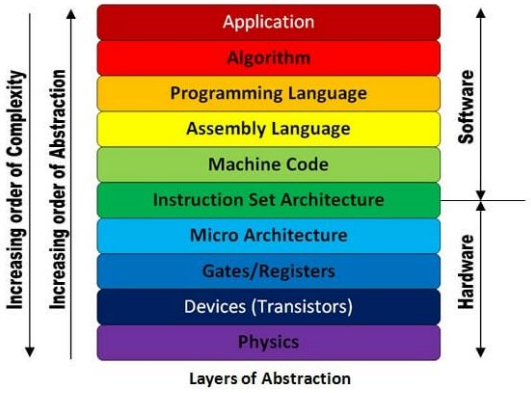


Fig. 1. HW-SW Layers of a computing system. [13]

The concept of Hardware-Software co-Protection embodies the integration of hardware and software-based security mechanisms, leveraging the strengths of each domain to create robust defenses against a broad spectrum of threats. Hardware-based defenses provide a solid foundation by implementing secure hardware architectures, encryption primitives [14], [15], and tamper-resistant technologies to safeguard critical system components against physical attacks. This security primitives in the hardware level can be incorporated in the software domain to facilitate risk-free execution of software programs [16], [17] . Meanwhile, software-based defenses employ techniques such as secure boot mechanisms, memory protection, and runtime monitoring to mitigate software vulnerabilities and thwart malware exploits. Software level techniques for security measurement [18] can be taken to construction of hardware to make the hardware secure.

This survey paper presents a detailed exploration of the Hardware-Software co-Protection paradigm against Invasive and Non-Invasive Security Threats. By systematically examining the landscape of security vulnerabilities and the interplay between hardware and software defenses, this survey aims to provide a thorough understanding of the latest advancements and best practices in this topic. Through an in-depth analysis

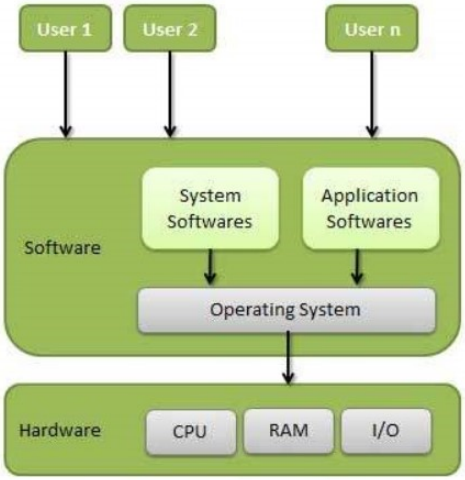


Fig. 2. How Softwares and Hardwares are intertwined in a Real Computing System.

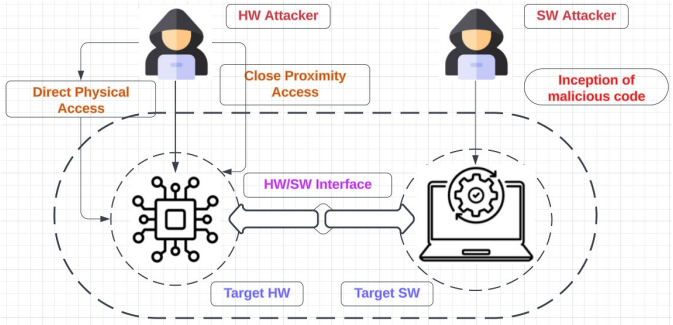


Fig. 3. HW-SW Attack Scenario and Possible co-Protection against them

of invasive threats targeting hardware components, including fault injection attacks [19], [20], [21] and reverse engineering techniques, coupled with an examination of software-based threats such as malware infections and side-channel attacks, this survey elucidates the diverse challenges facing modern computing systems. A framework for HW/SW co-ordination and probable holistic protection against attacks from either domain are shown in Figure 4.

The subsequent sections of this paper will discuss the following topics.

- *Overview of Security Threats in HW and SW Domain:* We will provide an in-depth examination of the current landscape of hardware security threats facing computing systems. This will include an analysis of both invasive threats, such as physical tampering and hardware Trojans, as well as non-invasive threats like software-based attacks including malware, side-channel attacks [22], and cryptographic vulnerabilities . By understanding the diverse range of threats, the paper sets the stage for the necessity of comprehensive protection mechanisms.
- *Threat model in SW and HW Domains Combined:* When a software runs into a hardware(e.g. RTL or gate level design), each of the domains are not aware of others' respective design properties or other quantities. We will explore which vulnerabilities or threats may arise because of lack of awareness of SW execution from hardware or hardware execution from software.
  For instance, it may happen that running a complex design in software domain is causing excessive power dissipation in a a particular part of the design. But the hardware is unaware and unprotected against this. Similarly, software is running without any awareness from the hardware execution. These kind of security vulnerabilities will be explored.
- *Insights from real-World instances and existing methodologies:* It will draw insights from real-world research papers to illustrate the effectiveness of hardware-software co-protection approaches. By referencing findings and case studies from reputable research publications, the paper will provide concrete examples of how these approaches have been implemented and their impact on enhancing security posture. This section will include summaries of key findings, experimental results, and comparative analyses from selected research papers.
- *Analysis of Co-Protection Methodologies:* This paper will delve into various methodologies and techniques that integrate both hardware and software defenses to mitigate security threats effectively. This analysis will cover a wide range of approaches including hardware sensor response based compiler execution, hardware root of trust, protection of software programs using hardware power traces and hardware model of invasive and non-invasive attacks, cryptographic accelerators, and software-based intrusion detection systems. The paper will discuss the strengths and limitations of each approach, highlighting the need for comprehensive solutions.
- *Categorization of Strategies:* We will categorize hardware-software co-protection strategies based on their underlying principles and deployment scenarios. This categorization may include classifications such as prevention techniques, detection mechanisms, and mitigation strategies. Additionally, the paper will categorize solutions based on the targeted threat models, such as protecting against physical attacks, network-based attacks, or insider threats.
- *Running and Future Working Directions and Challenges:* Lastly, the paper will discuss future directions and challenges in the development and implementation of hardware-software co-protection mechanisms. This may include emerging trends such as the integration of machine learning and AI-based approaches, challenges in securing emerging technologies like IoT and cloud computing, and the need for standardization and interoperability of security solutions.

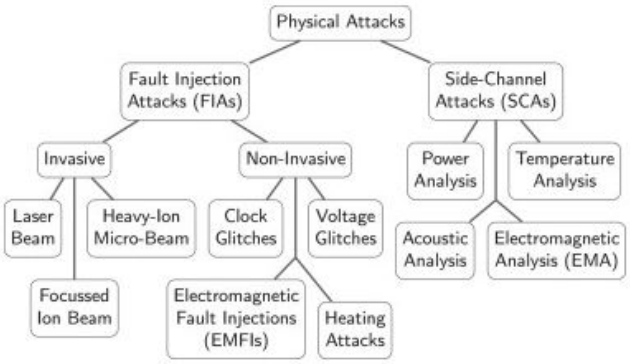


Fig. 4. HW Physical Attack Taxonomy [23]

II. Hardware non-Invasive and Invasive Security Vulnerabilities:

A. Hardware Non-Invasive Security Threats

Non-invasive hardware security vulnerabilities refer to weaknesses in electronic systems that can be exploited without physically altering the hardware [24]. These vulnerabilities often exploit unintended behaviors or characteristics of the hardware components themselves, such as electromagnetic emissions, power consumption, or timing variations. Principal types of non-Invasive attacks consist of fault injection attacks and side channel attacks.

1) Fault Injection Attacks:: These attacks involve inducing faults or errors in a device's operation to compromise its security. Through the exploitation of weaknesses within hardware design or the manufacturing process, attackers can inject faults such as voltage spikes, clock glitches, or electromagnetic interference. These flaws may result in unforeseen system behaviors, crashes, or breaches in security, posing a potential threat to the confidentiality, integrity, and availability of the system.

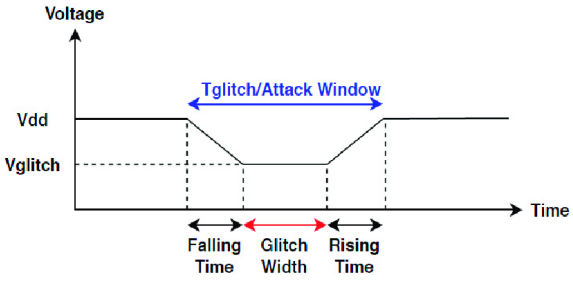


Fig. 5. Representation of negative voltage glitch [25]

- *Voltage glitch attack:* One major fault injection attack is Voltage glitching meaning manipulating the device's power supply to induce faults and trigger unexpected behaviors [26], [27]. By manipulating the voltage levels supplied to the device during its operation(please refer to Figure 5), attackers can induce glitches or faults in the system, causing it to malfunction or execute unintended commands. These attacks are often meticulously timed to occur during critical moments, such as cryptographic operations or authentication processes, enabling attackers to bypass security measures or extract sensitive information.

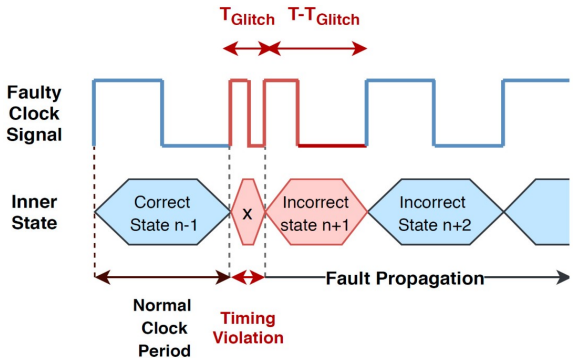


Fig. 6. Representation of clock glitch and fault-injection [28]

- *Clock glitch attack:* Clock glitching means introducing glitches into the device's clock signal (please refer to Figure 6) to disrupt its normal operation [29], [30] and potentially exploit vulnerabilities. By manipulating the clock signals that govern the device's operations, attackers can introduce glitches or disturbances in the timing sequence, causing the device to behave unpredictably or execute unintended instructions(please refer to Figure 6).
- *Optical fault Injection:* Using laser or light pulses to induce faults in the device's components [31] leading to security compromises. In this type of attack, a focused laser beam is precisely targeted at specific components within the device, such as integrated circuits or memory cells. By introducing localized heat or inducing electromagnetic interference, the laser can disrupt the normal operation of the targeted components [32], causing faults or errors in their behavior. These faults can be exploited by attackers to manipulate the device's operation, extract confidential data, or bypass security measures.

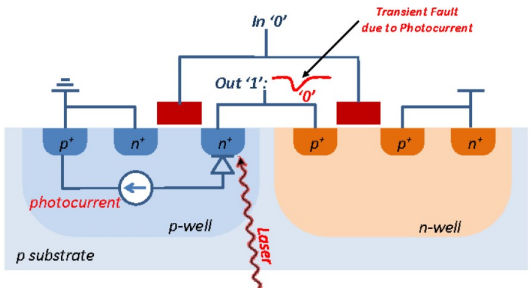


Fig. 7. Generation of photocurrent through the back-side due to LASER attack. [33]

2) Side Channel Attacks:: These attacks exploit information leaked by a device during its normal operation [34], such as power consumption, electromagnetic radiation, or timing variations. Common types include:

- *Power Analysis Attacks:* A Power Analysis Side-Channel Attack involves exploiting fluctuations in the power usage

of electronic devices during their functioning to deduce confidential information, like cryptographic keys or processed data [35], [36], [37]. By monitoring and analyzing these power consumption patterns, attackers can infer details about the device's internal operations, such as executed instructions or variable values. This type of attack is especially concerning for embedded systems and cryptographic devices due to its potential for remote execution without physical access.

- *Electromagnetic (EM) Side-Channel Attacks:* An Electromagnetic (EM) side-channel attack is a sophisticated method used to exploit unintentional emissions of electromagnetic radiation or electrical signals from electronic devices during their operation. By analyzing these emissions, attackers can glean sensitive information [38], [39], [40] such as cryptographic keys or data being processed by the device, without directly accessing the device itself. EM side-channel attacks pose a significant threat to the security of embedded systems, particularly those handling confidential or sensitive information, and require specialized equipment and expertise to execute.
- *Timing Attacks:* Timing variations in a device's operations can be exploited to deduce information about cryptographic computations or sensitive processes [41], [42].

B. Hardware Invasive Security Threats

Invasive hardware attacks involve physically tampering with electronic devices to exploit vulnerabilities or compromise their security [43]. Unlike non-invasive attacks that rely on analyzing the device's behavior or emissions without altering its physical structure, invasive attacks directly manipulate the hardware components. These attacks typically require physical access to the device, allowing attackers to directly interact with its internal circuitry.

Hardware Trojan attacks [44], [45], [46] involve the clandestine insertion of malicious circuitry, known as Trojans, into integrated circuits (ICs) during the design or manufacturing stages. These Trojans are designed to remain dormant under normal operating conditions but can be triggered remotely or under specific circumstances to perform malicious activities, such as leaking sensitive information [47], causing system malfunctions, or providing unauthorized access. Hardware Trojans pose significant challenges to the integrity and security of electronic systems [48], as they can evade traditional software-based security measures and remain undetected during functional testing. Detecting and mitigating hardware Trojans [49] require specialized techniques, including physical inspection, side-channel analysis, and formal verification, to ensure the trustworthiness of hardware components and prevent potential exploitation.

Attackers physically modify the device's circuitry at the chip level to introduce backdoors, modify functionality, or bypass security mechanisms. This can involve techniques such as laser cutting, wire bonding, or focused ion beam (FIB) milling.

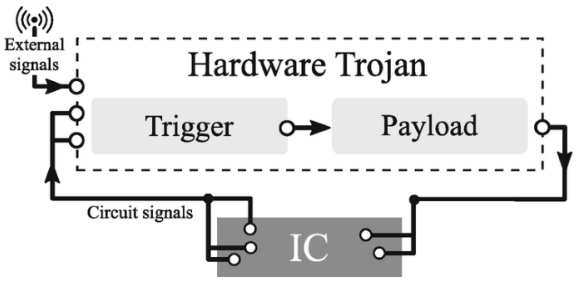


Fig. 8. Hardware Trojan [50]

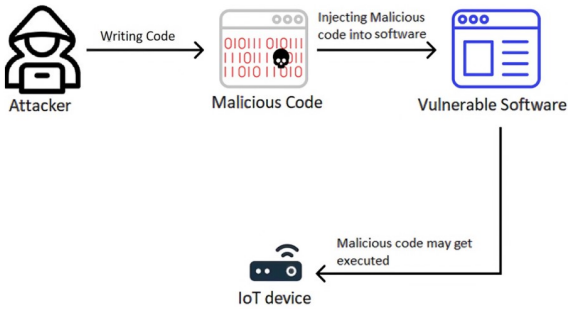


Fig. 9. Bad code injection process [51]

III. Software Execution Vulnerabilities

Software program security threats encompass a broad spectrum of risks and vulnerabilities that can compromise the confidentiality, integrity, and availability of software systems [52]. These threats can originate from various sources, including malicious actors, software bugs, design flaws, and insecure coding practices. Understanding and mitigating these threats are essential for ensuring the trustworthiness and reliability of software applications. Below are some common types of software program security threats:

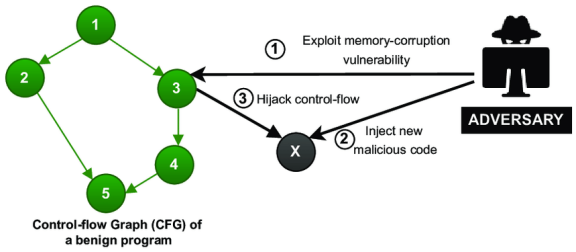


Fig. 10. Example of code-injection attack. The CFG represents the accurate execution flows of a harmless software, where the graph nodes(1-5) indicate a software instruction. A code-injection attacker performs the actions 1-3. [53]

- *Malware:* Malicious software, such as viruses, worms, Trojans, and ransomware, pose significant threats to software security [54]. Malware can infiltrate systems through various vectors, including email attachments, malicious websites, and infected software downloads. Once installed, malware can steal sensitive information, disrupt system operations, and provide unauthorized access to

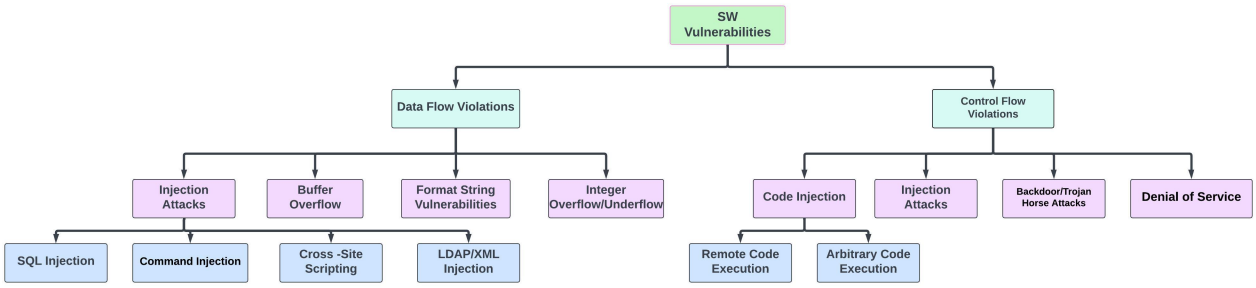


Fig. 11. SW Vulnerabilities and Attacks for data and control flow violations.

attackers [55]. A malicious code injection process can be seen in Figure 9.

- *Code Injection Attacks:* Injection attacks like SQL injection and cross-site scripting (XSS), can probe for vulnerabilities in software input validation mechanisms. Attackers inject malicious code or commands into input fields [56], allowing them to manipulate the behavior of the software and access sensitive data stored in databases or execute unauthorized actions on behalf of legitimate users. By inserting bad code, adversaries can also attempt to steal data and/or control flow of the software design [53], which can be seen in Figure 10.
- *Authentication and Authorization Flaws:* Weak or inadequate authentication and authorization mechanisms can lead to unauthorized access to sensitive data and functionalities. Common vulnerabilities include weak passwords, insufficient password policies, insecure session management, and privilege escalation exploits. Attackers exploit these flaws to bypass validation controls and acquire illegal access to critical system resources.

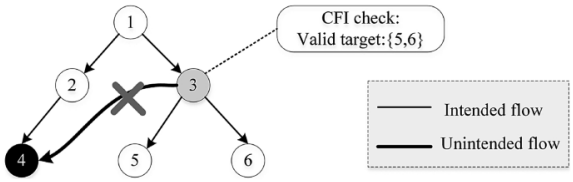


Fig. 12. Control Flow Integrity [57]

- *Information Leakage:* Information leakage vulnerabilities occur when sensitive data is inadvertently exposed to unauthorized parties [58], [59]. This can happen through various channels, including error messages, log files, configuration files, and network transmissions. Attackers can exploit information leakage vulnerabilities to gather intelligence about system configurations, user behaviors, and application logic, facilitating further attacks [60].
- *Data Exfiltration Attacks:* Data exfiltration attacks involve unauthorized extraction or leakage of sensitive data from a software program. Attackers may exploit vulnerabilities in data handling processes, such as insecure data storage, weak encryption, or inadequate access controls, to steal sensitive information. By compromising data flow integrity, attackers can extract confidential data, trade secrets, or personally identifiable information (PII) from the target system.

Fig. 13. Data Leakage Resources.

- *Data Tampering:* Data tampering attacks involve unauthorized modification or manipulation of data stored or transmitted by software systems. Attackers can tamper with data to alter its integrity, accuracy, or authenticity [61], leading to erroneous decisions, financial fraud, or privacy breaches. Common targets of data tampering attacks include databases, configuration files, digital documents, and network communications [62].

IV. Threat Model: SW-HW Affecting Each Other

When there is a specific security attack in hardware domain, it often occurs that software execution is unaware of hardware vulnerabilities and vice versa. Software and hardware being unaware of each others' execution gives rise to several vulnerabilities to each domain.

How hardware attacks affect software execution:

- *Data breaches:* Hardware vulnerabilities, such as side-channel attacks or insecure memory access, can compromise the confidentiality of sensitive data processed by software applications. Attackers may exploit weaknesses in hardware components to gain unauthorized access to data stored in memory [64] or transmitted across the sys-

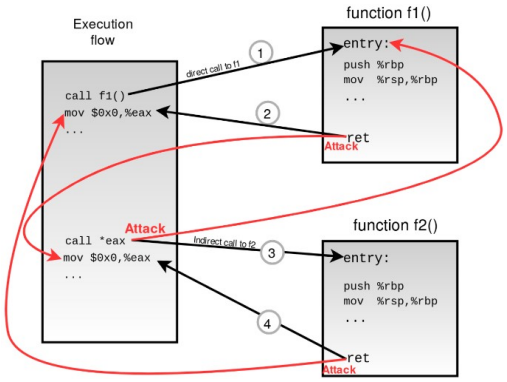


Fig. 14. Bypass example of coarse-grained control flow integrity. The attacker can divert the control flow from several calls and return points. Red arrows show the valid destinations where attackers can redirect the flow. [63]

tem, jeopardizing the privacy of users and organizations [65].

Hardware vulnerabilities can significantly contribute to the emergence of software data breaches by providing attackers with exploitable entry points into systems. These vulnerabilities often stem from weaknesses in the design, implementation, or configuration of hardware components, such as processors, memory modules, or peripheral devices. Attackers can exploit these vulnerabilities to acquire uninvited access to security-critical data or manipulate the behavior of software systems.

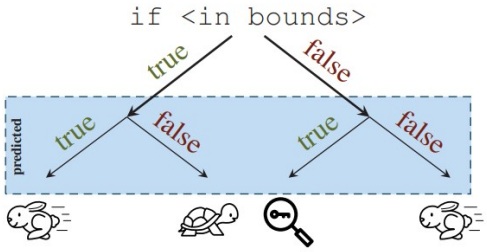


Fig. 15. Spectre attack scenario. Until the bounds check yields a definitive outcome, the branch predictor proceeds with the anticipated branch target, enhancing overall execution speed when predictions are accurate. However, in cases where the bounds check is mistakenly predicted as true, there's potential for secret information leakage under specific circumstances. [66].

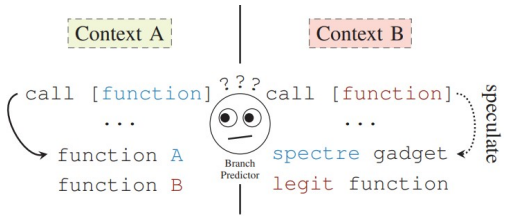


Fig. 16. Spectre attack scenario. Branch predictor makes wrong prediction according to training data from adversaries [66].

An instance of this attack is when attackers leverage hardware vulnerabilities to execute malicious code or exploit software bugs that would otherwise be inaccessible. For example, hardware vulnerabilities like speculative execution flaws (e.g., Spectre [66], Meltdown [67] and deterministic rowhammer [68]) can be exploited to bypass software-based security measures and access privileged information stored in memory. Similarly, vulnerabilities in hardware-based encryption or authentication mechanisms can undermine the security of software applications that rely on these mechanisms for data protection.

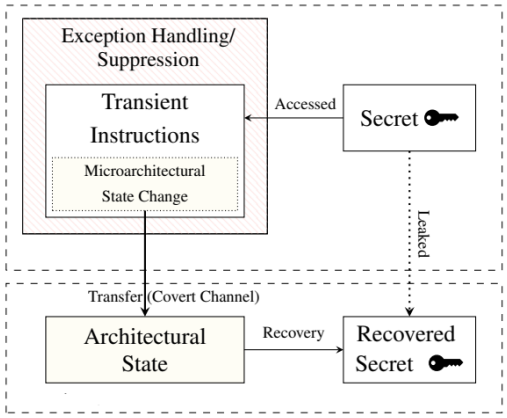


Fig. 17. The Meltdown exploit leverages exception handling or suppression to execute a sequence of temporary instructions. These temporary instructions acquire a secret value that persists and alter the microarchitectural state of the processor accordingly. This establishes one end of a microarchitectural covert channel. The recipient end reads the microarchitectural state, converting it to architectural, and retrieves the secret value. [67].

- *Integrity compromise:* Hardware-level attacks, such as firmware tampering or hardware Trojans, can undermine the integrity of software execution by injecting malicious code or altering critical system functions. This can lead to the execution of unauthorized commands, modification of software binaries, or manipulation of system behavior, posing significant risks to the reliability and trustworthiness of software applications.

  Hardware vulnerabilities can serve as the foundation for software integrity violations, undermining the trustworthiness of software systems and leading to potential security breaches. These vulnerabilities may arise from flaws in the design, implementation, or configuration of hardware components, such as processors, memory modules, or input/output devices. Attackers can exploit these vulnerabilities to manipulate the execution environment of software applications, compromise the integrity of data, or subvert critical security mechanisms.

  For instance, attackers leveraging hardware vulnerabilities to inject malicious code into software systems or modify existing code to alter program behavior. For example, vulnerabilities in hardware-based memory protection mechanisms can enable attackers to overwrite critical system data or execute arbitrary code in privileged contexts, leading to unauthorized access or control over software resources [69], [66]. Similarly, flaws in hardware-based encryption or authentication mechanisms can be exploited to bypass software-based security con-

trols and tamper with data integrity, compromising the trustworthiness of software operations [70], [71].

- *Availability Issues:* Hardware-based security threats can disrupt the availability of software services by exploiting vulnerabilities in underlying hardware infrastructure. Denial-of-Service (DoS) attacks [72] targeting hardware components, such as network interface controllers or memory modules, can degrade system performance, cause system crashes, or render software applications inaccessible, resulting in service disruptions and financial losses.

  A frequent occurrence involves attackers leveraging hardware vulnerabilities to exhaust system resources like CPU, memory, or network bandwidth, inundating the system with an abundance of traffic or nefarious requests. For instance, weaknesses in network hardware or protocols may be utilized to produce extensive volumes of network activity [73], overwhelming network connections and inducing congestion or packet loss. Likewise, deficiencies in memory management units (MMUs) [74] or memory controllers may prompt memory depletion or fragmentation, thereby precipitating system instability or failures.

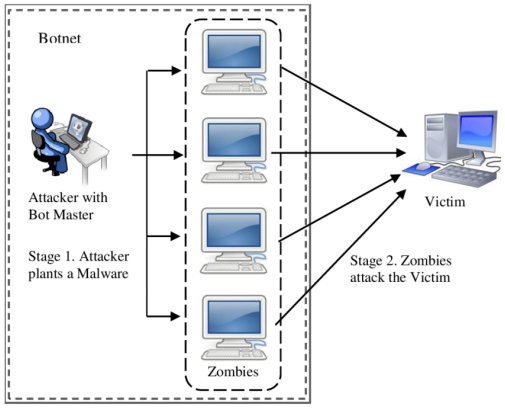


Fig. 18. A simple distributed denial of service attack scenario. [75].

Furthermore, compromised hardware components can serve as attack vectors for launching distributed denial-of-service (DDoS) attacks [72], [76], [77], where multiple compromised devices coordinate to flood target systems with malicious traffic. For instance, attackers may exploit vulnerabilities in Internet of Things (IoT) devices or embedded systems to create botnets capable of launching massive DDoS attacks against internet-facing services, disrupting their availability to legitimate users (Figure 18.

- *Software Exploitation:* Hardware vulnerabilities can serve as entry points for exploiting software vulnerabilities, enabling attackers to escalate privileges [66], [67], execute arbitrary code, or bypass software-based security mechanisms [78]. By exploiting weaknesses in hardware architectures, attackers can launch sophisticated attacks, such as buffer overflows, code injection [79], [80], or privilege escalation [66], compromising the security and stability of software systems.

  Some hardware vulnerabilities, such as buffer overflows or memory corruption flaws in processors, can directly impact software execution. Attackers can craft malicious inputs or code sequences that exploit these vulnerabilities to gain unauthorized access [81], execute arbitrary code, or manipulate system behavior.

How software attacks affect hardware execution:

Software attacks can significantly impact hardware execution by exploiting vulnerabilities in software components to manipulate or compromise the behavior of underlying hardware. These attacks can manifest in various forms, including:

- *Malware Exploitation:* Malicious software such as viruses, worms, or Trojans can extract security weaknesses in operating systems or applications to acquire unauthorized access to hardware resources. Once compromised, the malware can manipulate hardware functionality, disrupt system operations, or steal sensitive data.
- *Code Injection:* Techniques like buffer overflows or injection attacks enable attackers to inject malicious code into running processes. If successful, this injected code can execute arbitrary commands, manipulate hardware registers, or even reconfigure hardware settings, leading to system instability or unauthorized access.

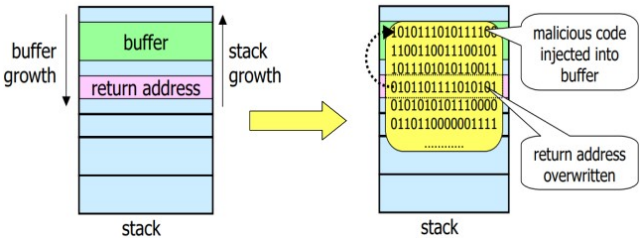


Fig. 19. Code injection attack scenario using stack. [82].

- *Privilege Escalation:* Software vulnerabilities those allow unauthorized users to escalate their privileges can enable attackers to gain elevated access to hardware resources. With escalated privileges, attackers can manipulate hardware configurations, access restricted data, or install malicious firmware, compromising the integrity of the hardware platform [83].

  Windows/Linux kernel Privilege escalation: This vulnerability allowed attackers to escalate privileges on Windows or Linux systems [84] by exploiting a flaw in the kernel. By running a specially crafted application, an attacker could execute arbitrary code with elevated privileges, potentially gaining unauthorized access to hardware resources and compromising system integrity [85].
- *Denial-of-Service (DoS) Attacks:* DoS attacks targeting software vulnerabilities can overwhelm hardware resources with excessive requests or malicious traffic. Software vulnerabilities can lead to unauthorized hardware Denial of Service (DoS) attacks through various mechanisms. Here's how:

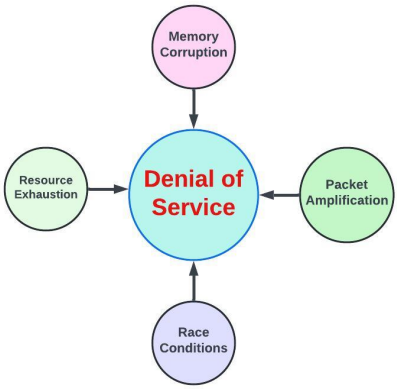


Fig. 20. Sources of denial of service attack in hardware due to software vulnerabilities.

- *Resource Exhaustion:* Vulnerabilities in software systems can be exploited to consume excessive system resources, such as CPU, memory, or network bandwidth. Attackers can leverage these vulnerabilities to launch DoS attacks by flooding the system with requests or executing resource-intensive operations [86], leading to the exhaustion of hardware resources and causing legitimate users to be denied access to the system [87]. Significance of detection [88] and prevention of resource exhaustion attack is paramount.
- *Memory Corruption:* Software vulnerabilities, such as buffer overflows [89], [90] or memory corruption flaws, can result in memory leaks or memory corruption issues. Attackers can exploit these vulnerabilities to consume system memory excessively [91], leading to memory depletion and system instability. This can cause hardware components to become unresponsive or malfunction, resulting in a Denial of Service for legitimate users.
- *Packet Amplification:* Vulnerabilities in network protocols or network-facing software can be exploited to amplify network traffic, leading to network congestion and service disruption. Attackers can manipulate network packets to increase their size or frequency, leveraging vulnerable software components to amplify the impact of their attacks on hardware resources, such as network switches, routers, or firewalls.
- *Interrupt Storms:* Software vulnerabilities in device drivers or kernel components can lead to the generation of excessive hardware interrupts or interrupts storms. Attackers can exploit these vulnerabilities to trigger a large number of hardware interrupts, overwhelming the system's interrupt handling capabilities and causing hardware devices to become unresponsive or enter into a degraded state, resulting in a Denial of Service for legitimate users.
- *Race Conditions:* Software vulnerabilities those result in race conditions or concurrency issues can be exploited to disrupt the normal operation of hardware components. Attackers can manipulate the timing or sequence of software operations to create race conditions [92], [66], leading to unpredictable behavior in hardware devices or systems. This can result in hardware resources being locked or unavailable for legitimate users, causing a Denial of Service [76].

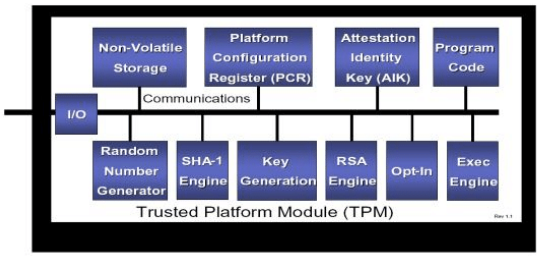
- *Firmware Exploitation:* Vulnerabilities in firmware, such as BIOS or device drivers, can be exploited to compromise hardware functionality. Attackers can modify firmware settings, implant rootkits, or disable security features, undermining the integrity and security of the hardware platform [93].
- *Side-Channel Attacks:*
Software side-channel attacks, such as timing attacks or cache-based attacks while primarily targeting vulnerabilities within software, can also precipitate significant issues in hardware components. These attacks exploit the unintended leakage of information from software execution, often exploiting the underlying architecture and implementation of hardware. For instance, speculative execution [66], a performance optimization technique in modern processors, can inadvertently expose sensitive data through timing or cache-based side channels. This exposure can lead to a myriad of problems in hardware, including compromised confidentiality, integrity, and availability.

V. Existing Techniques for Hardware Software Co-Protection:

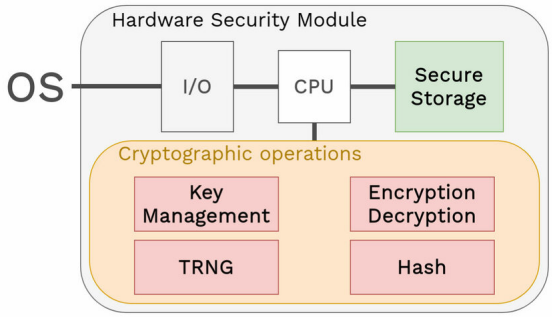
A. Hardware-based Security Mechanisms:

Hardware-based security features such as Trusted Platform Modules (TPM) [94], [95], Secure Enclaves (e.g., Intel SGX) [96], and Hardware Security Modules (HSM) [97], [98] provide a secure foundation for software execution. These components offer secure storage, cryptographic operations, and isolation mechanisms to protect sensitive data and code.

A Trusted Platform Module (TPM) operates as a secure cryptoprocessor that provides a hardware-based approach to managing and protecting cryptographic keys and other sensitive data. At its core, the TPM is designed to carry out cryptographic operations and securely store keys that protect information [94]. When a system with a TPM starts up, the module conducts a series of integrity checks to ensure that the system has not been tampered with. This process, known as the Trusted Boot (tBoot), involves validating each component of the startup process before it is loaded, ensuring that only trusted software is executed. The TPM can generate cryptographic keys that remain within the device; these keys can be used for various security functions but cannot be extracted by software. Additionally, the TPM can encrypt and decrypt data using these keys, providing secure storage that is resistant to external software attacks [95].



(a) A typical Trusted Platform Module Architecture. [99]



(b) Hardware Security Module Architecture. [100]

The TPM also supports remote attestation, creating a virtually tamper-proof environment. This feature allows the TPM to provide a cryptographic report of the hardware and software configuration of the host system to a remote verifier, ensuring that the system is secure and has not been altered. Furthermore, the TPM can seal and bind data, encrypting it in such a way that it can only be accessed on the same TPM with the same hardware configuration. This ability makes TPMs invaluable for scenarios requiring high levels of data security, such as in enterprise environments where ensuring the confidentiality and integrity of sensitive data is critical. Overall, the operation of a TPM enhances the security of a computing system by integrating hardware-based security measures that protect against unauthorized access and tampering.

However, exiting TPM systems possess several drawbacks including performance overhead, cost implications, complexity in management, compatibility issues etc.

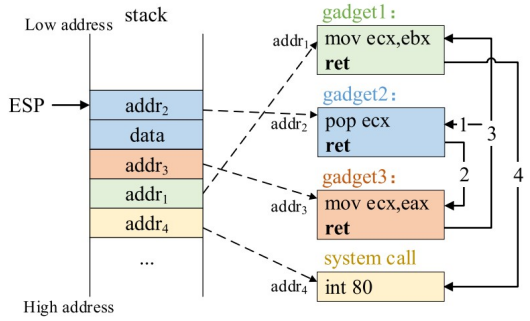


Fig. 21. An example Return on Programming(ROP) attack. [101]

program by altering the destination addresses of indirect jump or call instructions, thereby seizing control over the program's flow. To safeguard against such tampering, a linear encryption technique, such as XOR encryption, encrypts the instructions located at these target addresses, fortifying the integrity of the program's control flow.

When an indirect jump or call instruction is triggered, the instructions at the destination addresses undergo decryption using a decryption key generated through XOR encryption of key2 (as shown in Figure 22) and the address of the call site acquired from the PC register. As long as the program adheres to the paths outlined in the original Control Flow Graph (CFG), the decryption process will proceed accurately, enabling the program to operate smoothly. However, deviating from these paths may lead to a system error and failure of the Jump-Oriented Programming (JOP) technique.

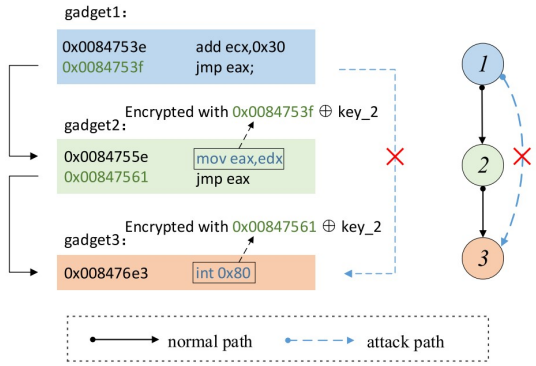


Fig. 22. An example of protecting the control flow of a program encrypting all first instructions at target addresses in the CFG. [101]

B. *Software-hardened Hardware:*

Software techniques such as Data Flow Integrity(DFI) [102], [103] , Data Execution Prevention (DEP) [104], and Control Flow Integrity (CFI) [105], [106], [107] can be implemented to harden hardware against various attacks. These measures make it more difficult for attackers to exploit vulnerabilities in hardware components. But often they include code-redundancy and data-redundancy.

An example control flow protection method is explained in Figure 22. Adversaries manipulate the control flow of a

C. *Hardware-assisted Sandboxing:*

Hardware virtualization technologies such as Intel VT-x [108] and AMD-V enable the creation of isolated execution environments, or sandboxes, where untrusted software can run safely. By leveraging hardware support for virtualization, these sandboxes provide strong isolation between applications and the underlying system.

Hardware-assisted sandboxing leverages specialized features within the hardware architecture to enhance the security and isolation of software applications. By utilizing hardware

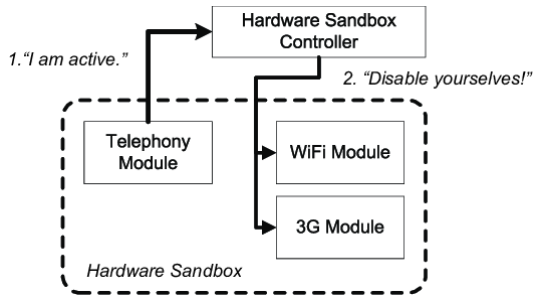


Fig. 23. An instance showcasing the application of hardware sandboxing is the prevention of real-time wiretapping over the internet. This is achieved by disabling all hardware modules necessary for Internet connectivity while a phone call is in progress. [109]

support, such as virtualization extensions in modern CPUs, sandboxing can create isolated environments, known as sandboxes, where untrusted or potentially malicious code can run safely without compromising the integrity of the host system. These hardware features enable the efficient implementation of sandboxing mechanisms, such as memory isolation, privileged access controls, and secure execution environments. As a result, hardware-assisted sandboxing offers robust protection against various security threats, including malware, exploits, and unauthorized access, thereby safeguarding sensitive data and critical system resources.

D. Fine-grained Access Control:

Hardware-enforced access control mechanisms, such as Memory Protection Units (MPUs) [110], [111] and Hardware-based Access Control (HBAC) [112], [113], restrict access to critical resources based on predefined security policies. These mechanisms prevent unauthorized access and limit the impact of software vulnerabilities.

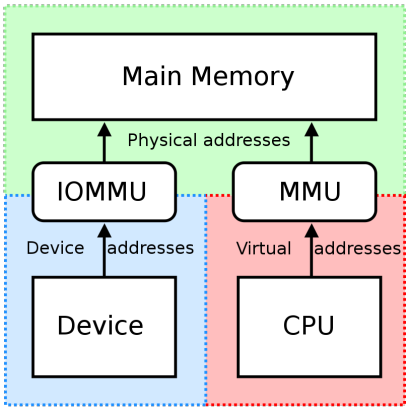


Fig. 24. A typical architecture of memory management unit. Memory management or protection unit is used as a fine grained HW resource distribution approach. [114]

The Memory Protection Unit (MPU) oversees processor transactions, such as instruction fetches and data accesses, and is capable of initiating a fault exception upon detecting an access violation(Figure 25). The primary objective of MPU is to restrict a process from accessing memory regions that have not been specifically allocated to it.

At its core, the MPU operates by defining and enforcing access permissions for various memory regions based on predefined rules and configurations. These rules typically include specifying the allowable types of access (e.g., read, write, execute) and the range of memory addresses accessible to each process or application.

When a processor executes instructions or accesses data in memory, the MPU monitors these transactions and compares them against the configured memory protection settings. If an access violation is detected such as an attempt to read from or write to a memory region that the process is not authorized to access the MPU triggers a fault exception which interrupts the normal flow of execution.

Fine-grained access control of hardware plays a crucial role in reducing software security vulnerabilities by providing granular control over the interactions between software components and hardware resources [114]. By allowing administrators to define precise rules governing access to hardware resources such as memory, input/output ports, and peripherals, fine-grained access control restricts the ability of malicious software to exploit hardware vulnerabilities for unauthorized access or privilege escalation [115], [116] . This approach enhances security by minimizing the attack surface exposed to potential exploits and mitigating the impact of software bugs or vulnerabilities that could otherwise be leveraged to compromise system integrity [117]. Furthermore, fine-grained access control facilitates the implementation of defense-in-depth strategies, where multiple layers of security mechanisms work together to protect against different types of threats, thereby strengthening the overall resilience of the system against cyberattacks.

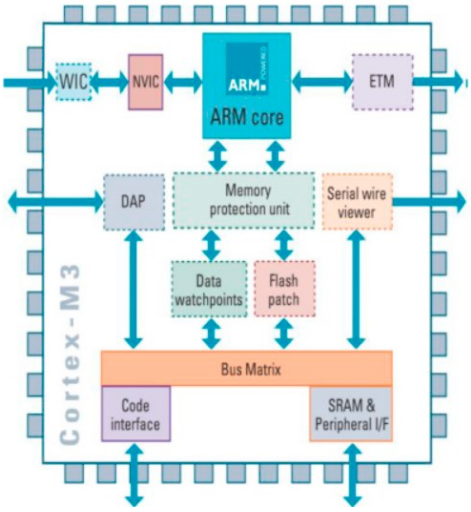


Fig. 25. Memory protection unit available in ARM-cortex M7. [118].

E. Hardware-accelerated Cryptography:

Hardware accelerators for cryptographic operations [119], such as AES-NI and SHA extensions in modern CPUs [120],

improve the performance and efficiency of cryptographic algorithms. By offloading cryptographic tasks to dedicated hardware, these accelerators reduce the attack surface and enhance overall system security.

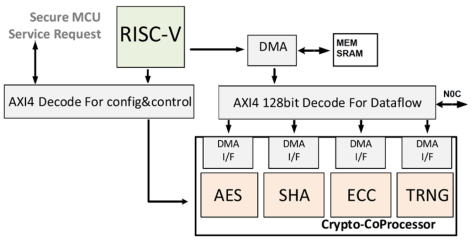


Fig. 26. Hardware architecture of a system with cryptographic accelerator. [121].

Hardware-accelerated cryptography represents a powerful approach to mitigating hardware and software security vulnerabilities by offloading cryptographic operations to specialized hardware components. By leveraging dedicated cryptographic processing units or accelerators integrated into modern hardware architectures, such as CPUs, GPUs, or dedicated cryptographic co-processors, hardware-accelerated cryptography enhances the efficiency and security of cryptographic operations while reducing the burden on software implementations. This not only improves the overall performance of cryptographic algorithms but also minimizes the exposure of sensitive cryptographic keys and operations to potential software-based attacks, such as side-channel attacks or malware exploits.

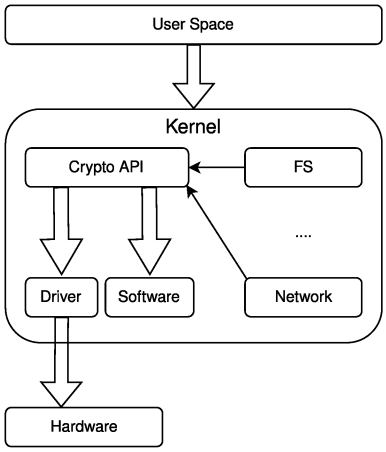


Fig. 27. A crypto API stack. [121].

For instance, when a user space application initiates a cryptographic operation through the Crypto API, the request is relayed to the kernel, which then determines whether to execute it using hardware or software, based on a priority-based hierarchy. While the Linux kernel itself provides a software implementation as an alternative to OpenSSL, hardware implementations typically take precedence due to their higher priority. Applications utilizing this API remain oblivious to the underlying method employed for cryptographic computation, allowing for potential acceleration via either hardware or more efficient software implementations, all without necessitating modifications to their code. The sole requirement is the inclusion of any new implementation into the existing priority list.

F. Hardware-based Intrusion Detection and Prevention:

Hardware-based intrusion [122] detection and prevention systems (IDPS) use specialized hardware components, such as network interface cards (NICs) [123] and programmable logic devices (FPGAs), to monitor and analyze network traffic in real-time. These systems detect and block malicious activities before they can compromise the system.

Hardware-based intrusion detection and prevention systems are a proactive cyber-security approach utilizing dedicated hardware components to detect and mitigate threats at the hardware level. These systems employ specialized hardware modules, like security co-processors or dedicated intrusion detection units, to continuously monitor system activity in real-time. By analyzing network traffic, system calls, memory access patterns, and other critical system events, hardware-based intrusion detection systems can identify anomalous behavior indicative of potential security breaches or unauthorized access attempts. Additionally, these systems can implement hardware-enforced security policies and access controls to prevent malicious activities from compromising system integrity. Operating at the hardware level offers several benefits, including reduced overhead, increased resilience against sophisticated attacks, and improved scalability across heterogeneous computing environments. In summary, hardware-based intrusion detection and prevention systems play a crucial role in strengthening cyber-security defenses, providing an extra layer of protection against evolving cyber-threats.

VI. Analysis of Co-Protection Methodologies: Proposed Approaches

Hardware can be protected through software feedback, and software can be protected using hardware feedback. Hardware-software co-protection methodologies aim to fortify systems against security threats by leveraging a combination of hardware sensors, power spectrum analysis, and information flow modeling. Hardware sensors can be integrated into devices to monitor physical and operational parameters, such as temperature, voltage fluctuations, and electromagnetic emissions, providing real-time insights into potential tampering or anomalies. Power spectrum analysis further enhances security by analyzing the electrical signals produced by hardware components to detect unusual patterns indicative of malicious activity. Meanwhile, information flow modeling involves mapping and controlling the pathways through which data travels within a system, ensuring that sensitive information is protected and that any unauthorized access or data leakage is promptly identified. By combining these approaches, systems can achieve a robust defense mechanism that not only detects and responds to threats in real-time but also proactively mitigates vulnerabilities through comprehensive monitoring and control.

A. *Hardware sensor based SW Protection:*

Hardware sensors are integrated into the physical components of the system, including processors, memory modules, input/output interfaces, and peripheral devices. These sensors continuously monitor physical parameters such as temperature, voltage, current, electromagnetic emissions, and other environmental conditions.

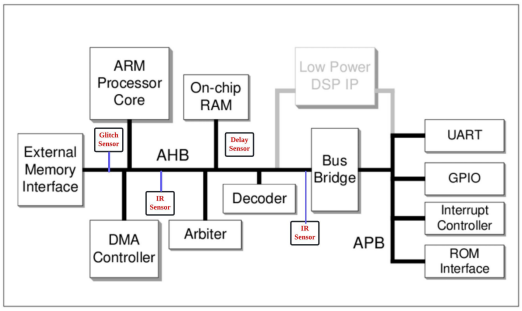


Fig. 28. Arm-SoC with inserted various sensors to capture activities and properties of various modules . [124]

Protecting software execution through hardware on-chip sensor placement involves strategically embedding sensors directly onto the integrated circuits of computer hardware to monitor and detect various aspects of software execution. These sensors can capture real-time data related to temperature, voltage fluctuations, electromagnetic emissions, and other physical characteristics of the hardware environment. By analyzing this data, hardware-based security mechanisms can detect anomalies indicative of unauthorized software execution, such as malicious code injection or runtime attacks. Leveraging hardware sensors offers several advantages, including low-level access to critical system components, reduced susceptibility to software-based attacks, and the ability to operate independently of the software stack, thus enhancing overall system security and resilience.

For detection and protection against several fault-injection attacks, different hardware sensors have been proposed. For instance, Fault-to-time converter(FTC) [125] sensor converts various non-invasive faults to delay and captures the encoded response in ZynQ FPGA. Laser fault injection sensor [126] captures the response of LASER injection into device.

Quantifying security properties of an RTL design and relating them to various injected faults and corresponding violations has been a long discussed issue. Security property driven vulnerability assessment framework against fault injection attacks(SoFI) [127] has been developed to co-relate specific security property violation due to fault injection attacks. How the on-chip sensors respond against faults and how they are related to security property violation has also been discussed [128].

To protect the SW execution using HW sensor response against FIAs, the injection attacks can be modeled in terms of internal quantities such as delay. When SW codes are running into hardware, or in a gate level synthesized design,

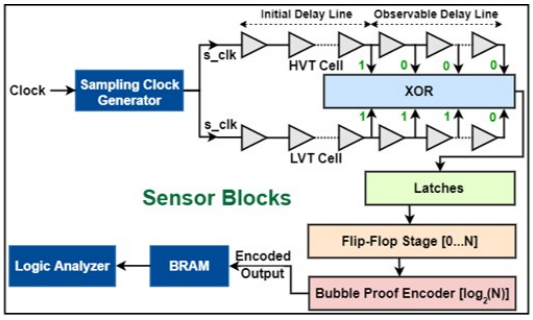


Fig. 29. Fault to time converter sensor. [125]

specific cells of the libraries are being used, each of which are vulnerable to the FIAs defined before. The vulnerability of each cell against each attack can be quantized. When a compiler transforms a high level code(C/C++) into assembly, it can be sensitive to each attack modeled previously. In this way SW execution can be sensitive to HW sensor response and can be protected by redundancy or any other methods. This method is displayed in Figure 34.

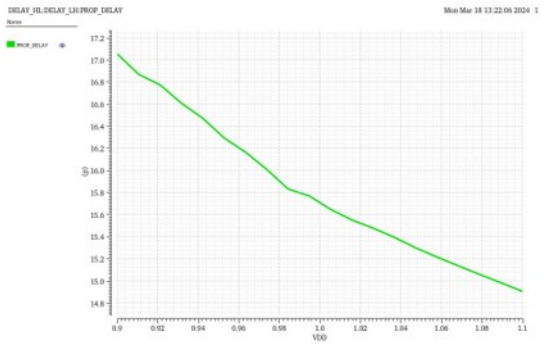


Fig. 30. Propagation delay vs supply voltage variation.

Modeling supply voltage variation involves simulating changes in the voltage supplied to the hardware components, which can occur due to fluctuations in the power supply or deliberate manipulation by attackers. This variation can lead to transient faults, where the voltage drops below the required threshold, causing errors or malfunctions in the system. Several previous research suggested that supply voltage variation can be modeled as a fluctuation in delay(Figure **??**). So, we can add a delay component in the standard cell library that can be activated at a certain time to show the effects of supply voltage variation.

Modeling laser fault injections in standard cells involves simulating the effects of laser-induced faults on the behavior of semiconductor devices within the cells. One approach to achieve this is by adding additional current components to the standard cell models, which represent the changes in device characteristics caused by laser irradiation. Modeling and validation of LFI into hardware involves several steps such as identifying vulnerable locations, defining fault models, integrating current components, simulate LFI attacks etc.

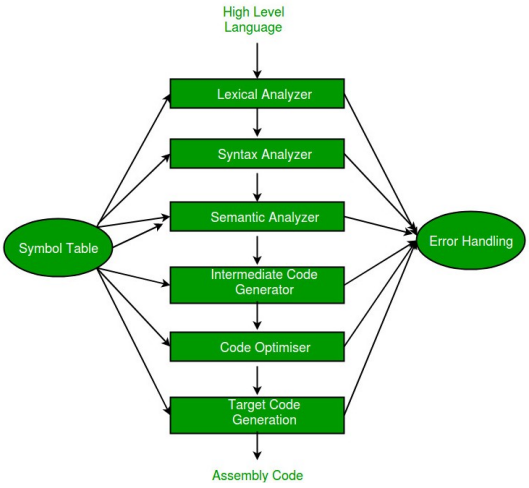


Fig. 31. Steps a compiler performs to translate a high level code to machine language.

The compiler plays a significant role in bridging the gap between software and hardware execution by translating high-level programming code into low-level instructions that can be understood and executed by hardware components. As software developers write code in languages like C, C++, or Python, the compiler analyzes the code, performs optimizations, and generates machine code tailored to the target hardware architecture(Figure 31). This machine code is then executed directly by the hardware, enabling the software's functionality to be realized efficiently. Additionally, modern compilers often incorporate optimization techniques like loop unrolling, instruction re-arrangement, and register relocation to maximize performance and minimize resource utilization.

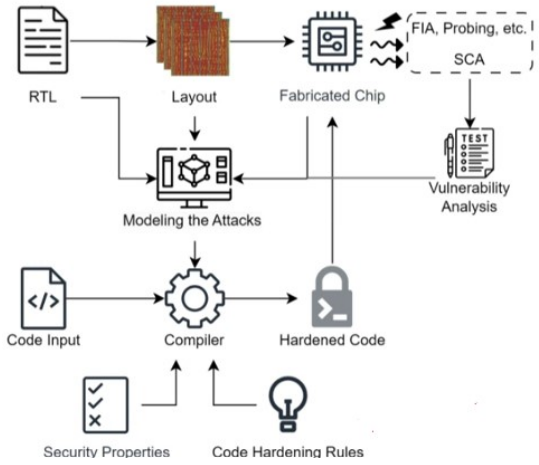


Fig. 32. During compilation, software can be hardened against physical attacks by this framework.

Compilers may play a vital role in mitigating hardware-software vulnerabilities by implementing various security mechanisms and optimizations during code generation. One fundamental approach is through the enforcement of memory safety checks, such as stack canaries, bounds checking, and address space layout randomization (ASLR) [129], which prevent buffer overflows and other memory corruption vulnerabilities. Additionally, compilers can implement control-flow integrity (CFI) mechanisms to detect and prevent code execution hijacking attacks, for instance: return-oriented programming and jump-oriented programming.

We can drive the compiler or generate extra plugins to make it aware of hardware vulnerabilities(Figure 32). The compiler may take the essence of modeling various hardware faults and be aware of hardware execution.

B. Instruction spectrum based software-hardware protection:

When a software runs on a hardware, it creates several property traces on a hardware, such as power, delay variation etc. These traces can be tracked to HW execution strategies and HWs can be made aware of the placement of sensors etc. Modifications of fault injection detection and prevention strategies in the hardware side can be done to prevent any attack that can for example, produce high power traces or any unusual activities during the SW execution.

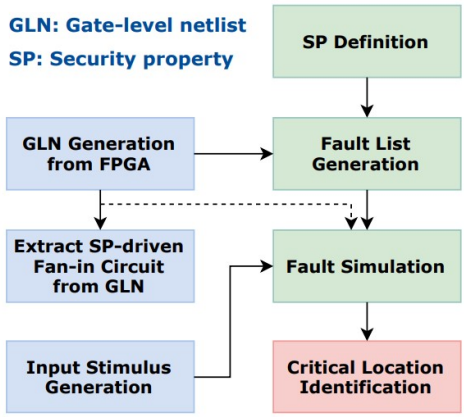


Fig. 33. Critical Location identification on HW using SoFI Framework. [127]

Developing a power model for assembly instructions involves quantifying the power consumption associated with executing each instruction within a processor. By analyzing the power spectrum derived from these models, software execution can be guided to optimize both hardware and software security simultaneously. The power spectrum reflects the power consumption patterns exhibited by different instructions during execution, offering insights into the energy requirements of various software operations.

Leveraging this information, software can be designed or modified to prioritize low-power instructions or sequences, reducing overall power consumption and minimizing the risk of hardware-based attacks, such as side-channel attacks. Additionally, by aligning software execution with the power spectrum, potential vulnerabilities in both hardware and software can be mitigated, as the power consumption characteristics of specific instructions can serve as indicators of potential security risks. This approach not only enhances hardware

security by reducing susceptibility to power-based attacks but also strengthens software security by optimizing execution patterns to minimize exposure to potential vulnerabilities.

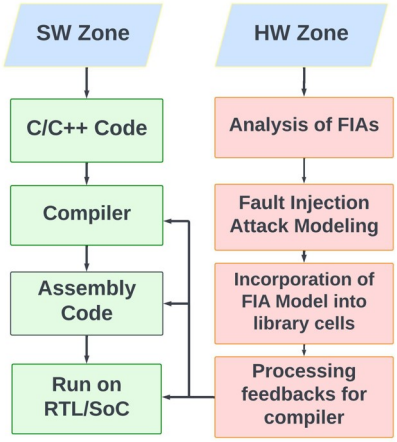


Fig. 34. SW protection by HW sensor feedback against Fault Injection attacks.

Building power model for each type of instruction(such as load,store from memory, arithmetic operations etc) enables us to construct power model for specific applications(Figure 35). If any application, such as matrix multiplication, or convolution operation for a CNN creates stress in the specific part of the hardware by drawing excessive power, we can trace that information in the hardware domain, and send it to the compiler so that software execution is aware of the hardware execution and power trace.

Software modules(such as sensors) running on the system assist in monitoring and analyzing the power consumption patterns. These software components collect power consumption data and perform statistical analysis to identify anomalies or suspicious behavior. They also define and manage security policies based on the observed power spectra and trigger appropriate responses to mitigate security risks.

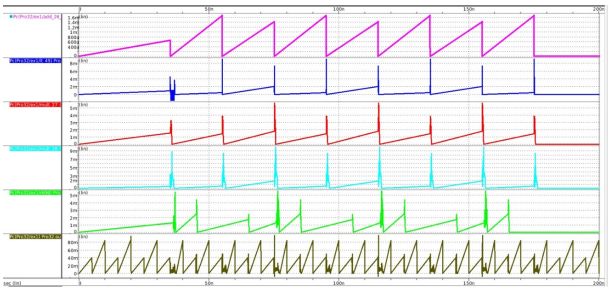


Fig. 35. Power traces of hardware blocks during execution of instructions in a processor and its peripherals.

C. Securing SW execution via monitoring HW Architectural Activity:

Securing software execution through hardware architectural activity is an effective strategy in modern computing systems. By integrating security measures directly into the hardware architecture, such as through hardware-based encryption, secure enclaves, or trusted execution environments, vulnerabilities at the software level can be mitigated more effectively. Hardware-based security provides a robust foundation for protecting sensitive data and critical processes from various threats, including malware, unauthorized access, and tampering.

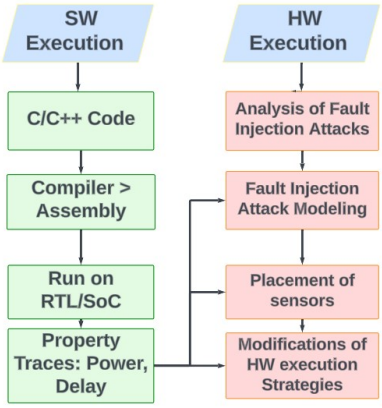


Fig. 36. HW protection by examining property traces during SW execution.

When a SW program runs into HW, such as a processor, different components of the processor gets 'activated' with the execution of instructions. As the execution of instruction sequences correlate with hardware resources such as registers, memory, computing units, corruption in any of the blocks will also hamper SW execution. Corruption in hardware can be in many forms. For instance, a data forwarding unit chooses the data to be put in ALU from execution or memory stage. If the forwarding unit is corrupted, wrong data can be put into the hardware even if we do the correct software execution (Figure 38).

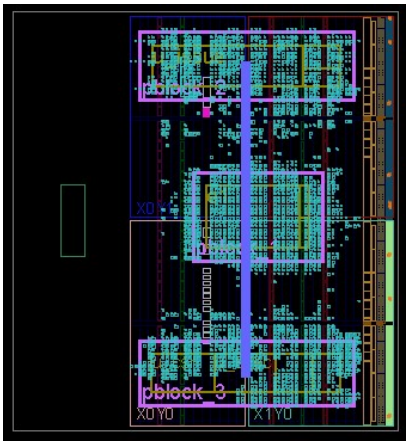


Fig. 37. FTC Sensor placed among various blocks of an SoC and the response is characterized

Hardware architectural activities can be collected via sensors also. In figure 37, the FTC sensor is placed between

different placed parts of a ZynQ SoC that has a core processor and peripherals like UART, SPI, timer etc. The sensor response changes when they are placed closer or further to some blocks those have relatively higher activities. Via placement of sensors and collecting their responses, we can send feedback to the software side that during execution of some particular instructions, some blocks have more vulnerability towards a bit flip or data failure.

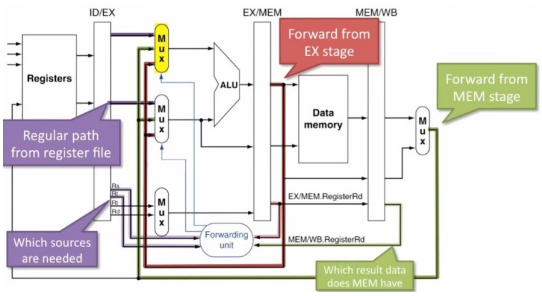


Fig. 38. Simple processor displaying the usage and probable corruption of a data forwarding path.

Securing software execution involves monitoring the activity of distinct hardware blocks within the system to detect and prevent potential security threats. By continuously monitoring the behavior of hardware components such as the CPU, memory modules, and input/output interfaces, anomalous activities indicative of malicious software behavior can be identified in real-time. This monitoring process typically involves analyzing metrics such as resource utilization, data access patterns, and communication protocols to detect unauthorized access attempts, abnormal program executions, or other suspicious activities. By integrating hardware-level monitoring mechanisms into the system architecture, software execution can be safeguarded against a wide range of security threats, including malware infections, code injections, and privilege escalation attacks.

D. Information flow modeling approach for HW/SW Security Verification

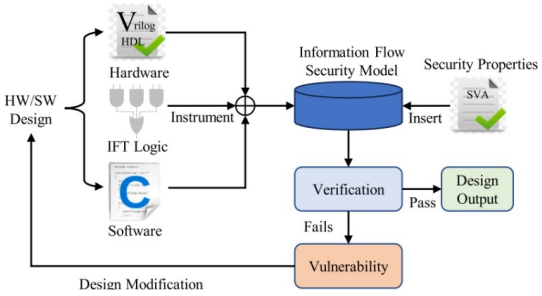


Fig. 39. Proposed design flow of HW/SW co-verification method

Information flow implication method is another approach we consider. Software programs are converted into hardware descriptions using a model and combined with hardware designs to form a logic circuit to track the information flow among software and hardware. So using data security labels, all logical information flows are captured. This flow can be incorporated into CAD verification tools and easily determine the violation of information flow security property, leading to detecting software, hardware, system level security vulnerabilities.

Security properties for HW/SW designs.

#	Security Vulnerabilities for SW/HW Designs	Implementation level	Security Properties	
			Confidentiality: Security assets can not leak to unclassified regions.	Integrity: Untrusted data can not flow trusted zones.
1	malicious/backdoor program	SW	√	√
2	insecure software function	SW		√
3	malicious logic or hardware Trojan	HW	√	√
4	hardware design flaw	HW	√	√
5	system-level hardware Trojan	HW and SW	√	√
6	timing side-channel	HW and SW	√	

Fig. 40. Security properties of HW/SW designs.

VII. Future Work and Conclusion

The exploration of hardware-software co-protection against interactive security threats offers a promising avenue for future research and development in the field of cybersecurity. As interactive security threats continue to evolve and grow in sophistication, it is imperative to develop comprehensive and integrated approaches that combine hardware and software mechanisms to mitigate these threats effectively.

One area for future work is the development of novel hardware architectures and co-design methodologies specifically tailored to address interactive security threats. Sensor based and machine learning based hardware-software property analysis are two prominent directions to protect both hardware and software. Collaborative efforts between hardware and software engineers will be essential to design and implement these advanced security features seamlessly within existing computing systems.

Additionally, future research should focus on the refinement and optimization of hardware-software co-protection mechanisms to achieve a balance between security, performance, and usability. This involves conducting extensive performance evaluations and benchmarking studies to assess the overhead and impact of security mechanisms on system performance, as well as user experience. Furthermore, exploring adaptive and dynamic security strategies that can respond to evolving threats in real-time will be crucial for ensuring the resilience of hardware-software co-protection solutions.

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