

REPQC: Reverse Engineering and Backdooring Hardware Accelerators for Post-quantum Cryptography

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ABSTRACT

Significant research efforts have been dedicated to designing cryptographic algorithms that are quantum-resistant. The motivation is clear: robust quantum computers, once available, will render current cryptographic standards vulnerable. Thus, we need new Post-Quantum Cryptography (PQC) algorithms, and, due to the inherent complexity of such algorithms, there is also a demand to accelerate them in hardware. In this paper, we show that PQC hardware accelerators can be backdoored by two different adversaries located in the chip supply chain. We propose REPQC, a sophisticated reverse engineering algorithm that can be employed to confidently identify hashing operations (i.e., Keccak) within the PQC accelerator – the location of which serves as an anchor for finding secret information to be leaked. Armed with REPQC, an adversary proceeds to insert malicious logic in the form of a stealthy Hardware Trojan Horse (HTH). Using Dilithium as a study case, our results demonstrate that HTHs that increase the accelerator’s layout density by as little as 0.1% can be inserted without any impact on the performance of the circuit and with a marginal increase in power consumption. An essential aspect is that the entire reverse engineering in REPQC is automated, and so is the HTH insertion that follows it, empowering adversaries to explore multiple HTH designs and identify the most suitable one.

CCS CONCEPTS

• **Security and privacy** → **Hardware reverse engineering**; *Malicious design modifications*; **Cryptography**; • **Hardware** → *Application specific integrated circuits*.

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KEYWORDS

Reverse Engineering, Post-Quantum Cryptography, Hardware Trojan Horses, Backdoors, Hardware Accelerators

1 INTRODUCTION

The ability to communicate with people worldwide is the cornerstone of the modern globalized society. It also, in turn, exposes several attack surfaces for security and privacy breach. Public-key cryptographic schemes like RSA and ECC have been protecting us against them for the past two decades. They allow two parties who wish to communicate to start a key exchange over an insecure channel and later switch to a simpler private-key cryptographic scheme. Consequently, several networking protocols, like the Transport Layer Security (TLS) protocol, heavily depend on these schemes.

Despite their current effectiveness, the impending dawn of quantum computers threatens the security of classical cryptographic algorithms. Recognizing this challenge, in 2017, the National Institute of Standards and Technology (NIST) [45] initiated a call for post-quantum Key Encapsulation Mechanisms (KEM) and Digital Signature Algorithms (DSA) to safeguard communications and data exchange in a post-quantum scenario. In early 2023, NIST selected several schemes for standardization, including the lattice-based candidates Kyber [59] and Dilithium [8]. While the standards are currently being drafted, it is important to emphasize that many federal agencies already have mandates for adopting them [22].

PQC algorithms will be gradually deployed in various application domains, and computed on a wide range of software and hardware platforms. While software implementations of PQC offer flexibility and ease of implementation, dedicated hardware platforms like a Field-Programmable Gate Array (FPGA) or an Application Specific Integrated Circuit (ASIC) offer significant speedups¹. FPGAs do offer flexibility since they can be reprogrammed, whereas ASICs deliver significantly higher performance than FPGAs but are static in nature and cannot be reprogrammed. For example, the FPGA implementation reported in [4] outperforms the Cortex-M4 one reported in [17] by 363×. Various FPGA-based accelerators are described in [3, 4, 6, 10, 11, 14, 15, 17, 19, 20, 24, 29, 35, 44, 56, 57, 62, 65]. Similarly, hardware accelerators tailored for the ASIC platform are reported in [9, 15, 24, 30–32, 61, 64]. For the time being, while the transition to PQC is taking place, FPGAs are suitable platforms.

¹This was true for classical cryptography and remains true for PQC.

Once standards are finalized and widely adopted, ASIC designs will be more advantageous since they display smaller area footprint, low power, and higher performance.

For the secure implementation of PQC schemes, we must consider several attack scenarios. Flaws in the protocols or underlying mathematical assumptions can render a cryptographic scheme *weak*. For example, [18] reports an attack on an isogeny-based PQC scheme, leading to its exclusion from NIST’s consideration. Assuming the schemes have withstood scrutiny and are mathematically sound, their hardware implementations may still be vulnerable to side-channel analysis (e.g., SPA, DPA) or fault attacks. These attacks vary in the level of intrusiveness – in principle, side-channel attacks can be performed even remotely [63] whereas fault attacks require physical access to the device under attack. The Deep Learning attack on Kyber [33] is an example of a side-channel attack on an otherwise mathematically sound scheme that succeeds, as expected.

There are several known techniques to protect against side-channel and fault attacks [1, 2, 12, 23, 46, 55]. These techniques were developed for classical cryptography but, in general, can be applied to PQC hardware as well. However, one key assumption remains: the hardware accelerator is assumed to be conceived in a trusted supply chain. This paper assumes an opposing view: **the supply chain is vulnerable** and may contain rogue elements interested in compromising cryptographic chips. In particular, PQC-capable chips are vulnerable as well. Our study focuses on accelerators intended for ASIC platforms since those have stringent security requirements while also having ambitious power/timing/area requirements. To be precise, the threat we are considering in this paper is that of a **Hardware Trojan Horse (HTH) inserted into an ASIC PQC accelerator**. We will show that reverse engineering such accelerators can be done by locating their hashing building block, i.e., Keccak.

From the point of view of an adversary attempting to mount an HTH attack, many challenges appear [13]. In order to be successful, the adversary must decide the HTH’s location (‘where’) and the HTH’s insertion form (‘how’), concepts which we term *node localization* and *HTH insertion*, respectively. *Node localization* involves determining the optimal insertion point knowing that the adversary does not necessarily enjoy a full understanding of the design. Having to mount an attack into a sea of unnamed logic gates is far from trivial. For *HTH insertion*, on the other hand, the adversary has to play a difficult balancing act between detection and attack success: the more logic the HTH design requires, the more sophisticated the attack may become. However, the larger the footprint of the HTH is, the more susceptible to detection it will become. Additionally, a large HTH is harder to fit into the original design without altering its characteristics.

Node localization can be achieved via reverse engineering approaches that group and classify gates. If successful in his/her reverse engineering effort, the adversary can mount very precise and effective attacks. As for *HTH insertion*, automation is key. However, we highlight that automated insertion of HTHs is an area of active study for which there are no general solutions, neither for classical cryptography nor for PQC. We will show that the complexity of PQC hardware and the unique attributes of one of its building blocks, Keccak, allow us to make clever observations leading to a

Table 1: Comparison of related works.

Reference	Node localization	HTH insertion	PQC specific
[54] *	Manual	Manual	✓
[42, 52]	Manual	Manual	×
[25]	Manual	Manual	×
[27]	Automated	Automated	×
[28] †	Manual	Manual	✓
[49, 50]	Manual	Automated	×
This work	Automated	Automated	✓

* Assumes 3PIP setting. † Assumes a SW/HW attack.

feasible attack strategy. In other words, the main idea put forward in this work is that specialized hardware for PQC is **not immune** to many supply chain-related threats, including reverse engineering and subsequent HTH insertion.

1.1 Related Works on HTHs

The study of compromising cryptographic primitives through HTHs has garnered considerable attention among researchers. This active line of research is adversarial in nature, where security experts mount attacks to comprehend the real capabilities of an adversary. Ravi *et al.* [54] were among the first to propose malicious logic that targets PQC hardware. However, their threat model considers only the Third-Party Intellectual Property (3PIP) setting, where a PQC hardware IP is bought from a malicious third party and comes with a backdoor already inside. Their attack was mounted on FPGA-based accelerators for Kyber and Saber.

In [52] and [42], the authors used a notion of a blue-team versus red-team for HTH detection, where the red-team fabricated a compromised ASIC, and the blue-team was responsible for analyzing it and finding the HTH [42]. In [52], this existence of an HTH is *emulated*. These two works enormously contribute to the field, providing a solid foundation for detecting HTHs through physical inspection. In [25], Ghandali *et al.* devised an HTH that makes a masked hardware implementation of a symmetric-key scheme, PRESENT [16], behave as if it is not masked by violating timing margins almost on demand.

Hepp *et al.* [27] proposed a generic methodology for HTH insertion based on the relative ‘importance’ of ASIC gates, leveraging reverse engineering tools. In [28], Hepp *et al.* described four different means to compromise a PQC hardware accelerator. Two of those require malicious software to trigger the HTH. All four Trojans are inserted manually. Perez *et al.* [49, 50], described how to leverage an existing feature in chip design tools called the Engineering Change Order (ECO) flow, for HTH insertion. Remarkably, the authors of [28, 49, 50] also validated their results on an HTH-compromised fabricated chip. A summary of the many characteristics of related works is given in Tab. 1. Notice how automation is rarely present. Furthermore, the few works that display automated HTH insertion are very recent developments.

1.2 Novelty and Contributions

Novelty. This is the **first** paper to propose an automated approach to backdoor PQC hardware accelerators, including the steps of node localization and HTH insertion.

Being so, this work opens up new perspectives for reverse engineering and backdooring PQC hardware implementations. To this end, our contributions are as follows:

- **Contrast between different attackers concerning design and fabrication-time adversaries.** We provide a contrast between different attacks in the supply chain and how they can compromise a chip. For this, we consider a design-time adversary A-IP and a fabrication-time adversary A-FO, both capable of backdooring a PQC accelerator (see Section 3).
- **First automated method for PQC backdooring.** We propose the first approach for automated node localization and HTH insertion in PQC hardware. It consists of a tool termed **REPOC** and a specific **HTH architecture**. REPOC is an open-source tool we propose for reverse engineering ASIC PQC hardware accelerators. Moreover, we offer a novel HTH architecture that, when mounted on a Dilithium implementation, gives the adversary a message-controlled trigger and leaks the long-term key of the digital signature scheme (see Section 4).
- **Descriptive result evaluations.** We support our work with results and layouts of several HTH-compromised 28nm ASIC implementations of hardware accelerators for Dilithium (see Section 5).

2 BACKGROUND

In this section, we briefly describe all the elements involved in our attack, including a brief overview of PQC and the target algorithm of our attack – the NIST-selected DSA scheme Crystals-Dilithium [8]. Within this signature scheme, we target the hashing of secret values performed using Keccak. Our background explanations also cover the basics of reverse engineering and HTHs.

2.1 Post-quantum Public-key Cryptography

KEM and DSA schemes help two parties to initiate a key-exchange; this shared key is then utilized to encrypt/decrypt communication packages. A KEM helps to encapsulate or decapsulate a shared key and a DSA scheme allows senders to sign their encapsulated packages for authenticity. Public-key schemes are also often called asymmetric schemes because the encapsulation/decapsulation or sign/verify keys are distinct. These asymmetric schemes typically have very large key and ciphertext components with respect to their symmetric counterparts. Hence, this exchange is expensive in terms of time and memory and is only done once at the beginning of a communication.

The KEM-related secret key can be refreshed as and when required. On the other hand, the DSA-related secret and public key pairs are long-term and require validation from a certifying authority every time they are changed. If an attacker gets ahold of a user’s digital signature secret key, they can pretend to be the user (i.e., impersonation). It can also lead to other critical attack scenarios like man-in-the-middle attacks, where the attacker can conveniently listen to a conversation and gain critical information. Thus, it is crucial that the authentication is protected and does not leak any information.

In the current classical scenario, standardized schemes based on RSA and ECC provide this functionality. These schemes are based on specific computationally hard problems. However, these

Algorithm 1 Signing of Dilithium [8], simplified

Input: Secret-key $sk = \{\rho, K, tr, s_1, s_2, t_0\}$, and msg M

Output: The signature (z, h, \bar{c})

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1:  $A = \text{ExpandA}(\rho)$ 
2:  $\kappa = 0, (z, h) = \perp$ 
3:  $\mu = \text{Hash}(tr||M)$  ▷ M will serve as trigger
4:  $\rho' = \text{Hash}(K||\mu)$  ▷ K is to be leaked
5: while  $(z, h) = \perp$  do
6:    $y = \text{ExpandMask}(\rho', \kappa)$ 
7:    $w = A \cdot y$ 
8:    $w_1 = \text{HighBits}(w, 2\gamma_2)$ 
9:    $\bar{c} = \text{Hash}(\mu, w_1), c = \text{SampleInBall}(\bar{c})$ 
10:   $z = y + c \cdot s_1$ 
11:   $r_0 = \text{LowBits}(w - cs_2), 2\gamma_2$ 
12:  if  $\|z\|_\infty \geq \gamma_1 - \beta$  or  $\|r_0\|_\infty \geq \gamma_2 - \beta$  then
13:     $(z, h) = \perp$ 
14:     $\vdots$  ▷ Omitted operations
15:  end if
16: end while
17: return  $(z, h, c)$ 

```

problems can be solved with ease on a quantum computer². Although quantum computers still need to be stronger to break the classical schemes, experts believe it is only a matter of time. Realizing this, NIST launched a standardization call for secure KEM and DSA in a post-quantum scenario. The PQC NIST competition, as it became known, culminated in 2023 with Kyber [59], Dilithium [8], Falcon [51], and SPHINCS+ [7] declared as winners. Out of these, lattice-based schemes Kyber and Dilithium are considered most compatible for applications that require both functionalities, like the TLS protocol. In this work, we recover the secret key of Dilithium. Hence, we present a brief description of this scheme.

Dilithium. The computational hardness of Dilithium relies on the Module Learning With Errors and Module Short Integer Solution problems. It has three basic functionalities: key generation, signing, and verification. From an attacker’s perspective, the most worthwhile operation to compromise is the signing operation. This is because key generation does not happen frequently and offers less opportunity for attack. On the other hand, the verification procedure requires only the public key, thus presenting zero opportunity for a key-recovery attack. Signing is the only operation that happens frequently and involves the secret key. For more details, please refer to [8].

A simplified signing procedure is described in Alg. 1. The secret consists of various components, including ‘ K ’, which is used to generate a pseudo-random string essential for the subsequent generation of polynomial ‘ y ’ (Steps 4 and 6). Then, we compute ‘ z ’ (Step 10), which serves as the output—an LWE sample whose security relies on the secrecy of ‘ s_1 ’ and ‘ y ’. However, it is crucial to note that knowledge of y alone can potentially lead to the disclosure of information about the secret polynomial s_1 , making it susceptible to signature forgery. The authors in [21] show that knowledge of s_1 is sufficient to break the security of the scheme. Consequently,

²Technically, a cryptanalytically relevant quantum computer capable of executing Peter Shor’s algorithm is required.

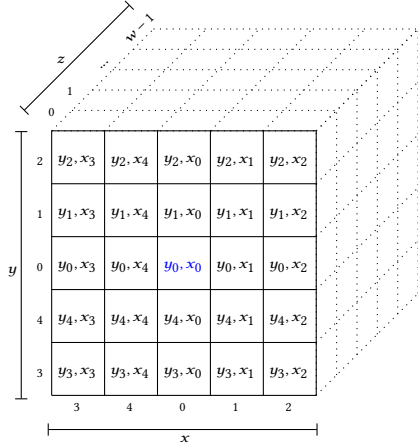


Figure 1: Keccak state as a $5 \times 5 \times 64$ 3D matrix, for keccak-f[1600]. Each box in the Keccak state represents one bit.

this presents an interesting attack surface. To obtain y , an attacker would only need to know K , which undergoes processing by the Keccak hash function (Step 4). This will allow the attacker to know ρ' and consequently y . Using this, the attacker can recover s_1 from Step 10. This observation leads us to the possibility of devising a clever HTH that uses ‘ M ’ as a trigger to leak ‘ K ’ – the details are given in Section 4.2.

Keccak. Keccak [48] is the core of NIST-standardized [43] Secure Hash Algorithm-3 (SHA-3). Keccak is a “sponge” function, which absorbs the input data and then “squeezes” a digest. It can also be used as an Expandable Output Function (SHAKE), where it absorbs a small seed and produces a long string of pseudo-random bits. On the other hand, in the hash function mode (SHA-3), Keccak absorbs a large input data and then outputs a brief digest (hash output). For Dilithium, Keccak is employed in four modes: SHA-3/256, SHA-3/512 variants for hashing; and SHAKE128, SHAKE256 for pseudo-random number generation.

At the core of Keccak is its permutation function denoted as keccak-f[b], where $b = 25 \times 2^l$ and $0 \leq l \leq 6$. The keccak-f[b] is defined over $s \in \mathbb{Z}_2^b$, where b represents the width of the permutation. In essence, the permutation used in SHA-3 variants can be configured with different parameters, including capacity, rate, etc. For more detailed information, we refer readers to [43, 48]. The keccak-f[b] permutation operates on a state a that is defined as a three-dimensional array denoted as $a[5][5][w]$, where $w = 2^l$. For the maximum permutation width (keccak-f[1600] and $l = 6$), w is equal to $2^6 = 64$. Consequently, the state a is represented by a three-dimensional array with dimensions of $[5][5][64]$. A visual representation of the state a is provided in Fig. 1. It is worth mentioning that a single permutation computation in Keccak relies on $12 + 2 \times l$ rounds, each round comprising a combination of five linear and non-linear steps, namely $\{\theta, \rho, \pi, \chi, \iota\}$ [43].

2.2 Reverse Engineering

Reverse Engineering can be defined as the process of creating a *representation* of a piece of hardware by someone other than the original designer(s). In other words, it is the process of making sense

of an Integrated Circuit (IC) without *a priori* knowledge about its implementation. IC reverse engineering has two sides to it: physical and logical. On the physical side, many studies have disclosed how to perform product tear-down, IC sample preparation, delayering³, imaging⁴, and stitching⁵ of the acquired images to reconstruct the layout of a circuit. This process has many challenges [38], including the precision of the delamination, the throughput and resolution of the imaging, and the quality of the stitching.

However, in this work, we are not dealing with these physical requirements since our adversary possesses a perfect representation of the layout. This becomes clear in our threat model in Section 3, when we reveal that our adversary is a foundry engineer. In this work, we are dealing with logical reverse engineering: assuming a layout has been acquired and transformed into a netlist (schematic), one still has to comprehend it since the obtained netlist is rather opaque to a human. In order to attempt to give meaning to ‘blind’ netlists, different analytical approaches can be applied. A typical first step is netlist partitioning, primarily for the sake of making the problem tractable. Any partitioning solution that aids in the understanding of the design is a good partitioning. A further approach is the separation of datapaths from control logic. RELIC [39, 40] is a prime example of a tool for this task. It builds on the observation that wires in the control logic tend to have a non-repeatable *structure*, whereas wires in a datapath will have a structure similar to other wires of the same word. RELIC’s approach is not perfect, but it tends to be rather insightful. In Appendix A, we provide examples of distributions that illustrate the output of RELIC’s analysis.

Another classic problem in logical reverse engineering is register grouping [5]. The problem can be summarized as follows: for a netlist containing N individual flip-flops, how to best arrange N into registers that have the same properties? For instance, in a circuit that has a 64-bit datapath, one would be inclined to look for 64-bit registers that hold the input data to a 64-bit operation. Register grouping can be performed based on similarity, as discussed in [36].

Reverse engineering tools can be used for benign and malicious purposes and, in this work, we will use a *cocktail* of these tools for the purpose of *node localization*. Once nodes of interest are found, we then proceed with HTH insertion.

2.3 Hardware Trojan Horses

For decades, the IC industry has continuously become more and more distributed and globalized. Consequently, no IC design today is conceived by a single company and many entities are involved in what has been termed the fabless model. In this model, design-related activities are handled by fabless design houses while the fabrication is handled by a third-party silicon foundry⁶. The design house is the rightful IP owner but it has no oversight or control claim over the fabrication process. In other words, the fabrication process is considered untrusted by definition, and it is precisely at fabrication time that HTHs can be inserted.

HTHs have been studied for nearly two decades now, which has yielded a well-established taxonomy [13] and a database [58].

³Delayering or delamination is the process of removing the layers of a chip one at a time. It often is performed with chemical etching.

⁴Imaging processes based on SEM or X-ray are typically employed.

⁵Stitching is the process of aligning the many individual images.

⁶This is an oversimplification that abstracts away post-fabrication steps.

Among the many forms an HTH may take, additive HTHs stand out. Those are pieces of logic added on top of the original circuit design, hence the name. They may leak some secret information directly via a primary output of the chip, or simply cause the chip to stop working altogether, akin to a Denial of Service (DoS) attack. A specialized form of an additive HTH is a **side-channel HTH** that induces a controlled/modulated amount of power consumption through which information can be leaked. This HTH style has been analytically described in [37] and demonstrated as silicon-viable in [50]. By definition, a side-channel HTH is harder to detect since no primary outputs of the chip are used for information leakage. Hence, we will adopt the side-channel style of HTH due to its proven viability and inherent stealthiness.

Conceptually, HTHs have two components: a trigger and a payload [13]. The trigger is the logic that determines *when* the malicious activity should start. A ‘good’ trigger is one that is stealthy in the sense that only the adversary can reasonably (and deterministically) activate it. Examples of reasonable triggers are comparators and counters. The payload, on the other hand, is the component that determines *how* the HTH will interfere with the chip’s functionality. The most basic form of a payload is an XOR gate that flips some signal of the original design at will, thus corrupting the underlying computation. Ring oscillators [50], shift registers [27], and even antennas [34] can be considered as payloads for these HTHs as they can demonstrate modulated power consumption.

A distinction between hardware backdoors and HTHs is not always clear in the literature. A hardware backdoor tends to be inserted by someone at design time leading to compromised code or 3PIP [54]. On the other hand, the term HTH tends to refer to malicious logic inserted at fabrication time, as in [50]. We will consider both scenarios in our work and refer to them solely as HTH for the sake of simplicity.

3 THREAT MODEL

In this work, we consider two adversarial settings, namely the 3PIP and the untrusted foundry settings. We term the adversaries associated with these as A-IP and A-FO, respectively. The presence of these two adversaries in the IC design flow and supply chain is shown in Fig. 2.

The design flow depicted in Fig. 2 can be understood as a series of transformations. Logical synthesis is the process of translating a human-readable description of a design in hardware description language into a schematic of interconnected logic cells (AND, OR, XOR, flip-flops, etc.). Physical synthesis converts these logically connected cells into a physical representation, that is, a layout of the chip. Finally, fabrication transforms a layout into a physical device. Notice that once an artifact is compromised in this chain of transformations, the subsequent representations remain compromised.

A-IP is an external adversary that has provided a compromised IP to an honest design house. Such an IP is assumed to be a source code described in a hardware description language. This adversary must have a fair understanding of PQC in order to compromise a PQC hardware accelerator. However, he/she does not need to understand reverse engineering techniques or backend design since, to him/her, the design is transparent and human-readable.

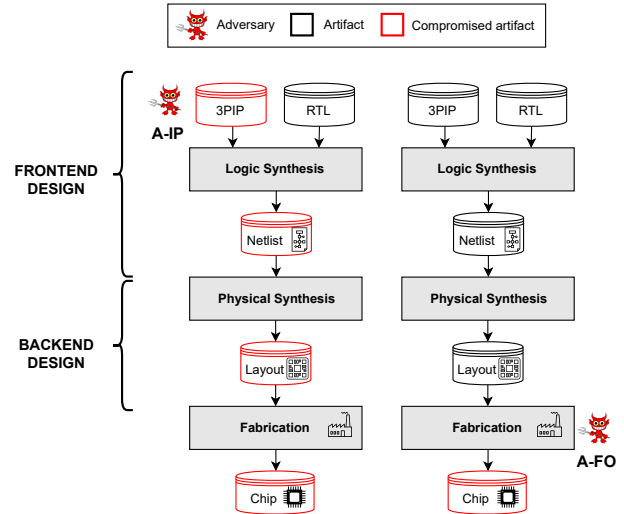


Figure 2: Locations of the adversaries A-IP and A-FO in the supply chain and design flow.

Contrary to this, A-FO is a foundry engineer that has the means to modify the layout before it goes into production. A-FO can also convert the layout to a netlist representation with ease [53]. Furthermore, A-FO should have: (i) a good understanding of PQC algorithms, (ii) reverse engineering skills, and (iii) advanced chip design skills. For (i), since the PQC algorithms are open and standardized, the adversary may have advanced knowledge about their requirements and what their building blocks are. For (ii), the adversary can adopt REPQC, the contribution of this work. For (iii), we assume the A-FO adversary is as skilled as the rogue engineer described in [50], in line with the assumptions made in most of the HTH literature. We further assume A-FO performs HTH insertion via the ECO flow.

On the surface, one might assume that A-IP is a more powerful adversary than A-FO. However, A-IP has a severe disadvantage: the compromised artifact generated by A-IP appears very early in the flow. Being so, many detection approaches are applicable, including verification by simulation, information flow tracking, and taint analysis. None of those approaches apply to A-FO. Only physical inspection of a (suspicious) chip can guarantee detection, but physical inspection of fabricated chips is neither cursory nor cost-efficient.

Next, we define what the trigger and the payload ought to look like in the HTHs inserted by A-IP and A-FO.

Trigger definition. We assume the trigger is the message M (or part of it), as highlighted in red in line 3 of Alg. 1. The adversary can select any message M of his/her liking for this purpose. The same assumption is made for A-IP and A-FO. Physically, the trigger logic is a comparator.

Payload definition. For the payload, we assume both adversaries are going to insert malicious logic that can modulate power consumption on demand in order to enable side-channel leakage. This is achieved by modulating power based on the value of K , as highlighted in red in line 4 of Alg. 1. Physically, the payload is a ring oscillator.

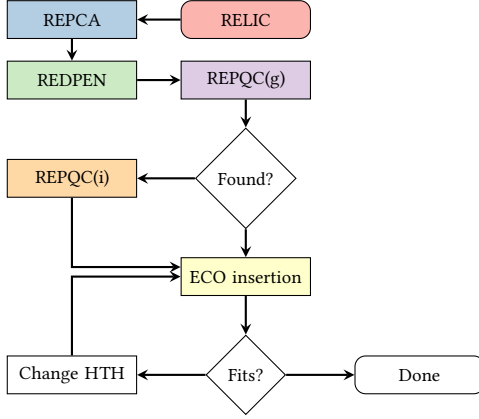


Figure 3: Flowchart of the entire attack.

Notice that, although the definitions above imply that the adversaries possess knowledge about the PQC algorithm, they do not have any *a priori* knowledge of the circuit under attack.

4 OUR PROPOSED REPQC TOOL AND HTH ARCHITECTURE

Let us first refer again to Fig. 2 before describing our proposed REPQC tool and HTH architecture. Note that only A-F0 has to perform RE since the entire design is transparent to A-IP. A-F0, on the other hand, has to identify where the two elements (M , K) exist in the design blindly, possessing only a netlist where the nodes have no name or any otherwise identifying characteristic. Hence, in this section, we describe an approach to empower the adversary A-F0 with as much knowledge about the design as that possessed by A-IP.

For this, we use a cocktail of RE tools: RELIC \rightarrow REPCA \rightarrow REDPEN \rightarrow REPQC. The first three are from the NETA suite [40], whereas REPQC is the main contribution of this paper. These tools are chained together as described in Fig. 3.

NETA-suite Reverse Engineering Tools. In Fig. 3, RELIC takes as input a design netlist and produces a list of flip-flops ordered by Z-score. The Z-score ($\in [0, \infty)$) is a measure of how much a flip-flop is likely to be part of the control (or data) path of a design. The higher the value, the more likely the flip-flop is unique and, therefore, part of the control logic. The closer the number is to zero, the more likely the flip-flop is part of the datapath. Examples of RELIC’s output are in Appendix A.

REPCA takes as input the same netlist and produces a list of groups of flip-flops, which we term registers. If REPCA does a good job, these registers should match the high-level registers in the original design description. REDPEN, a much simpler RE tool, takes a netlist as input and identifies all flip-flop dependencies. For example, if at any given clock cycle c_i , the content of a flip-flop f_1 depends on flip-flop f_2 at c_{i-1} , there is a dependency $f_2 \rightarrow f_1$.

RELIC and REPCA make use of the concept of features for assigning Z-scores and groupings to individual flip-flops. These features are varied and can be combined for making a recipe. The default recipe in NETA makes use of 20 features together. In our experiments, we use much more modest (and yet sufficient) recipes. Our

Algorithm 2 REPQC

Input: *file.scores*, *file.groups*, *file.deps*

Output: List of flip-flops that carry M and K

```

1:  $FFs \leftarrow parse(file.scores)$ 
2:  $GROUPs \leftarrow parse(file.groups)$ 
3:  $DEPs[] \leftarrow parse(file.deps)$ 
4: for each  $f \in FFs$  do
5:   if  $f.fanin/out \notin [FIF, FIC]/[FOF, FOC]$  then
6:      $FFs.remove(f)$ 
7:   end if
8: end for
9: for each  $f \in FFs$  do
10:  for each  $reg \in GROUPs$  do
11:   for each  $member \in reg$  do
12:    if  $DEPs[f, member]$  then
13:       $member.hit \leftarrow TRUE$ 
14:       $reg.hits \leftarrow reg.hits + 1$ 
15:    end if
16:   end for
17:  end for
18: end for
19: for each  $reg \in GROUPs$  do
20:  if  $reg.hits < 64$  then
21:     $GROUPs.remove(reg)$ 
22:  else
23:    for each  $member \in reg$  do
24:   if  $member.hit == FALSE$  then
25:     $reg.remove(member)$ 
26:   end if
27:  end for
28: end if
29: end for
30:  $sort(GROUPs)$ 
31: return  $GROUPs[0].members$  ▷ ranked by Z-score
  
```

RELIC recipe has only one feature: FANOUT. Our REPCA recipe has two features: INPUT and OUTPUT. The meaning of these features is explained in detail in the NETA repository [41]. Our choice of these simple features is discussed in Section 4.1.

4.1 Our Proposed Tool: REPQC

First, let us start with a high-level description of REPQC as given in Alg. 2. REPQC takes as input three files that correspond to the Z-scores from RELIC, the groups from REPCA, and the dependencies from REDPEN. The Z-scores for each flip-flop are stored in the FFs list, $GROUPs$ list stores the groups, and the map $DEPs[]$ stores dependencies.

The first step is to filter out flip-flops of interest. The goal is to find the flip-flops that implement the Keccak state a USING their fanin and fanout properties. For a given flip-flop f , its fanin and fanout are the numbers of flip-flops in FFs for which there is a dependency $f_i \rightarrow f$ and $f \rightarrow f_i$. Note that this is the definition of sequential fanin/fanout. Next, for every flip-flop in the design, we check whether the fanin and fanout are between the respective floor and ceiling, i.e., $[FIF, FIC]$, $[FOF, FOC]$ (line 5).

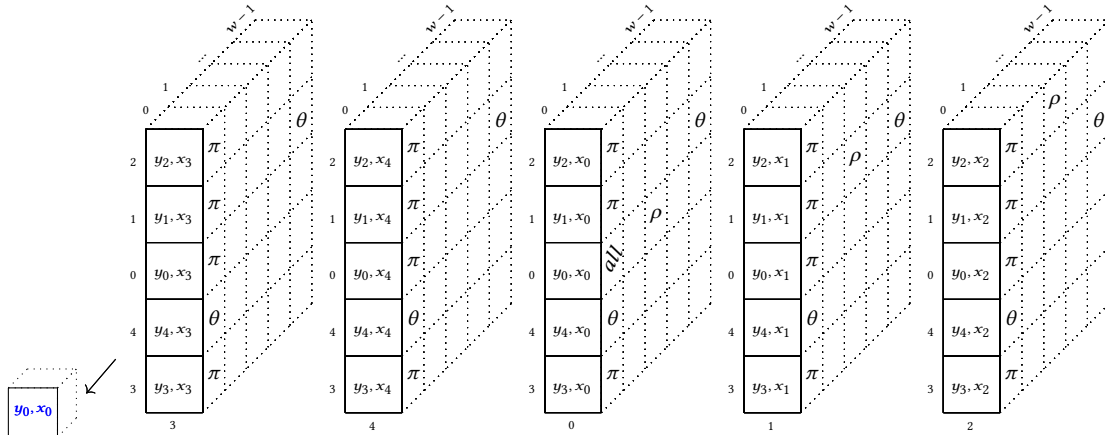


Figure 4: The element $a[0][0][0]$ is being updated and every other element for which there is a dependency is marked with the permutation function that creates the dependency. There are 33 dependencies in total.

Reasonable assumptions for these four constants can be determined primarily from analyzing the Keccak specification. The Keccak state, as shown in Fig. 4, is assumed to be implemented as a single register with 1600 flip-flops. Due to the iterative nature of the Keccak rounds, the state updates itself after every iteration by applying the round functions $\{\theta, \rho, \pi, \chi, \text{ and } \iota\}$. For keeping the Keccak hash operation secure, the state cannot be arbitrarily connected to random flip-flops. The connections must be such that the Keccak state can be loaded, processed (permuted), and read.

In Fig. 4, we show how bit $a[0][0][0]$ is updated after one round. Notice that the new value of $a[0][0][0]$ depends on exactly 32 other elements of a and itself. Hence, the *FIF* value is at least 33. Similar assumptions can be made for *FOF*, where the permutation logic determines, assuredly, that 34 dependencies exist. The actual fanout number may be higher because the Keccak state flip-flops may be connected to other units of the accelerator. In other words, 34 can be interpreted as a floor for the actual number of fanouts (*FOF*).

With these assumptions in place, a very large portion of the design flip-flops are immediately rejected as Keccak state candidates. Next, we use the notion of a ‘hit’ to find flip-flops that are inputs to Keccak. In order to identify the Keccak input, we compare every surviving candidate flip-flop against all groups. If a dependency is found, the group member is marked with a hit (line 13) and the number of hits associated with a group *reg* is incremented by one (line 14). As a reminder, our attack does not aim to compromise Keccak itself. Our goal is to use Keccak as an anchor for RE. This is visualized in Fig. 5. It is the input to Keccak that is of interest since it may hold the message M that is the trigger for the HTH. The input also holds the component K that we wish to leak.

Next, REPQC looks at the groups of interest. A group that has received less than 64 hits is not a reasonable candidate (line 20) because the input to Keccak is, by definition, 64 bits wide. For groups that have more than 64 hits, we have to check where these hits come from. Any member of a group that was never ‘hit’ by a candidate flip-flop is eliminated since it cannot be an input to Keccak (line 25). After all bad candidates are eliminated, the groups are sorted by their Z-score (line 30), and finally, the 64 lowest-scoring elements

of the lowest-scoring group are returned (line 31). For more details and optimizations, we refer the readers to our repository [47].

Fig. 5 shows the high-level objective of REPQC: finding the dark blue flip-flops based on the properties of the light blue flip-flops.

RELIC Features utilized in REPQC. For assigning Z-scores to flip-flops, the only feature we use is FANOUT. Meaning that flip-flops are compared against others based on their fanouts, and this determines whether a flip-flop is more data- or control-oriented. The insight here is that the permutation functions create regular and distinctive feedback from the Keccak state to itself (see Fig. 5), and this is captured by the FANOUT feature.

For grouping, we make use of the INPUT and OUTPUT features. These determine the sequential distance a given flip-flop has to primary inputs and outputs. It can be interpreted as the number of clock cycles it takes for a flip-flop to drive a primary output or to be reached by a primary input. Grouping flip-flops based on these features is similar to levelization. Notice from Fig. 5 that if the Keccak input register is assigned to a level L_i , the Keccak state should be in L_{i+1} .

Dealing with Imprecise Grouping. Locating the Keccak input is relatively harder than locating the state: when grouping flip-flops as registers, non-ideal clustering may cause Alg. 2 to return an empty list. For example, if the 64 flip-flops of interest get grouped into two registers of 32 elements each. This is a well-understood problem in RE and has also been reported in related works [60]. In order to tackle this issue, we propose two variants of the REPQC algorithm, REPQC(g) and REPQC(i), where *g* stands for groups and *i* stands for individuals. REPQC(g) matches the algorithm described in Alg. 2 while REPQC(i) assumes groups with a size of 1, which in practice is the same as performing individual flip-flop comparisons. The REPQC(i) variant is more time intensive because it cannot eliminate entire groups at a time (line 20 of Alg. 2 is therefore not considered).

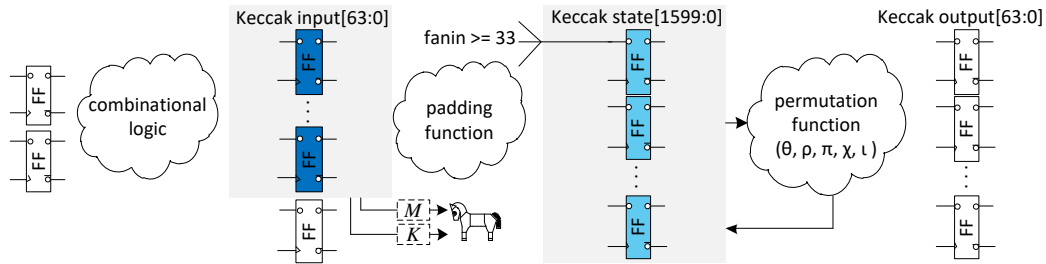


Figure 5: The Keccak state is composed of 1600 flip-flops that have predictable fanin/fanout properties. The goal is to find a register with 64 flip-flops that is the input to Keccak and therefore holds the message M and the component K .

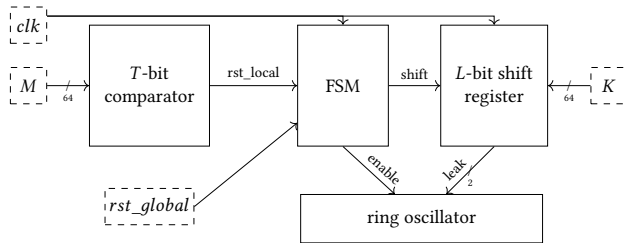


Figure 6: High-level diagram of the HTH.

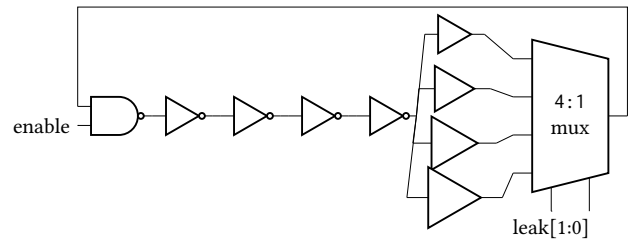


Figure 7: Schematic of the ring oscillator. The different-sized BUFFs modulate the frequency and power consumption.

4.2 HTH Architecture

First, let us describe the chosen HTH architecture, which is amenable to both high-speed and lightweight PQC accelerators. The high-level diagram of the HTH architecture is depicted in Fig. 6 and is employed by both A-IP and A-FO adversaries. The inputs M , K , clk , and rst_global are marked with dashed boxes. The HTH consists of a multi-bit comparator, a control logic implemented by a Finite State Machine (FSM), a shift register, and a ring oscillator.

Working principle. The HTH awaits for a carefully selected message M to be sent for hashing (line 3 in Alg. 1). Once this happens, the HTH is triggered and the FSM is reset using rst_local . Knowing that K will be hashed next (line 4 in Alg. 1), the FSM loads K before it gets fully absorbed by Keccak. Next, the FSM activates the ring oscillator via its $enable$ pin. The content of the shift register is shifted whenever $shift$ is asserted. At every clock cycle, two bits of K appear on $leak$. The FSM stops after the shift register is empty.

For scalability, the HTH has two parameters, T and L , where T determines the size of the trigger (which determines the comparator size). The parameter L determines the size of the shift register, meaning how many bits of K will be stored before they are leaked. The higher the values of T and L , the bigger the HTH. K can also be leaked in parts that can be indexed using leftover bits of message M . So the buffer storing K can be extremely small or large depending on the bits it has to leak. This flexibility enables concealed trojan insertion in not just high-speed but also extremely lightweight designs. In our repository, we provide all combinations of $T = \{16, 32, 64\}$ and $L = \{16, 32, 64\}$ for nine HTHs that leak entire secret K at once. In the results that follow, we set $T = 64$ without loss of generality since this is the largest and most difficult HTH to insert.

Fig. 7 illustrates details of the ring oscillator depicted in Fig. 6. By far, the ring oscillator is the most important part of the payload of the HTH. The proposed ring oscillator is capable of tuning its own frequency: depending on the value of $leak$, different paths will be multiplexed for the feedback path of the oscillator. By selecting different paths, the frequency of oscillation becomes modulated by $leak$, and so does the power consumption of the oscillator. This is used by the adversary to leak information via a (power) side channel. More details about the operation of the oscillator are given in Appendix B.

5 RESULTS AND DISCUSSIONS

5.1 Considered PQC Accelerators for Experiments

In our RE efforts, we considered seven unique PQC accelerators with different characteristics and different implementors behind them. Before delving into the more specific details of the seven selected PQC accelerators, we want to clarify that there is no particular fitness criteria behind their selection – We essentially considered every open source PQC hardware accelerator design that we were able to source. Since all of them make use of Keccak by definition, all of them can be analyzed with REPQC. More specific details of the chosen accelerators are given below.

First, we consider *kali* [4], a PQC accelerator with a crafty combination of Dilithium and Kyber. When attacking *kali*, we target only its Dilithium functionality. Since the design also supports Kyber, it complicates the RE effort. We consider four variants of *kali*: *kali_bl* is the original baseline design [4]; In *kali_nm*, we remove the memories from the design to emulate a harder scenario

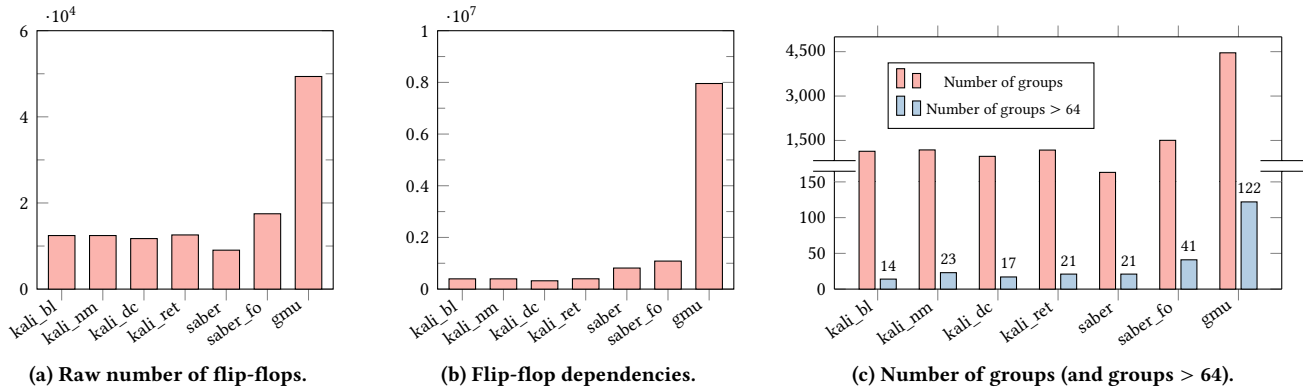


Figure 8: Characteristics of the circuits considered in this work.

in which the adversary cannot use the memories for netlist understanding; In *kali_dc*, we perform synthesis using Synopsys Design Compiler, whereas all other circuits are synthesized in Cadence Genus; Finally, in *kali_ret*, retiming⁷ is performed. Supposedly, retiming could reshape the flip-flop dependencies and make our fanin/fanout observations invalid.

We also consider two other PQC designs that implement Saber, a KEM algorithm that also makes use of Keccak. The reasoning is that if one can find Keccak in an accelerator for a completely different algorithm, this is an indication that Keccak can, in fact, be used as an anchor for reverse engineering. Furthermore, we consider the Saber accelerator described in *saber* [31]. This accelerator employs Keccak in a slightly different manner than *kali*, i.e., different rates and capacities are employed. For certain, the use of different rates and capacities has no bearing on the permutation functions, so the ability of REPQC to find the Keccak state should be precisely the same. We validate this premise by including this accelerator. In *saber_fo* [26], a first-order masked version of Keccak is considered to, potentially, further increase the difficulty of RE since this implementation contains many more flip-flops and intricate connections between them. Finally, in the *gmu* design [11], multiple instances of Keccak are part of the same Dilithium accelerator, creating a significant challenge for RE.

For all experiments reported in this work, logic synthesis was executed in Cadence Genus v19.10, physical synthesis using Cadence Innovus v18.10, and the technology considered is a commercial 28nm CMOS technology. Several implementation scripts are available in our repository for the sake of reproducibility. All execution times are reported in a Xeon CPU running at 3.60GHz.

5.2 Experimental Results

Reverse Engineering with REPQC. Let us describe the results related to the reverse engineering aspects of our work. In Fig. 8, the characteristics of the seven studied circuits are presented, and Fig. 8a gives the total number of flip-flops per circuit; notice that the *gmu* circuit is significantly larger than the others. Fig. 8b depicts the number of flip-flop dependencies, indicating that the *gmu* circuit is much more complex than the others. Finally, in Fig. 8c, the

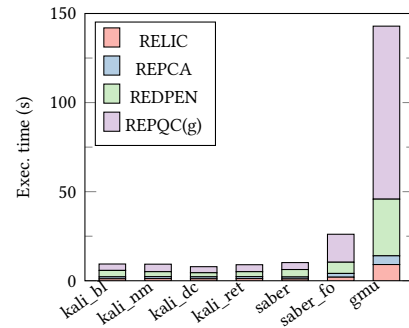


Figure 9: Execution time of the many RE steps.

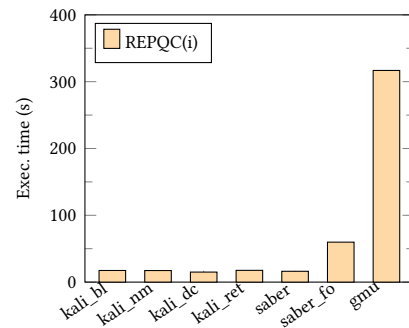


Figure 10: Execution times for REPQC(i), assuming the REPQC(g) strategy is not successful.

number of groups is shown (melon color), as well as the number of groups with more than 64 flip-flops (steel blue color). The difference between the bars gives a notion of the difficulty of the problems tackled by REPQC(g) and REPQC(i). Notice that the vertical axis has a discontinuity and different scales.

Execution times of the different reverse engineering steps are given in Fig. 9. Notice how the execution time is dominated by REPQC(g), and the largest circuit takes approximately two minutes to be analyzed. When grouping is not reliable, the REPQC(i) strategy is utilized, and the execution times increase accordingly, as shown in Fig. 10.

⁷Retiming is a circuit optimization technique that shifts the location of combinational logic with respect to sequential logic in order to balance the logic stages in a design.

The outcome of the REPQC analysis is provided in Tab. 2, where we indicate how many flip-flops are identified as Keccak state candidates. Initially, a naive search is conducted where $FIF = 33$; $FOF = 33$; FIC and FOC are unbounded (see Fig. 4 for details). This approach filters out thousands of flip-flops but always returns more candidates than the expected 1600 (or multiples of). In other words, the naive search finds all the expected correct candidates and a few more. A clever search procedure can be executed by setting $FOC = FIC$ and repeatedly incrementing FOC until the number of candidates exceeds the expected 1600. Now, the number of candidates is much closer to the expected value.

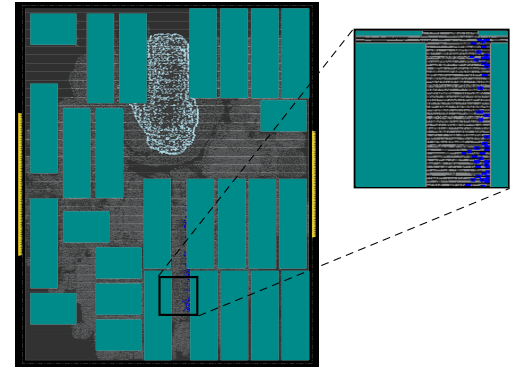
For the *saber_fo* circuit, the Keccak state identification is perfect. For the other circuits, even if the state identification is not perfect, this is already sufficient for REPQC to succeed because **all** of the correct candidates remain in the set of candidates. A simple approach for further filtering out candidates would be to find the dominant Z-score among the candidates and eliminate those with a higher Z-score.

HTH Insertion after REPQC. For HTH insertion, we will consider two implementations of the *kali* design, area-efficient and speed efficient, with target frequencies of 2.00GHz and 2.19GHz, respectively. First, we implement the layout of these two baseline designs by performing placement, clock tree synthesis, optimizations, and routing. The results are summarized in Tab. 3 and Tab. 4 for the area and speed-efficient implementations, respectively. Implementation scripts and floorplan decisions are provided in our repository. Both baseline designs have been generated using a commercial 28nm CMOS technology and an industry-grade design flow; therefore, they are considered fabrication-ready since they pass all design rule checks. We also highlight that the clock frequency of these designs is a near match to the one reported by the authors of [4].

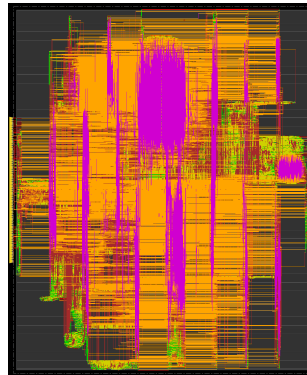
A few entries on these tables are marked in bold to indicate scenarios in which the presence of an HTH has made the design less efficient than the baseline, which is not desirable from the point of view of an adversary. We note that this is the case for all A-IP designs in Tab. 3, highlighting yet another disadvantage of A-IP over A-F0. For this reason, we envision that the adversary might have to iterate a few times until he/she is satisfied with the ‘quality’ of the HTH. In Fig. 3, this is visualized with the diamond-shaped decision block “Fits?”.

The reason why the HTHs inserted by A-F0 are less intrusive to the design is the ECO flow that the adversary uses. We clarify that the ECO flow was conceived for hotfixing a layout, such that a last-minute bug found in a design can be fixed without designers having to go through the entire flow. The ECO flow does that by promoting only local changes in a layout and attempts to keep the unaffected logic/wires untouched. This is why all vendors offering modern chip design tools support this benign functionality. Here, we turn this functionality into a malicious asset for the adversary.

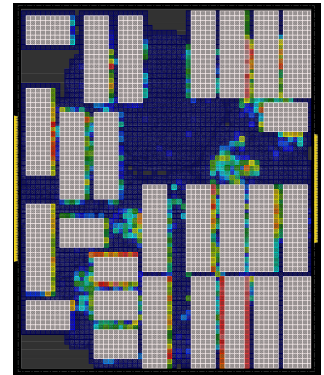
Some clear trends can be observed in Tab. 3, where all A-IP and A-F0 compromised designs lead to an increase in density, cell count, static power, and total power. This is expected. For the increase in power, we clarify that the numbers are reported assuming the oscillator is not enabled, which is how the victim would perceive the circuit/chip. Therefore, the increase in power is due to the



(a) Floorplan.



(b) Routed view.



(c) Placement density.

Figure 11: Multiple views of the speed-efficient *kali* design that measures $540\mu m \times 670\mu m$. The Keccak state is marked in light blue, and the inputs to Keccak are marked in dark blue. Large cyan rectangles are the memories.

HTH comparator that is constantly looking for the message M . In Tab. 4, the trends are not so clear because the A-IP compromised designs do not meet the target frequency of 2.19GHz. The most remarkable results are those from A-F0 with $T = 64$ and $L = 64$, which display a modest increment in density and power while achieving the malicious goals of the adversary. The execution time for the ECO insertion of this HTH only takes 73s.

The final layout of the speed-efficient *kali* design is given in Fig. 11. Fig. 11a shows the floorplan of the design where the memories are the large cyan rectangles, the Keccak state flip-flops are highlighted in light blue (paramecium-like structure), and the inputs to Keccak are marked in dark blue. Notice that the design is memory-heavy, and yet memories have no bearing on the success of REPQC. The signal routing for this design is shown in Fig. 11b. Note that the area next to the Keccak input flip-flops is very congested – pink is the highest metal in the metal stack, and it is heavily utilized in the considered region. Finally, in Fig. 11c, we highlight the placement density of the design, which also indicates that the region near the Keccak input flip-flops is heavily occupied.

The nature of the HTH proposed in this work, connected to the Keccak input, dictates that the HTH would compete with the existing logic for scarce routing and placement resources. This difficulty

Table 2: Results of the REPQC analysis.

Circuit	Flip-flops	Naive search			Clever search		
		FIF, FIC	FOF, FOC	CKFF/KFF	FIF, FIC	FOF, FOC	CKFF/KFF
<i>kali_bl</i>	12435	[33, ∞]	[34, ∞]	1774/1600	[34, ∞]	[34, 35]	1603/1600
<i>kali_nm</i>	12435	[33, ∞]	[34, ∞]	1774/1600	[34, ∞]	[34, 35]	1603/1600
<i>kali_dc</i>	11733	[33, ∞]	[34, ∞]	1709/1600	[34, ∞]	[34, 35]	1603/1600
<i>kali_ret</i>	12579	[33, ∞]	[34, ∞]	1772/1600	[34, ∞]	[34, 35]	1603/1600
<i>saber</i>	9042	[33, ∞]	[34, ∞]	1868/1600	[34, ∞]	[34, 35]	1720/1600
<i>saber_fo</i>	17493	[33, ∞]	[34, ∞]	3205/3200	[34, ∞]	[34, 145]	3200/3200
<i>gmu</i>	49368	[33, ∞]	[34, ∞]	5794/4800	[34, ∞]	[34, 35]	4861/4800

FIF and FIC stand for FanIn Floor and FanIn Ceiling. Similarly, FOF and FOC stand for FanOut Floor and FanOut Ceiling.

KFF stands for Keccak state flip-flops. CKFF stands for candidate Keccak state flip-flops. CKFF includes all the KFF candidates.

Table 3: Characteristics of the *kali* design when implemented with a very tight area.

Design	Trojan	Dimensions ($\mu\text{m} \times \mu\text{m}$)	Density (%)	Cell count	Frequency (GHz)	Static power (μW)	Power (μW)
Baseline (<i>kali_bl</i>)	N/A	460x670	66.70%	58215	2.00	3.860	354.85
A-IP compromised	$T=64, L=16$	460x670	67.83%	59026	2.00	3.929	360.37
A-IP compromised	$T=64, L=32$	460x670	68.79%	59218	2.00	3.982	363.06
A-IP compromised	$T=64, L=64$	460x670	69.58%	58747	1.96	3.985	364.77
A-FO compromised	$T=64, L=16$	460x670	66.87% (+0.17%)	58383	2.00	3.868	355.11
A-FO compromised	$T=64, L=32$	460x670	66.92% (+0.22%)	58415	2.00	3.871	355.19
A-FO compromised	$T=64, L=64$	460x670	67.01% (+0.31%)	58485	2.00	3.877	355.37

Table 4: Characteristics of the *kali* design when implemented with relaxed area and challenging frequency.

Design	Trojan	Dimensions ($\mu\text{m} \times \mu\text{m}$)	Density (%)	Cell count	Frequency (GHz)	Static power (μW)	Power (μW)
Baseline (<i>kali_bl</i>)	N/A	540x670	43.70%	59880	2.19	4.084	392.57
A-IP compromised	$T=64, L=16$	540x670	43.59%	59413	2.17	4.042	387.18
A-IP compromised	$T=64, L=32$	540x670	43.83%	59952	2.11	4.073	385.76
A-IP compromised	$T=64, L=64$	540x670	44.23%	60367	2.18	4.138	391.11
A-FO compromised	$T=64, L=16$	540x670	43.80% (+0.10%)	60048	2.19	4.092	392.88
A-FO compromised	$T=64, L=32$	540x670	43.83% (+0.13%)	60080	2.19	4.095	393.00
A-FO compromised	$T=64, L=64$	540x670	43.89% (+0.19%)	60150	2.19	4.101	393.27

explains, partially, why some A-IP compromised designs have not met the targeted frequency of operation. This problem is even more pronounced for the area-efficient version of *kali*, depicted in Fig. 12. By comparing Fig. 12a with Fig. 12c, it is possible to infer that the tool tried to squeeze the HTH between two memories but, due to lack of space, ended placing the HTH nearby. By comparing Fig. 12b with Fig. 12d, it is barely possible to notice changes before and after HTH insertion. This is the intended outcome of a malicious ECO operation since only deep physical inspection would reveal the HTH presence. More details about the differences in routing are provided in Appendix C.

5.3 Discussions

The success of the attack is intimately linked to the adversary’s capability to locate the Keccak state a , which we hypothesize that will always be there as flip-flops. Implementing the state in SRAM memory would be incredibly inefficient since Keccak rounds have concurrent read/write from/to all of its state elements. There is also the possibility of not implementing the state and instead encoding the entire 24 rounds in a purely unrolled combinational implementation. This would immediately turn Keccak into the performance

bottleneck of the entire PQC accelerator and is simply not desirable. These assertions are supported by the findings of [30], where the authors find that only two rounds can be unrolled before the Keccak operation slows down the entire accelerator.

Improving the Attack. Many additional observations can be made by an attacker attempting to improve his/her reverse engineering-based attack. In REPQC, only flip-flops are considered, but combinational logic can also be used for structural analysis. We also do not use any physical hints: an adversary can correctly assume that all 1600 Keccak state flip-flops are supposed to be clumped together, and any flip-flop outside of a certain range is not a reasonable candidate. This can be visualized in Fig. 11a.

Furthermore, an attacker can specialize REPQC for a given targeted implementation by asserting values for the fanin/fanout margins (i.e., *FIF*, *FIC*, *FOF*, and *FOC*). An attacker can also specialize the RELIC recipes for better filtering Keccak state candidate flip-flops. Our analysis and experimental results show that our proposed recipes are good enough for the generic case, but other recipes may yield better results for individual circuits.

Improving the Defence. A summary of the many possible defence approaches is given in Tab. 5. Our observation is that, among

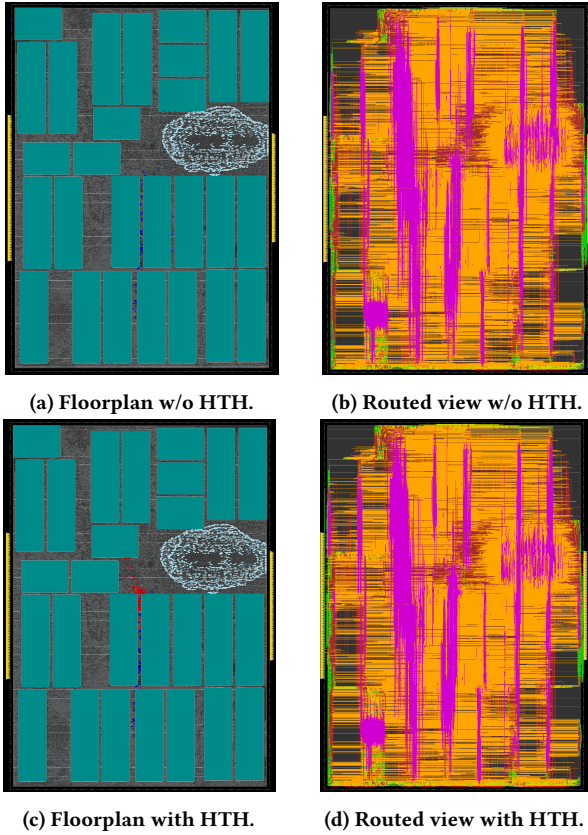


Figure 12: Multiple views of the area-efficient *kali* design that measures $460\mu\text{m} \times 670\mu\text{m}$. The HTH is highlighted in red.

the approaches considered in this work, having multiple Keccak instances is fairly effective, as is the case in the *gmu* design. Those do not directly impede the localization of the Keccak state but make register grouping far more difficult. In fact, for *gmu*, the REPQC(g) strategy is not suitable. First-order masking has been considered in the *saber_fo* design. Since the input message (M) is only used for hashing, it will be boolean-masked (using XOR gate). The control flow will be fixed so the attacker can insert the trojan for XORing the two shares of M , which will be loaded in the Keccak states for hashing. Hence, the approach is very easily applicable for masked implementation. Surprisingly, the masking structure is so regular that it made REPQC more reliable (this is what we refer as ‘hints’ in Tab. 5). On the other hand, it remains to be studied what effect other masking schemes would have. At a bare minimum, we expect execution times to increase as more complicated or higher order masking schemes are considered.

We have also considered circuits synthesized in tools from different vendors and concluded that the Keccak round structure is not affected, as expected, since synthesis must respect the hardware description. We have also considered retiming but to no avail. In theory, the Keccak round structure is not retiming-friendly since it contains a feedback loop. Moving the combinational logic, in this case, achieves no rebalancing of the logic stages. This can be explained by the fact that the Keccak sponge function is analogous to a pipeline with a depth of one. It is possible, however, that retiming

Table 5: Summary of potential mitigations.

Approach	Used in TW	Implication for RE
Multiple instances	✓	Increases execution time ☹ Prevents register grouping ☹
Masking (FO)	✓	Increases execution time ☹ Creates additional hints ☹
Masking (Other)	✗	Increases execution time ☹
Diversified synth.	✓	None ☹
Retiming	✓	None ☹
Decoys	✗	Unknown

TW=this work. Smile faces are from the point of view of the defender.

might affect the Keccak input, but we have not witnessed it in our experiments with *kali_ret*.

Finally, we propose a couple of other promising approaches. We hypothesize that decoy flip-flops could break the rigid Keccak structure, but this is only of interest as long as other security properties remain in place. It is also possible to consider a combination of defences to confuse the RE process.

6 CONCLUSION

Today, the transition to PQC is going full steam ahead. Partially motivated by ‘Store Now, Decrypt Later’ attacks, we are already observing the transition to quantum-resistant cryptography before quantum computers become widely available. Being so, the need to have PQC hardware accelerators is urgent. We have shown in this paper that such accelerators can be reverse-engineered and backdoored with remarkable levels of sophistication and automation. Furthermore, since this study is the first to reveal an automated approach for RE of PQC hardware accelerators, many avenues for future research remain open, both adversarial and defensive. On the adversarial side, we confidently state that locating the Keccak state in a blind netlist can be done with high confidence. However, the same cannot be said about locating the Keccak input. Our insight is that defensive approaches that fuzzy the location of the Keccak input, directly or indirectly, will pose significant challenges to an adversary.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The C++ source code and a binary for REPQC is available from our repository [47]. It also contains several shell scripts for automation, many HTH samples and netlists.

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A RELIC

Each panel of Fig. 13 is a representation of RELIC’s output for a given circuit. Values close to zero indicate that the considered flip-flop is more likely to be part of a datapath than part of the control logic. The opposite is true for high values.

Notice from the distributions for *kali* variants, i.e., panels (a-d), that there are similarities, despite these circuits have been generated by different tools and in different ways. This is an indication that the properties of Keccak are kept; thus, REPQC, which builds on RELIC, is agnostic with respect to synthesis.

Notice too that the Keccak state flip-flops, marked in light blue triangles, do not appear continuously one after another in these plots. In particular, the plot in panel (d) reveals that the Keccak state appears in two distinct regions. However, the plot in panel (f) reveals that the state appears in 9 separate continuous regions. In other words, the Z-score alone is not sufficient to determine which flip-flops implement/do not implement the Keccak state.

B OSCILLATOR

Notice that all branches of the oscillator depicted in Fig. 7 have a common NAND and four common INVs. However, the BUFFs connected to the MUX input ports have different sizes which in turn will yield different frequencies of oscillation. Note that the NAND port controls the operation of the circuit through the external enable signal; the number of INVs determines the base oscillation frequency; the BUFFs are purposefully sized differently to create distinct power profiles from different frequencies of oscillation.

The range of operation of the oscillator is given in Fig. 14. This is a Monte Carlo (MC) simulation for 1000 datapoints for each of the four leak configurations, i.e., $leak = \{00, 01, 10, 11\}$. This type of simulation is useful to determine how the oscillator will behave

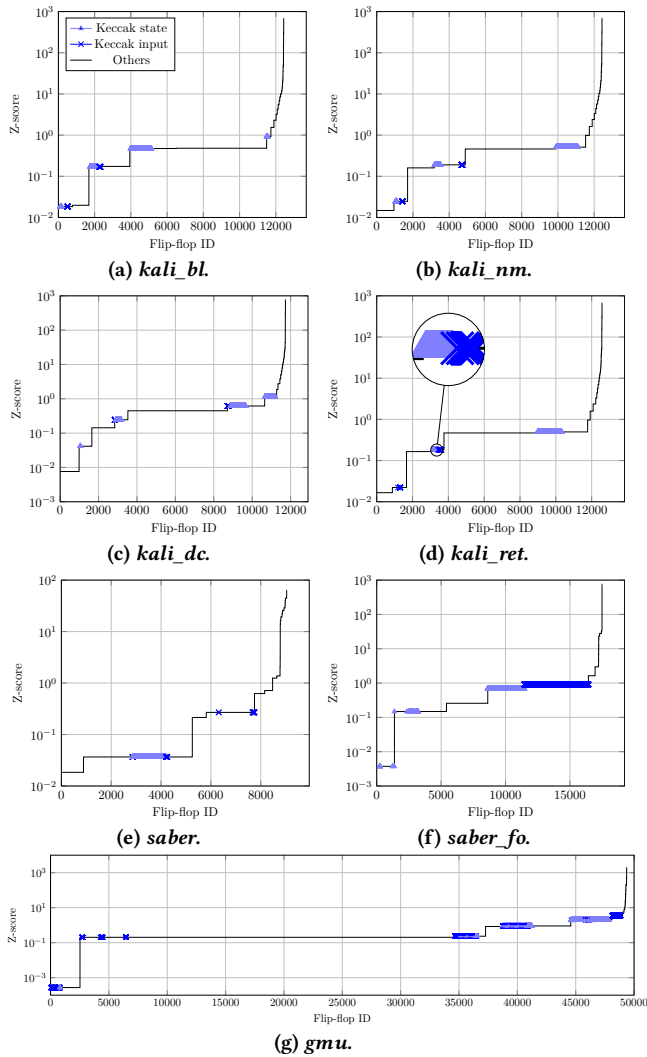


Figure 13: Z-scores of the PQC accelerators considered in this work.

given that no silicon is identical and there is significant process variation involved. The mean frequencies of operation are 639, 671, 732, and 767MHz, which in turn correspond to the dynamic power values of 32.3, 34.2, 36.9, and 38.9uW depicted as distribution means in Fig. 14.

When an adversary is devising his/her payload, many oscillator features can be configured. The number of bits being leaked at a time can be increased/decreased by using a MUX with more/less ports (or a chain of MUXes). The base frequency of oscillation can be increased/decreased by removing/adding more inverters to the common branch. The separation between the power consumption distributions can be tuned by uniquely sizing the BUFFs that drive the MUX ports. It is important that these distributions are distinguishable from one another, so the leaked data is clean and easy to read is. In Fig.14, the minimal overlap between distributions happens in near-impossible scenarios where one BUFF and one BUFF

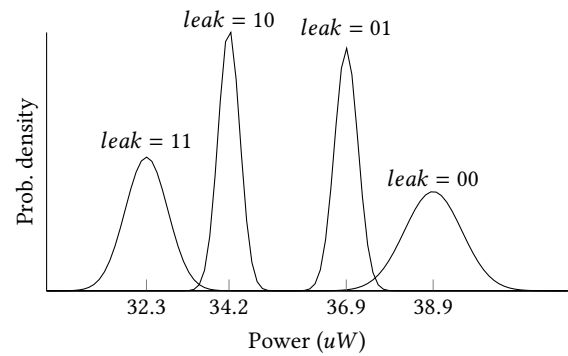


Figure 14: Monte Carlo analysis of the ring oscillator.

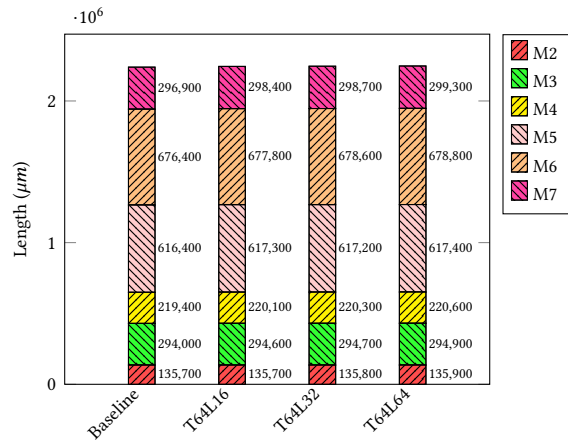


Figure 15: Wirelength of the compromised designs versus the Trojan-free baseline.

only is disproportionately affected by process variation, which is an artefact of the over-pessimistic nature of MC simulation.

A single SPICE file with all the individual gate sizings is available in our repository. Yet, this is only one possible configuration, many more are possible by tuning the ring oscillator branches.

C METAL STACK AND ROUTING STATISTICS

The considered metal stack in our layouts contains 9 metals. Metal 1 is reserved for intra-cell routing and cannot be used for signal routing. Metals 8 and 9 are reserved for the power grid and cannot be used for signal routing either. The remaining metals are 2-7. In Fig. 15, we show the metal utilization of these metals (wirelength) for the baseline and three compromised versions of the speed-efficient kali design depicted in Fig. 12. We recall that the adversary considered is A-FO and the additional metal is incurred from the ECO operation. Notice how there are very small differences in metal utilization, which is an indication that the HTH insertion is stealthy and preserves the properties of the original design. This is the power of the ECO engine, here turned into a malicious attack vector.