Block-Wise Dynamic-Precision Neural Network Training Acceleration via Online Quantization Sensitivity Analytics

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Figure 1: Mixed-precision quantization in NN training

1 INTRODUCTION

Neural networks(NN) have been widely adopted in many fields, including computer vision[1], speech recognition[2], and natural language processing[3]. However, training NN usually needs large computing power, which requires high-cost cloud servers and makes it infeasible to train on low-power edge devices. Researchers have been studying various methods for NN training acceleration, such as exploiting data pruning algorithm[4] and developing more efficient hardware accelerators[5].

As NN training is usually carried out with 32-bit float point data, low-bit network quantization can be an effective way for NN training acceleration. There are 3 ways for NN quantization: post-training quantization[6], quantization aware training[7], and fully-quantized training[8]. The first 2 methods only quantize network inference data and do not accelerate training process, and they usually need to train auxiliary NN or use methods like evolutionary search, leading to even longer training time[9]. Meanwhile, fully-quantized training aims at online quantization of all training data, which can significantly reduce the computation cost needed for training.

Early works on fully-quantized training adopt an equal bit-width for the entire network[8], which leads to either high accuracy loss or limited bit-width reduction. Later works utilize mixed-precision training to provide better acceleration while maintaining network accuracy. Some works like [10] assign different bit-widths to each network layer, and state-of-the-art quantization results are acquired through block-wise mixed-precision training[11]. As shown in Fig. 1, block-wise mixed-precision training divides training data into small blocks, and quantizes them into different bit-widths. Whether layer-wise or block-wise, mixed-precision training is challenging in how to perform online precision assignment for each layer/block of data. Some of the existing works use data quantization sensitivity acquiring algorithms such as calculating Hessian eigenvalue and

ABSTRACT

Data quantization is an effective method to accelerate neural network training and reduce power consumption. However, it is challenging to perform low-bit quantized training: the conventional equal-precision quantization will lead to either high accuracy loss or limited bit-width reduction, while existing mixed-precision methods offer high compression potential but failed to perform accurate and efficient bit-width assignment. In this work, we propose DY-NASTY, a block-wise dynamic-precision neural network training framework. DYNASTY provides accurate data sensitivity information through fast online analytics, and maintains stable training convergence with an adaptive bit-width map generator. Network training experiments on CIFAR-100 and ImageNet dataset are carried out, and compared to 8-bit quantization baseline, DYNASTY brings up to 5.1× speedup and 4.7× energy consumption reduction with no accuracy drop and negligible hardware overhead.

CCS CONCEPTS

• Computing methodologies → Neural networks; *Philosophi*cal/theoretical foundations of artificial intelligence.

KEYWORDS

fully-quantized network training, mixed-precision quantization, neural network training acceleration

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trace[10, 12], which are too complicated for hardware implementation; other works utilize heuristic methods like greedy search[11], which does not generate accurate bit-width distribution.

To address the aforementioned weakness, we propose DYNASTY (**DYN**amic **A**nalytics of **S**ensitivi**TY**), a block-wise dynamic-precision NN training framework. By using analytics methods, DYNASTY performs fast dynamic data bit-width assignment, and achieves average 2-bit quantization with minimum accuracy drop. Key contributions of the work are concluded as follows:

- A software-hardware co-designed block-wise fully-quantized mixed-precision NN training framework named DYNASTY. It provides a block-float-point quantized training algorithm with 0-8 bits dynamic block precision, and extends an on-line bit-width assignment module to the NN acceleration hardware architecture.
- A Relative Quantization Sensitivity Analytics algorithm. By applying relaxed Lagrange duality, it transforms the NP-hard bit-width searching problem into *O*(*N*) complexity, providing fast but still accurate online data quantization sensitivity analysis.
- An Adaptive Bit-Width Map Generator that maps data sensitivity to bit-width. It performs online tuning of algorithm hyperparameter to maintain stable average bit-width, and employs bit-width map temporal smoothing to furtherly enhance network accuracy.
- Experiments on our algorithm show 5.1× training speedup with no accuracy drop on CIFAR-100, and 1.9× speedup with 0.39 % accuracy drop on ImageNet, compared to 8-bit quantization baseline. Our hardware architecture shows minimum overhead on die area (+1.4 %) and brings at most 78.8 % energy consumption reduction.

2 PRELIMINARY & RELATED WORKS

2.1 Quantized NN Training Basics

While NN inference requires only one forward pass computation, training involves three different stages: forward, backward and weight update. Each stage includes multiply-accumulate(MAC) operations on different data: for the forward stage, they are activations and weights; for the backward stage, they are activation gradients (also called errors) and weights; and for the backward stage, they are activations and activation gradients.

Researchers have found training quantization to be more challenging than inference. Xiao Sun et al. [13] point out that quantization saturation can be severe in training due to the large dynamic range of gradient data in the backward stage. Later work[14] furtherly discover that different network layers show widely different ranges of gradients across training epochs.

To better suit these different data distributions, either handcrafted quantization formats for different layers and stages need to be carefully designed as having been done in [13, 14], or better we employ mixed-precision quantization that adaptively adjusts the quantization method for different parts of data in networks.

2.2 Mixed-Precision NN Training

Early works of mixed-precision fully-quantized training such as HAWQ[10] and AdaQS[15] only calculate a relative ordering of the



DYNASTY

e Quant

Sensitivity Analytics

On

Chip

Figure 2: Proposed block-wise dynamic-precision NN training framework

DYNASTY Extended NN Accelerator Hardware

Weight Update

Ctrl

Data

Loader

Variable Bit-Width NN Accelerate

Computing Cores

importance of each data block. They require empirically assigning bit-width to each block, making their method design include trial and error and hard to be accurate.

A better way to get bit-width distribution is through analytics methods, where the bit-width distribution solving is formulated as an optimization problem to minimize impacts brought by quantization noise. ActNN[11] proposes to define the mean square of weight gradients as the optimization target, but this optimization is hard to solve and they have to use greedy search for a heuristic result. HAWQ-V3[16] needs to solve an integer linear programming problem, and MPQCO[17] formulates it into a multiple-choice knapsack problem, both of which are NP-hard to solve.

3 BLOCK-WISE DYNAMIC-PRECISION NN TRAINING FRAMEWORK

3.1 Quantization Training Framework

Figure 2 depicts the overall framework of our system, where the DY-NASTY module extends an NN accelerator for block-wise dynamicprecision training. Input data of all training stages are quantized by Block-Float-Point(BFP) format, which divides data into 4×4 blocks¹. Data in each block have mantissa quantized into a same bit-width, and they also share a single 8-bit exponent. Two strategies are used for mantissa bit-width assignment: in each training stage, one of the input data is statically quantized to 8-bit mantissa; sensitivity analytics is performed for the other input data, whose mantissa is dynamically quantized into 0-8 bits according to the bit-width map generated by the DYNASTY module.

The DYNASTY module is in charge of the dynamic bit-width assignment, and consists of two sub-modules. The first sub-module, named **Relative Quantization Sensitivity Analytics**, receives the current quantization range together with data gradients, and generates a relative quantization sensitivity value for each block.

¹Block division is along C_{in} and C_{out} dimensions for weight and weight gradients, C_{in} and *Batch* dimensions for activations, and C_{out} and *Batch* dimensions for activation gradients.



Figure 3: An example of per-layer relative sensitivity distribution. Red markers represent the mean sensitivity per layer, and different colored squares represent the proportion of different sensitivity ranges in each layer.

This analytics happens at the end of the training of each mini-batch. This sub-module will be detailed in Section 3.2. The second sub-module, the **Adaptive Bit-Width Map Generator**, works at the end of each training epoch. It maps the sensitivities into a bit-width distribution and maintains stable training. This mapping happens at the end of each training epoch. Details of this sub-module will be provided in Section 3.3.

3.2 Relative Quantization Sensitivity Analytics

To perform fast online data analysis and dynamically identify which data is more important and need larger quantization bit-width than others, the Relative Quantization Sensitivity Analytics module is designed to calculate data quantization sensitivity based on their quantization range and corresponding gradients. We first establish an optimization problem based on the minimization of first-order mean square loss noise. Then we propose to solve the optimization by relaxed Lagrange duality method and get the sensitivity values.

3.2.1 Optimization Problem Based On First-Order Mean Square Loss Noise. Quantization brings noise to network training process, leading to less stable training and lower network accuracy. An ideal bit-width assignment should minimize this noise and bring minimum perturbation to the train loss. We propose to use the first-order mean square loss noise(ΔL^2) to quantify this perturbation. The math formula of ΔL^2 caused by weight quantization is shown as Eq. (1). It is calculated as the mean square value of firstorder loss noise caused by each quantized data. And we use S_i to denote the ratio of loss noise to quantization levels in each data block. In Eq. (1), $\Delta W_{i,i}$ is the gradient of the *j*th weight of the *i*th block; $\sigma_{i,j}$ is the quantization noise of corresponding data; N is the total number of data blocks; B is the number of values inside each block; b_i is the quantization bit-width of the mantissa of the *i*th block of weights; and e_i is the exponent of each block so that 2^{e_i} is the corresponding quantization range. Note that, ΔL^2 brought by activation quantization can also be calculated in the same way, and we omit its formula here for simplicity. With our formulation, ΔL^2 is calculated from the quantization range of each block and their corresponding gradient values, both of which are already known during NN training.

$$\Delta L^{2} = \frac{1}{NB} \sum_{i=1}^{N} \sum_{j=1}^{B} \left(\Delta W_{i,j} \cdot \sigma_{i,j} \right)^{2} = \frac{2}{3NB} \sum_{i=1}^{N} S_{i} \left(2^{-b_{i}} \right)^{2}$$

$$S_{i} = \frac{(2^{e_{i}})^{2}}{16} \sum_{i=1}^{B} \Delta W_{i,j}^{2}$$
(1)

The full optimization is shown as Eq. (2). Aside from ΔL^2 as our optimization target function, we also specify the optimization constraints. The α denotes the desired average computation bit-width, which is the T_i weighted average of block bit-width b_i , where T_i represents the amount of computation associated with corresponding data. Bit-width lower bound 0 and upper bound β are also specified.

S

$$\underset{\mathbf{b}}{\operatorname{arg\,min}} \qquad f(\mathbf{b}) = \Delta L^2 \qquad (2a)$$

ubject to
$$\frac{\sum_{i=1}^{N} T_i b_i}{\sum T_i} \le \alpha$$
 (2b)

$$b_i \in \mathbb{Z}$$
 (2c)

$$0 \le b_i \le \beta \tag{2d}$$

3.2.2 Problem Solving for Relative Quantization Sensitivity. Optimization in Eq. (2) is a mixed integer convex programming problem. It is NP-hard to solve and too complicated for hardware implementation. Thus we propose to relax the restriction in Eq. (2c) to the \mathbb{R} set, and then apply Lagrange duality to this problem. This leads to the solution shown in Eq. (3). The bit-width is calculated from value r and a hyperparameter λ . r is easy to compute based on Eq. (3b). It is positively correlated with S_i and negatively correlated with T_i , and only requires O(N) time complexity for weights and activations of the entire network. r tells the relative bit-width between data blocks, and we call it the **relative quantization sensitivity**. Though we still do not know the value of λ , we successfully **transform the searching of bit-width of N different blocks into the searching of only a single hyperparameter.** We call λ the **global quantization coefficient**.

$$b_i = \max(0, \min(r_i - \lambda, \beta)) \tag{3a}$$

$$T_i = \frac{1}{2}\log_2 \frac{S_i}{T_i} \tag{3b}$$

An example of r distribution during training of ResNet-18 is shown as Fig. 3. We can see that the desired bit-width distribution should be different across network layers. Data in several layers requires much larger bit-widths than others, including weights in the first, the last, and the 3 shortcut layers, and activation in the last layer. Bit-width distribution inside each layer is also different, and activations' bit-widths tend to be more spread out and reside in larger ranges than weights'. These observations suggest that manually setting bit-width can hardly suit the data requirement, and online bit-width assignment based on data sensitivity is needed.

However, though Eq. (3b) uncovers the relative bit-widths between data blocks, it still does not give us the absolute bit-width of each block of data. Two problems remain to be solved. The first is how to search the value of λ . The second is that the sensitivities of some blocks are unstable across training epochs, leading to bit-width fluctuating periodically as shown in Fig. 4, which brings



Figure 4: Data bit-width fluctuation reduces network accuracy.



Figure 5: Real network bit-width when targeting 3-bit quantization. Without linear interpolation-based tuning of λ , the average bit-width tends to become larger than desired.

0.4% to 1% network accuracy drop in our experiment. Both of these problems are addressed in Section 3.3.

3.3 Adaptive Bit-Width Map Generator

The Adaptive Bit-Width Map Generator aims to solve the remaining problems mentioned in Section 3.2 and maps the relative sensitivities r of each block to their exact quantization bit-widths.

3.3.1 Dertermine the Value of λ . To find the exact global quantization coefficients λ , we develop an adaptive quantization coefficient adjustment algorithm to dynamically determine the coefficient during training. In theory, if we ignore these upper and lower bounds constraints in Eq. (3a), an approximate of λ can be easily deduced as $\hat{\lambda} = \sum_i B_i - N\alpha$, where N is the number of blocks. With experiments, we discover that in the initial training of a network, differences in the importance of data in the network are not much and seldomly make b_i reach the lower or upper bound, thus $\hat{\lambda}$ is a good estimation of the initial λ value.

However, as shown in Fig. 5, using only $\hat{\lambda}$ leads to the average bit-width becoming larger than desired as training continues, especially for activation data. To prevent λ drifting away from the desired value, we design Algorithm 1, which tunes λ with linear interpolation using the last λ value as the start point of the interpolation. The number of interpolation iterations *L* is empirically set to 3. By using this method, average bit-width can be maintained stably at the target bit-width, as the blue lines show in Fig. 5.

3.3.2 Prevent Bit-Width Fluctuatation. To solve the bit-width fluctuation problem, we propose a bit-width map temporal smoothing

Trovato	et	al.

Algorithm 1 Global Quantization Coefficient Tuning				
Input: λ_{in} : the last global quantization coefficient				
r: relative sensitivity				
α : target averaged quantization bit-width				
Output: λ_{out} : the tuned global quantization coefficient				
Parameter: <i>L</i> : number of interpolation iterations				
1: begin				
2: $\lambda_{out} = \lambda_{in}$				
3: $\lambda_0, \lambda_1 \leftarrow \min(\mathbf{r}) - \alpha, \max(\mathbf{r}) - \alpha$				
4: for $l = 1$ to L do				
5: $b_0 \leftarrow \frac{1}{N} \sum_i \max(\min(r_i - \lambda_0, \beta), 0)$				
6: $b_1 \leftarrow \frac{1}{N} \sum_i \max(\min(r_i - \lambda_1, \beta), 0)$				
7: $\overline{b} \leftarrow \frac{1}{N} \sum_{i} \max(\min(r_i - \lambda, \beta), 0)$				
8: if $\overline{b} > \alpha$ then				
9: $t \leftarrow (\overline{b} - \alpha) / (\overline{b} - b_1)$				
10: $\lambda_0, \lambda_{out} \leftarrow \lambda_{out}, (1-t) \lambda_{out} + t \cdot \lambda_1$				
11: else				
12: $t \leftarrow (\overline{b} - \alpha) / (\overline{b} - b_0)$				
13: $\lambda_{out}, \lambda_1 \leftarrow (1-t) \lambda_{out} + t \cdot \lambda_0, \lambda_{out}$				
14: end if				
15: end for				
16: end				

method: at every epoch, an exponential moving average is performed on the bit-width map, shown as Eq. (4). This prevents sudden changes in data bit-width caused by any calculation error. The smooth factor γ is empirically set to 0.5.

$$b_{i,\text{smoothed}} = \gamma \cdot b_{i,\text{last}} + (1 - \gamma) b_{i,\text{new}}$$
(4)

Note that, during the first training epoch when we have not got the value of $\hat{\lambda}$, we assign 4 bits to every block as the initial bit-width map. And for hardware simplicity, we perform rounding on the bit-width map to only use 0,2,4,6,8 as possible quantized bit-widths. Specially, when a block is quantized to 0 bit, we skip the computation of this block. The smoothed bit-width map is then sent to the accelerator computing cores for dynamic data quantization.

4 HARDWARE ARCHITECTURE

Support of variable bit-width operation has been realised through NN accelerators with bit-serial-based computation array[5, 18]. These accelerators get linear speedup as the operation bit-width shrinks. The DYNASTY hardware architecture extends such accelerators with online bit-width assignment ability.

Fig. 6 shows the hardware architecture of the DYNASTY module. The use of 16 parallel sensitivity analytics units makes it capable of calculating the sensitivities and generating bit-width map for 16 blocks, i.e. 256 weights or activations in one cycle. Note that, the DYNASTY module is running in parallel with the main array of the accelerator. A recovery remainder-based divider is used in the Bit-Width Map Generator, but since there is only one divider, and the divisions only happen at the end of each training epoch, it does not bring much area and power overhead.



Figure 6: DYNASTY module hardware architecture

5 EXPERIMENTAL RESULTS

5.1 Experiment Setup

In our experiments, we train ResNet-18 network[19] on the CIFAR-100[20] and ImageNet[21] dataset. For both datasets, we adopt a batch size of 128, and use SGD as the optimizer with an initial learning rate of 0.1. For CIFAR-100, we train the network for 200 epochs; learning rate linear warming up is used in the 1st epoch; and we perform learning rate decay at the 60th, 120th, and 160th epochs with a decay factor of 0.2. For ImageNet, we train the network for 95 epochs; learning rate linear warming up is used in the first 5 epochs; and we perform learning rate decay at the 30th, 60th, and 80th epoch with a decay factor of 0.1.

We also perform training with 2 other methods aside from DY-NASTY as our baseline. The first method is to train with float-32 format without quantization; the second is 8-bit quantized training according to the work of Ron Banner et al. [22].

We implement the DYNASTY module in Verilog and get its area and power information by synthesizing it in Synopsys Design Compiler with TSMC 65nm CMOS technology. The hardware metrics of other modules in a full accelerator are taken from the UNPU accelerator[18].

5.2 Algorithm Evaluation

5.2.1 Network Accuracy. Table 1 shows the validation accuracy that DYNASTY gets with different quantization bit-width. On CIFAR-100, we achieve 4-bit quantization with no accuracy drop compared to float-32 training; even with 2-bit quantization, we only get an accuracy drop of 1.40 % compared to float-32 training and get better accuracy than the 8-bit baseline. On ImageNet, while the accuracy drop with 2-bit quantization is not small (6.25 %), the 4-bit training experiment still reveals good accuracy with only 0.88 % accuracy drop.

5.2.2 Training Convergence Speed Improvement. Figure 7 presents the accuracy-time curve in the experiments. Note that, the training

Table 1: Network accuracy with different average quantization bit-width

Dataset	Method	Average Bit-Width*	Top 1 Validation Accuracy (%)
CIFAR-100	Float-Point	All Float-32	76.54
	Banner et al.	8	74.77 (-1.77)
	DYNASTY	6	76.57 (+0.03)
		4	76.55 (+0.01)
		3	75.81 (-0.73)
		2	75.14 (-1.40)
ImageNet	Float-Point	All Float-32	68.77
	Banner et al.	8	68.28 (-0.49)
	DYNASTY	6	68.60 (-0.17)
		4	67.89 (-0.88)
		3	65.84 (-2.93)
		2	62.52 (-6.25)

^{*}Average bit-width refers to the bit-width of dynamic quantized training data.



Figure 7: Training convergence speed improvement with DY-NASTY

speed for unquantized float-32 training is not compared here, as the cores of the UNPU accelerator cannot handle float-32 operations.

Because the DYNASTY module runs in parallel with the accelerator cores, we enjoy a linear speedup as the quantization bitwidth decreases. Compared to 8-bit training baseline, for CIFAR-100, DYNASTY reaches the same validation accuracy (74 %) in 58.3 %, 38.9 %, 29.2 %, and 19.6 % training time with 6, 4, 3, 2-bit quantization, respectively; because the better convergence than baseline, the speedup ($5.1 \times$ with 2-bit) is even higher than expectation (4×). For ImageNet, DYNASTY needs 75.0 % and 52.5 % time to get 67 % accuracy with 6 and 4-bit quantization, respectively.

5.3 Architecture Evaluation

Table 2 shows the area and power of the DYNASTY module compared to other modules in the accelerator. We can see that DYNASTY brings no more than 1.4% area overhead.

The average power consumption of DYNASTY varies with the network scale and quantization bit-width as these factors affect the duty cycle of the DYNASTY module, and we only show the value

Table 2: Area and power overhead of DYNASTY



Figure 8: Energy consumption reduction with DYNASTY

in a typical situation in Table 2. Details on the energy consumption overhead can be seen in Fig. 8. DYNASTY brings at most 7.9 % power consumption overhead to the accelerator, but this overhead is overcome by the energy saving due to shorter training time with lower-bit quantization. When targeting 74 % accuracy on CIFAR-100, we get 40.0 %, 59.5 %, 69.2 %, and 78.8 % energy consumption reduction when quantizing to average 6, 4, 3, and 2 bits. For ImageNet, we also achieve 23.2 % and 45.7 % energy reduction with 6 and 4-bit quantization when targeting 67 % accuracy.

6 CONCLUSION

In this paper, we propose DYNASTY, a software-hardware codesigned block-wise dynamic-precision neural network training framework. We utilize an analytics method based on network firstorder mean square loss noise to efficiently generate data quantization sensitivity online, and develop an Adaptive Bit-Width Map Generator to accurately map sensitivity to bit-width distribution that maintains desired computation reduction and high network accuracy at the same time. Experiments on CIFAR-100 and ImageNet dataset are carried out, and compared to 8-bit quantization baseline, we achieve up to 5.1× speedup and 4.7× energy consumption reduction with no accuracy drop and negligible hardware overhead.

REFERENCES

- [1] Alex Krizhevsky, Ilya Sutskever, and Geoffrey E Hinton. Imagenet classification with deep convolutional neural networks. In F. Pereira, C.J. Burges, L. Bottou, and K.Q. Weinberger, editors, Advances in Neural Information Processing Systems, volume 25. Curran Associates, Inc., 2012. URL https://proceedings.neurips.cc/ paper/2012/file/c399862d3b9db76c8436e924a68e45b-Paper.pdf.
- [2] Ossama Abdel-Hamid, Abdel-rahman Mohamed, Hui Jiang, Li Deng, Gerald Penn, and Dong Yu. Convolutional neural networks for speech recognition. *IEEE/ACM Transactions on Audio, Speech, and Language Processing*, 22(10):1533–1545, Oct 2014. ISSN 2329-9304. doi: 10.1109/TASLP.2014.2339736.
- [3] Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N Gomez, Ł ukasz Kaiser, and Illia Polosukhin. Attention is all you need. In I. Guyon, U. Von Luxburg, S. Bengio, H. Wallach, R. Fergus, S. Vishwanathan, and R. Garnett, editors, Advances in Neural Information Processing Systems, volume 30. Curran Associates, Inc., 2017. URL https://proceedings.neurips.cc/paper/2017/ file/3f5ee243547dee91fbd053c1c4a845aa-Paper.pdf.

- 10.1109/DAC18072.2020.9218710.
 [5] Yongwei Zhao, Chang Liu, Zidong Du, Qi Guo, Xing Hu, Yimin Zhuang, Zhenxing Zhang, Xinkai Song, Wei Li, Xishan Zhang, Ling Li, Zhiwei Xu, and Tianshi Chen. Cambricon-q: A hybrid architecture for efficient training. In 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA), pages 706–719, June 2021. doi: 10.1109/ISCA52012.2021.00061.
- [6] Ron Banner, Yury Nahshan, and Daniel Soudry. Post training 4-bit quantization of convolutional networks for rapid-deployment. In H. Wallach, H. Larochelle, A. Beygelzimer, F. d'Alché-Buc, E. Fox, and R. Garnett, editors, Advances in Neural Information Processing Systems, volume 32. Curran Associates, Inc., 2019. URL https://proceedings.neurips.cc/paper/2019/file/ c0a62e133894cdce435bcb4a5df1db2d-Paper.pdf.
- [7] Benoit Jacob, Skirmantas Kligys, Bo Chen, Menglong Zhu, Matthew Tang, Andrew Howard, Hartwig Adam, and Dmitry Kalenichenko. Quantization and training of neural networks for efficient integer-arithmetic-only inference. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), June 2018.
- [8] Shuchang Zhou, Yuxin Wu, Zekun Ni, Xinyu Zhou, He Wen, and Yuheng Zou. DoReFa-Net: Training Low Bitwidth Convolutional Neural Networks with Low Bitwidth Gradients. arXiv e-prints, art. arXiv:1606.06160, June 2016.
- [9] Tianzhe Wang, Kuan Wang, Han Cai, Ji Lin, Zhijian Liu, Hanrui Wang, Yujun Lin, and Song Han. Apq: Joint search for network architecture, pruning and quantization policy. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR), June 2020.
- [10] Zhen Dong, Zhewei Yao, Amir Gholami, Michael W. Mahoney, and Kurt Keutzer. Hawq: Hessian aware quantization of neural networks with mixed-precision. In Proceedings of the IEEE/CVF International Conference on Computer Vision (ICCV), October 2019.
- [11] Jianfei Chen, Lianmin Zheng, Zhewei Yao, Dequan Wang, Ion Stoica, Michael Mahoney, and Joseph Gonzalez. Actnn: Reducing training memory footprint via 2-bit activation compressed training. In Marina Meila and Tong Zhang, editors, Proceedings of the 38th International Conference on Machine Learning, volume 139 of Proceedings of Machine Learning Research, pages 1803–1813. PMLR, 18–24 Jul 2021. URL https://proceedings.mlr.press/v139/chen21z.html.
- [12] Zhen Dong, Zhewei Yao, Daiyaan Arfeen, Amir Gholami, Michael W Mahoney, and Kurt Keutzer. Hawq-v2: Hessian aware trace-weighted quantization of neural networks. In H. Larochelle, M. Ranzato, R. Hadsell, M.F. Balcan, and H. Lin, editors, Advances in Neural Information Processing Systems, volume 33, pages 18518–18529. Curran Associates, Inc., 2020. URL https://proceedings.neurips.cc/ paper/2020/file/d77c703536718b95308130ff2e5cf9ee-Paper.pdf.
- [13] Xiao Sun, Jungwook Choi, Chia-Yu Chen, Naigang Wang, Swagath Venkataramani, Vijayalakshmi (Viji) Srinivasan, Xiaodong Cui, Wei Zhang, and Kailash Gopalakrishnan. Hybrid 8-bit floating point (hfp8) training and inference for deep neural networks. In H. Wallach, H. Larochelle, A. Beygelzimer, F. d'Alché-Buc, E. Fox, and R. Garnett, editors, *Advances in Neural Information Processing Systems*, volume 32. Curran Associates, Inc., 2019. URL https://proceedings.neurips.cc/ paper/2019/file/65fc9fb4897a89789352e211ca2d398f-Paper.pdf.
- [14] Xiao Sun, Naigang Wang, Chia-Yu Chen, Jiamin Ni, Ankur Agrawal, Xiaodong Cui, Swagath Venkataramani, Kaoutar El Maghraoui, Vijayalakshmi (Viji) Srinivasan, and Kailash Gopalakrishnan. Ultra-low precision 4-bit training of deep neural networks. In H. Larochelle, M. Ranzato, R. Hadsell, M.F. Balcan, and H. Lin, editors, Advances in Neural Information Processing Systems, volume 33, pages 1796–1807. Curran Associates, Inc., 2020. URL https://proceedings.neurips.cc/paper/2020/file/13b919438259814cd5be8cb45877d577-Paper.pdf.
- [15] Jinrong Guo, Wantao Liu, Wang Wang, Jizhong Han, Ruixuan Li, Yijun Lu, and Songlin Hu. Accelerating distributed deep learning by adaptive gradient quantization. In ICASSP 2020 - 2020 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), pages 1603–1607, 2020. doi: 10.1109/ICASSP40776.2020.9054164.
- [16] Zhewei Yao, Zhen Dong, Zhangcheng Zheng, Amir Gholami, Jiali Yu, Eric Tan, Leyuan Wang, Qijing Huang, Yida Wang, Michael Mahoney, and Kurt Keutzer. Hawq-v3: Dyadic neural network quantization. In Marina Meila and Tong Zhang, editors, Proceedings of the 38th International Conference on Machine Learning, volume 139 of Proceedings of Machine Learning Research, pages 11875–11886. PMLR, 18–24 Jul 2021. URL https://proceedings.mlr.press/v139/yao21a.html.
- [17] Weihan Chen, Peisong Wang, and Jian Cheng. Towards mixed-precision quantization of neural networks via constrained optimization. In Proceedings of the IEEE/CVF International Conference on Computer Vision (ICCV), pages 5350–5359, October 2021.
- [18] Jinmook Lee, Changhyeon Kim, Sanghoon Kang, Dongjoo Shin, Sangyeob Kim, and Hoi-Jun Yoo. Unpu: An energy-efficient deep neural network accelerator with fully variable weight bit precision. *IEEE Journal of Solid-State Circuits*, 54(1): 173–185, Jan 2019. ISSN 1558-173X. doi: 10.1109/JSSC.2018.2865489.

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ASP-DAC 2023, Janurary 16-19, 2023, Tokyo, Japan

- [19] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. Deep residual learning for image recognition. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), June 2016.
- [20] Alex Krizhevsky, Vinod Nair, and Geoffrey Hinton. Cifar-100 (canadian institute for advanced research). URL http://www.cs.toronto.edu/~kriz/cifar.html.
- [21] Jia Deng, Wei Dong, Richard Socher, Li-Jia Li, Kai Li, and Li Fei-Fei. Imagenet: A large-scale hierarchical image database. In 2009 IEEE Conference on Computer

Vision and Pattern Recognition, pages 248–255, June 2009. doi: 10.1109/CVPR. 2009.5206848.

[22] Ron Banner, Itay Hubara, Elad Hoffer, and Daniel Soudry. Scalable methods for 8-bit training of neural networks. In S. Bengio, H. Wallach, H. Larochelle, K. Grauman, N. Cesa-Bianchi, and R. Garnett, editors, Advances in Neural Information Processing Systems, volume 31. Curran Associates, Inc., 2018. URL https://proceedings. neurips.cc/paper/2018/file/e82c4b19b8151ddc25d4d93baf7b908f-Paper.pdf.