HHS Public Access

Author manuscript

Symp VLSI Circuits. Author manuscript; available in PMC 2017 April 05.

Published in final edited form as:

Symp VLSI Circuits. 2016 June ; 2016: .

A 66pW Discontinuous Switch-Capacitor Energy Harvester for Self-Sustaining Sensor Applications

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Abstract

We present a discontinuous harvesting approach for switch capacitor DC-DC converters that enables ultra-low power energy harvesting. By slowly accumulating charge on an input capacitor and then transferring it to a battery in burst-mode, switching and leakage losses in the DC-DC converter can be optimally traded-off with the loss due to non-ideal MPPT operation. The harvester uses a 15pW mode controller, an automatic conversion ratio modulator, and a moving sum charge pump for low startup energy upon a mode switch. In 180nm CMOS, the harvester achieves >40% end-to-end efficiency from 113pW to 1.5μW with 66pW minimum input power, marking a >10× improvement over prior ultra-low power harvesters.

Introduction

Energy harvesting from the ambient environment is essential for self-sustaining sensor nodes and there is a continuing need to harvest extremely small input power sources to enable new application fields. For example, a miniature 100×100um solar cell generates ~150 pW under low lighting conditions (32 lux). Efficient DC-DC upconversion from such a power source voltage to typical battery voltages is extremely difficult. Recent works using both boost and switched-capacitor (SC) DC-DC converters demonstrate various circuit techniques to reduce the minimum input power required for successful harvesting [1–3]. However, they are limited by the constant charge pump leakage and clock generation power and have demonstrated harvesting only down to 1.2nW.

Discontinuous Energy Harvesting

This work proposes a *discontinuous* harvesting approach based on the observation that at low power levels, charge pump efficiency plummets while the efficiency of the energy source remains high due to continuing operation at its maximum power point. Discontinuous harvesting operates in two modes, allowing it to achieve a balance between these two efficiencies and obtain higher overall end-to-end efficiency. In *harvest* mode, the charge pump is power gated, reducing its leakage to just a few pW while the power source charges a capacitor. In *transfer* mode, the charge pump is enabled and energy accumulated on the capacitor is transferred to the battery (Fig. 1). Since the capacitor voltage deviates from the MPPT point of the energy source, the transfer efficiency to the capacitor is reduced. However, since the charge pump operates at a much higher power level (μW) during transfer mode, its efficiency dramatically improves.

Using these two modes, the discontinuous harvester decouples the two main losses and allows us to optimally trade them off, enabling efficient operation across a very wide range of input power (23,000× in our implementation). An asynchronous mode controller with <15pW power consumption controls the mode switch. It maintains a constant power source voltage fluctuation (ΔV_{sol} in Fig. 1), thereby automatically increasing the duty cycle at low input power levels and maintaining optimal end-to-end efficiency. We further propose a moving-sum charge pump that was designed for low start-up energy, which reduces overhead during the harvest to transfer mode transition. In measurement, the harvester obtains 37% end-to-end efficiency at 66pW input power drawn from a 0.01mm^2 solar cell at 6 lux and has a maximum input power of 1.5μW.

Harvester Implementation

Fig. 2 shows the overall architecture of the proposed harvester, which consists of C_{buf}, an always-on mode controller, and a harvester in a gated power domain. During harvest mode, S1–3 are open to limit leakage from the battery and C_{buf} to 2.6pW (simulation). V_{sol} is monitored by an asynchronous mode controller; when V_{sol} crosses V_{ref_H} the mode controller switches to transfer mode. This closes S1–3, enabling power transfer from C_{buf} to the battery, and enters a *startup* phase where the charge pump conversion ratio is initialized while the clock and logic operate from the battery (4V). After the pump voltages stabilize, the system enters *operation* mode and switches to an internally generated 1.2V supply to reduce switching power loss. Since the charge pump transfers charge from a capacitor and not a variable current source, the optimal pump frequency can be predetermined for both startup and operation modes, which significantly simplifies the charge pump design. The clock frequency change from startup to operation mode is performed by a glitch-free clock mux. As the charge pump drains C_{buf}, V_{sol} drops and an automatic conversion ratio modulator (ACRM) adjusts the conversion ratio to maintain optimum efficiency. When $V_{sol} < V_{ref\_L}$, the mode controller power gates the pump and changes to harvest mode.

A low-power mode controller is a key requirement that determines the lower bound of harvestable input power. An asynchronous design is used to save clock and logic power (Fig. 3). The mode is stored in flip-flop D1, which toggles based on comparators C1 and C2. The controller has < 100 gates, implemented in thick-oxide I/O devices, and consumes <15pW (measured). A diode stack is used to lower supply voltage from 4V to 1.6V, reducing the impact of GIDL.

In transfer mode, the conversion ratio is modulated based on $\Delta V = V_{in} * R - V_{out}$, where R is the conversion ratio and ΔV is an indicator of conduction loss. The ACRM (Fig. 4) approximates ΔV by multiplying input voltage V_{solar_pg} by $M*(R+1) = V_{mult}$, where M is a fixed weight and R is the current conversion ratio (Fig. 4). V_{mult} is then compared to a fixed threshold V_{ref_ACRM}. If $V_{mult} < V_{ref\_ACRM}$, a ratio counter increments, changing the conversion ratio to R+1. Multiplication is done by a switched-capacitor amplifier. Switch drivers for this amplifier are supplied by an auxiliary 2:1 DC-DC converter to reduce power consumption. The ACRM is duty cycled and only enabled every three SYSCLK cycles. After each modulation, ACRM shuts down its clock by itself.

As shown in Fig. 5 a 3-phase moving-sum charge pump is proposed to reduce startup energy. Charge in flying capacitors leak away during harvest mode and need to be restored during startup phase, presenting a power overhead. A traditional Dickson charge pump maintains high efficiency in operation mode, but startup energy is high due to the large number of flying caps and their high voltage potential. We design a “moving-sum” charge pump that consists of a Dickson charge pump with only 10 stages, followed by a modified series-parallel (S-P) charge pump with 4 flying caps to boost conversion ratio. In phases A and B, the Dickson stage operates conventionally except that four selected voltages are connected to the four flying caps in S-P stage. In phase C, the four S-P flying caps are connected in series to achieve 10–20× conversion ratios.

Measurement Results

The test chip is fabricated in 180nm CMOS. First examining moving-sum charge pump and ACRM performance, measured results in Fig. 6 show that the conversion ratio chosen by ACRM is within 2 of optimal, yielding < 10% efficiency degradation. The moving-sum charge pump achieves 60% peak efficiency at 256nW output power, and operates effectively across an output range of 4.2nW to 4μW (Fig. 7). We quantify the trade-off between startup energy and pump overhead (i.e., transfer phase efficiency) vs. solar cell efficiency by sweeping ΔV_{sol} in Fig. 8, with overall efficiency peaking at 120mV. Proposed harvester efficiency is measured with C_{buf} of 35.2μF, battery voltage of 3.8–4.2V, and a 0.01mm^2 solar cell as the energy source. The measured range of harvestable input power is 66pW to 1.5μW, marking a 23,000× range (Fig. 9). End-to-end efficiency of 37% is achieved at 6 lux with 66pW input power, and >30% efficiency is maintained up to a maximum power of 1.5μW at 43klux. Table 1 compares to prior work and shows 18× lower minimum harvestable power and 23× wider output power range.

References

1. Jung W, et al. ISSCC. 2014
2. Bandyopadhyay S, et al. ISSCC. 2014
3. Chen P, et al. ISSCC. 2015
4. Chew K, et al. ISSCC. 2013

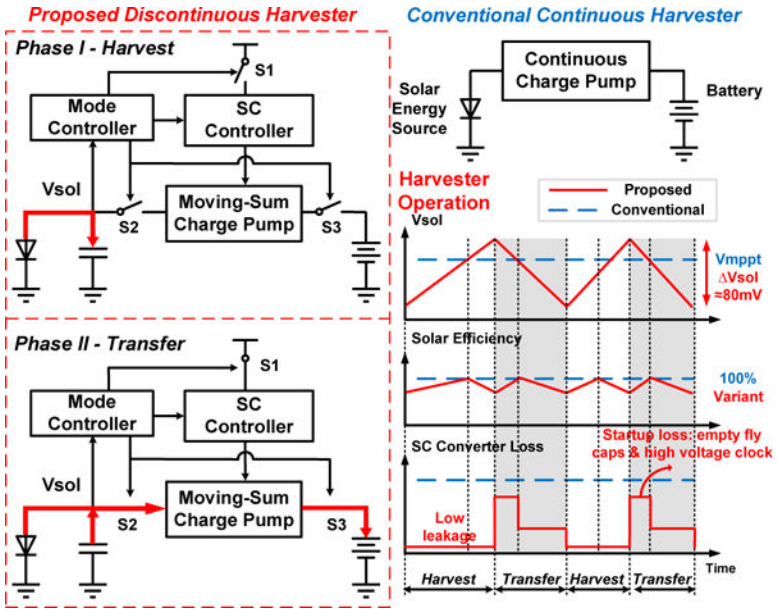

Figure 1.

Conventional and proposed discontinuous energy harvesting and associated energy trade-offs for a solar cell example

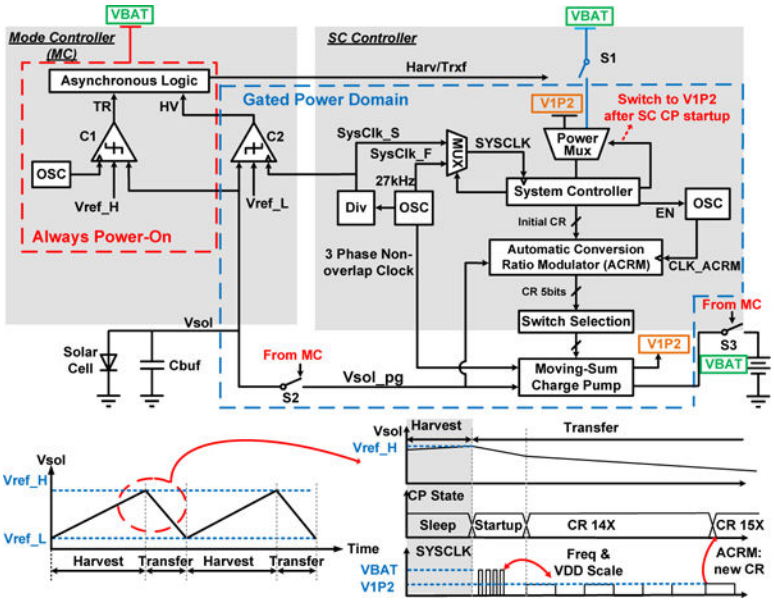

Figure 2.
Overall architecture and phase transition diagram

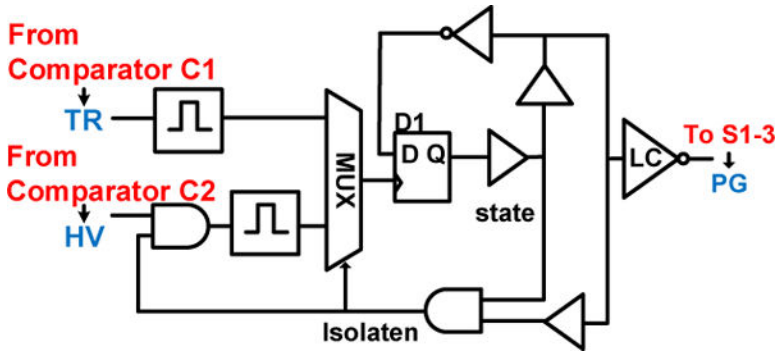

Figure 3.
Low leakage asynchronous logic for mode controller

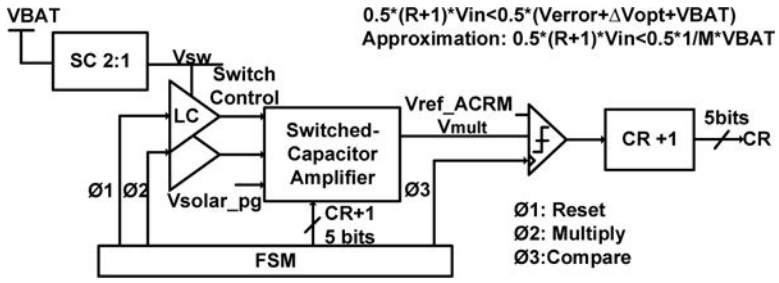

Figure 4.
ACRM circuit and working principle

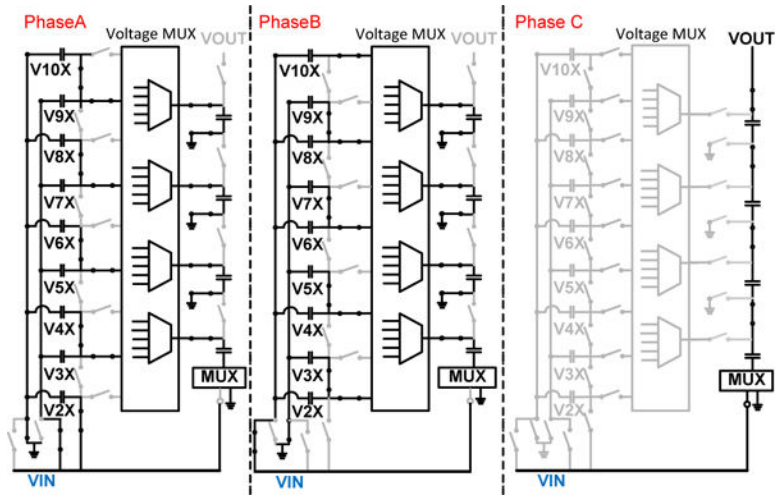

Figure 5.
Circuit implementation and operation of moving-sum charge pump

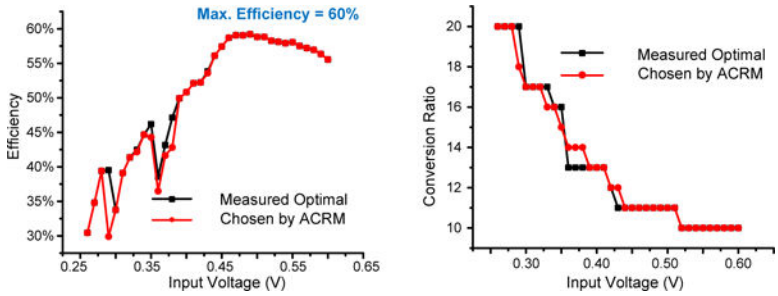

Figure 6.
Moving-sum CP measurements

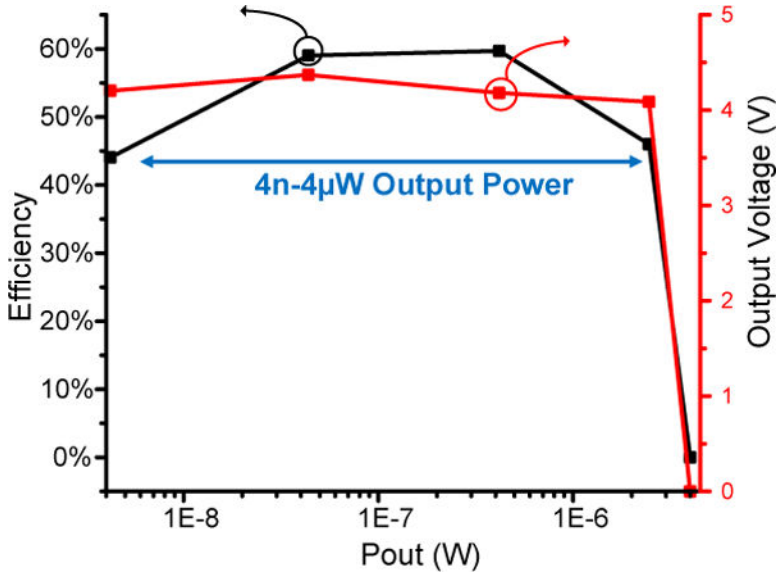

Figure 7.
Moving-sum CP measurement

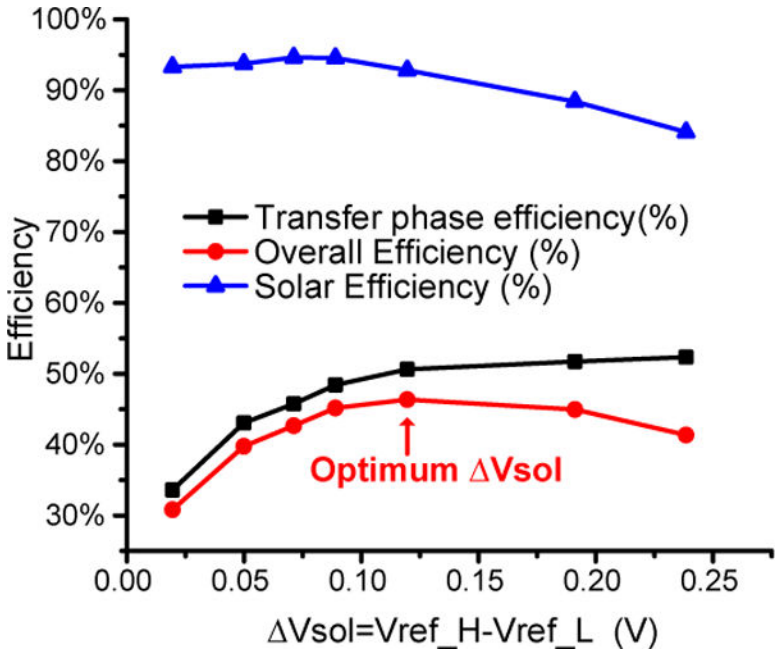

Figure 8.
Measured transfer vs. solar efficiency trade-off

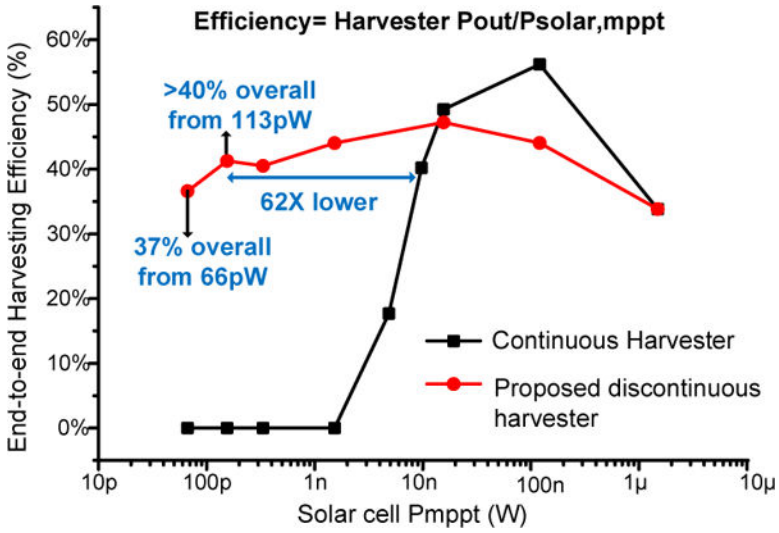

Figure 9.
Measured Harvester efficiency

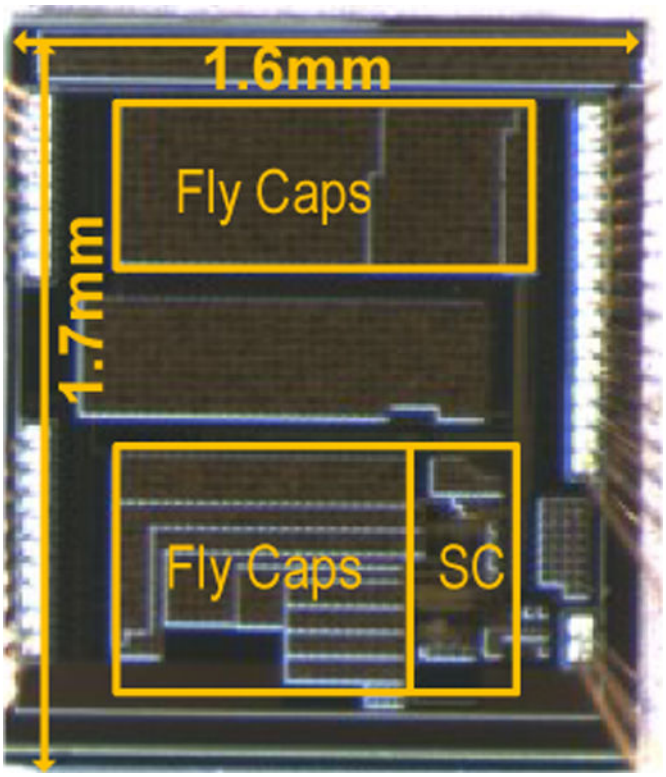

Figure 10.
Die photo in 180nm CMOS

Table 1

Performance summary and comparison

Metric	[1]	[2]	[4]	This Work
Technology	0.18µ	0.18µ	0.18µ	0.18µ
Topology	Switched-Capacitor	Boost with Voltage Doubler	Buck boost	Switched-Capacitor
Input voltage	0.14–0.5V	20–70mV	N/R	0.25–0.65V
Output voltage	2.2–5.2V	1.5–1.9V	1V,1.8V and 3V	3.8–4V
CP Peak Efficiency	50% @ 0.45V	56% @ 0.1V	N/R	60% @ 0.5V
End-to-end Peak Efficiency	50% @ 100nW output power[1]	56% @ 0.9nW output power[1]	83% @ 90µW[1]	50% @ 8nW
Output Power Range	5nW – 5µW w/>40% efficiency	544pW-4nW	1µW–10mW w/> 68% efficiency	64pW – 1.5µW w/>40% efficiency
Efficiency at minimum input power	> 30% @ 4.5nW	53% @ 1.2nW	68% @ 1.47µW	37% @ 66pW
Harvestable Power Range (Pout,max/Pout,min)	1000	7.4	10000	23000
Idle Power Consumption	3nW	544pW	400nW	15pW

N/R: Not reported

[1]Estimated number from the paper