Latency-aware Unified Dynamic Networks for Efficient Image Recognition

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Abstract—Dynamic computation has emerged as a promising strategy to improve the inference efficiency of deep networks. It allows selective activation of various computing units, such as layers or convolution channels, or adaptive allocation of computation to highly informative spatial regions in image features, thus significantly reducing unnecessary computations conditioned on each input sample. However, the practical efficiency of dynamic models does not always correspond to theoretical outcomes. This discrepancy stems from three key challenges: 1) The absence of a unified formulation for various dynamic inference paradigms, owing to the fragmented research landscape; 2) The undue emphasis on algorithm design while neglecting scheduling strategies, which are critical for optimizing computational performance and resource utilization in CUDA-enabled GPU settings; and 3) The cumbersome process of evaluating practical latency, as most existing libraries are tailored for static operators. To address these issues, we introduce Latency-Aware Unified Dynamic Networks (LAUDNet), a comprehensive framework that amalgamates three cornerstone dynamic paradigms—spatially-adaptive computation, dynamic layer skipping, and dynamic channel skipping—under a unified formulation. To reconcile theoretical and practical efficiency, LAUDNet integrates algorithmic design with scheduling optimization, assisted by a latency predictor that accurately and efficiently gauges the inference latency of dynamic operators. This latency predictor harmonizes considerations of algorithms, scheduling strategies, and hardware attributes. We empirically validate various dynamic paradigms within the LAUDNet framework across a range of vision tasks, including image classification, object detection, and instance segmentation. Our experiments confirm that LAUDNet effectively narrows the gap between theoretical and real-world efficiency. For example, LAUDNet can reduce the practical latency of its static counterpart, ResNet-101, by over 50% on hardware platforms such as V100, RTX3090, and TX2 GPUs. Furthermore, LAUDNet surpasses competing methods in the trade-off between accuracy and efficiency. Code is available at: https://www.github.com/LeapLabTHU/LAUDNet.

Index Terms—Dynamic networks, Efficient inference, Convolutional neural networks, Vision Transformers.

1 Introduction

DEEP neural networks have demonstrated exceptional capabilities in various domains such as computer vision [1], [2], [3], [4], [5], natural language processing [6], [7], [8], [9], and multi-modal understanding/generation [10]. Despite their stellar performance, the intensive computational requirements of these deep networks often limit their deployment on resource-constrained platforms, like mobile phones and IoT devices, highlighting the need for more efficient deep learning models.

Unlike traditional static networks [2], [3], [4] which process all inputs uniformly, dynamic models [11] adaptively allocate computation in a data-dependent fashion. This adaptivity involves bypassing certain network layers [12], [13], [14], [15] or convolution channels [16], [17] conditionally, and executing spatially adaptive inference that concentrates computational effort on the most informative regions of an image [18], [19], [20], [21], [22], [23]. As the field evolves and various dynamic models show promise, it begs the question: How can we design a dynamic network for practical use?

Addressing this question is challenging due to difficulties in fairly comparing different dynamic-computation paradigms. These challenges fall into three categories: 1) The lack of a unified framework to encompass different paradigms, as research in this area is often fragmented; 2) The focus on algorithm design, which often results in the mismatch between practical efficiency and their theoretical computational potential, due to the significant impact of scheduling strategies¹ and hardware properties on real-world latency; 3) The laborious task of evaluating a dynamic model's latency on different hardware platforms, as common libraries (e.g. cuDNN) are not built to accelerate many dynamic operators.

In response, we introduce a Latency-Aware Unified Dynamic Network (LAUDNet), a framework that unifies three representative dynamic-inference paradigms. Specifically, we examine the algorithmic design of layer skipping, channel skipping, and spatially dynamic convolution, integrating them through a "mask-and-compute" scheme (Fig. 1 (a)).

Next, we delve into the challenges of translating theoretical efficiency into tangible speedup, especially on multi-core processors such as GPUs. Traditional literature commonly adopts hardware-agnostic FLOPs (floating-point operations) as a crude efficiency measure, failing to provide latency-aware guidance for algorithm design. In dynamic networks,

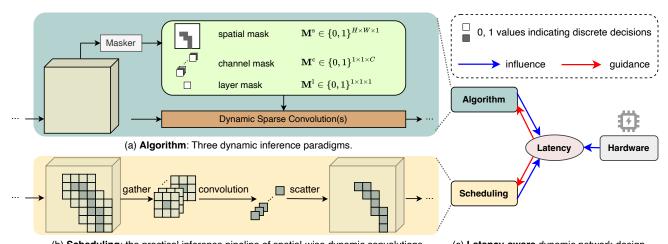
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^{1.} Scheduling strategies are essential for practical efficiency because they optimize the use of GPU threads and memory with CUDA codes.



(b) **Scheduling**: the practical inference pipeline of spatial-wise dynamic convolutions. (c) Latency-aware dynamic network design. Fig. 1: An overview of our method. (a) illustrates three representative adaptive inference algorithms (i.e. spatial-wise dynamic

convolution, channel skipping, and layer skipping); (b) is an example of the scheduling strategy for spatial-wise dynamic convolution; and (c) presents our key idea of using the latency to guide both algorithm design and scheduling optimization.

adaptive computation coupled with sub-optimal scheduling strategies intensifies the gap between FLOPs and latency. Moreover, most existing methods execute adaptive inference at the finest granularity. For instance, in spatial-wise dynamic inference, the decision to compute each feature pixel is made independently [19], [20], [21]. This fine-grained flexibility results in non-contiguous memory access [21], necessitating specialized scheduling strategies (Fig. 1 (b)).

Given that dynamic operators exhibit unique memory access patterns and scheduling strategies, libraries designed for static models, like cuDNN, fail to optimize dynamic models effectively. The lack of library support implies that each dynamic operator requires individualized scheduling optimization, code refinement, compilation, and deployment, making network latency evaluation across hardware platforms labor-intensive. To address this, we propose a novel latency prediction model that efficiently estimates network latency by taking into account algorithm design, scheduling strategies, and hardware properties. Compared to hardwareagnostic FLOPs, our predicted latency offers a more realistic representation of dynamic model efficiency.

Guided by the latency prediction model, we tackle the aforementioned challenges within our latency-aware unified dynamic network (LAUDNet) framework. For a given hardware device, we use the predicted latency as the guiding metric for algorithm design and scheduling optimization, as opposed to the conventionally used FLOPs (Fig. 1 (c)). In this context, we propose coarse-grained dynamic networks where "whether-to-compute" decisions are made at the patch/group level rather than individual pixels/channels. Though less flexible than pixel/channellevel adaptability in prior works [16], [17], [19], [20], [21], this approach encourages contiguous memory access, enhancing real-world speedup on hardware. Our improved scheduling strategies further permit batching inference. We investigate dynamic inference paradigms, focusing on the accuracylatency trade-off. Notably, previous research has established a correlation between latency and FLOPs on CPUs [21], [23], hence in this paper, we primarily target the GPU platform, a more challenging but less explored environment.

The LAUDNet is designed as a general framework in two

ways: 1) Multiple adaptive inference paradigms can be easily implemented in various vision backbones, like ResNets [2], RegNets [24] and vision Transformers [25], [26]; and 2) The latency predictor functions as an off-the-shelf tool that can be readily applied to diverse computing platforms, such as server-end GPUs (Tesla V100, RTX3090), desktop-level GPU (RTX3060) and edge devices (Jetson TX2, Nvidia Nano).

We evaluate LAUDNet's performance across multiple backbones for image classification, object detection, and instance segmentation. Our results show that LAUDNet significantly improves the efficiency of deep CNNs, both in theory and practice. For instance, the inference latency of ResNet-101 on ImageNet [1] is reduced by >50% on different types of GPUs (e.g., V100, RTX3090 and TX2), without compromising accuracy. Moreover, our method outperforms various lightweight networks in low-FLOPs scenarios.

Although parts of this work were initially published in a conference version [27], this paper significantly expands our previous efforts in several key areas:

- A unified dynamic-inference framework is proposed. While the preliminary paper [27] predominantly focused on spatially adaptive computation, this paper delves deeper into two additional and important dynamic paradigms, specifically, dynamic layer skipping and channel skipping (Fig. 1 and Sec.3.1). Furthermore, we integrate these paradigms into a unified framework, and provide more thorough study on architecture design and complexity analysis (Sec.3.2).
- The latency predictor has been enhanced to support an expanded set of dynamic operators, including layer skipping and channel skipping (Sec. 3.3). Moreover, we adopt Nvidia Cutlass [28] to optimize the scheduling strategies. Hardware evaluations demonstrate that our latency predictor can accurately predict the latency on real hardware (Fig. 5).
- The LAUDNet framework has been extended to accommodate Transformer architectures, as detailed in Sec. 3.2. This extension notably enhances latency optimization through the implementation of dynamic token skipping (spatially adaptive computation), head (channel) skipping, and layer skipping. Such ad-

vancements significantly broaden the applicability of LAUDNet. The empirical evaluation, illustrated in Fig. 10 (c) and discussed in Sec. 4.3.2, yields valuable insights into the design of efficient Transformers, underpinning the framework's versatility and efficacy.

- For the first time, we incorporate batching inference for our dynamic operators (Sec. 3.4). This innovation leads to more consistent prediction outcomes and an enhanced speedup ratio on GPU platforms (Fig. 8, 12).
- We undertake an exhaustive analysis of various dynamic granularities (Fig. 9) and paradigms (Fig. 10,11,13, Tab. 2,3), spanning different vision tasks and platforms, with added evaluations on contemporary GPUs like RTX3060 and RTX3090. We are confident that our results will offer valuable insights to both researchers and practitioners.

2 RELATED WORKS

Efficient deep learning has garnered substantial interest. Traditional solutions involve lightweight model design [29], [30], [31], [32], network pruning [33], [34], [35], [36], weight quantization [37], [38], [39], [40], and knowledge distillation [41], [42]. However, these *static* methods have sub-optimal inference strategy, leading to intrinsic redundancy since they process all inputs with equal computation.

Dynamic networks [11], [12], [18], [43] propose an appealing alternative to static models by enabling input-conditional dynamic inference. This adaptive approach has yielded superior results across various domains. In visual recognition, prevalent dynamic paradigms include early exiting [12], [13], [44], layer skipping [14], [15], [43], channel skipping [16], [17], [45], and spatial-wise dynamic computation [19], [20], [21]. This paper primarily targets the latter three paradigms, as they can be readily applied to arbitrary visual backbones, thereby offering a generality advantage. Layer skipping and channel skipping explore structural redundancy within deep networks by selectively activating computation units, such as layers or convolution channels when processing different inputs. Spatial-wise dynamic models alleviate spatial redundancy in image features and selectively assign computation to the regions most pertinent to the task at hand.

Despite their effectiveness, previous studies often fail to recognize the shared underlying formulation across different dynamic paradigms. In contrast, we introduce a unified framework that encompasses all three paradigms, facilitating a thorough exploration of dynamic networks. Additionally, existing methods primarily concentrate on algorithm design, which often results in a significant disparity between theoretical and practical efficiency. In our latency-aware codesign framework, we bridge this gap by utilizing latency directly from our latency predictor to guide both algorithm design and scheduling optimization. This approach results in improved latency performance across diverse platforms. Hardware-aware network design. Researchers have acknowledged the necessity to bridge the gap between theoretical and practical efficiency of deep models by considering actual latency during network design. Two primary approaches have emerged: the first entails conducting speed tests on hardware and deriving guidelines to facilitate hand-designing

lightweight models [32], and the second involves performing

speed tests for various types of *static* operators and modeling the latency predictor as a small trainable model [46], [47], [48], [49]. Neural architecture search (NAS) techniques [50], [51] are then used to *search* for hardware-friendly models.

Our work distinguishes itself from these approaches in two significant ways: 1) while existing works predominantly focus on constructing *static* models that inherently exhibit computational redundancy by treating all inputs uniformly, our goal is to design latency-aware *dynamic* models that adjust their computation based on inputs; 2) conducting speed tests for dynamic operators across various hardware devices can be laborious and impractical. To circumvent this, we propose a latency prediction model that efficiently estimates the inference latency of dynamic operators on any given computing platform. This model accounts for algorithm design, scheduling strategies, and hardware properties simultaneously, providing valuable insights without the need for extensive speed testing.

3 METHOD

This section begins by providing an introduction to the foundational concepts underlying three dynamic inference paradigms (Sec. 3.1). We then present the architecture design of our LAUDNet framework, which unifies these paradigms under a cohesive *mask-and-compute* formulation (Sec. 3.2). Next, we explain the latency prediction model (Sec. 3.3), which guides the determination of granularity settings and scheduling optimization (Sec. 3.4). Finally, we describe the training strategies for our LAUDNet (Sec. 3.5).

3.1 Preliminaries

Spatially adaptive computation. Existing spatial-wise dynamic networks typically incorporate a masker \mathcal{M}^s within each convolutional block of a CNN backbone. Given an input $\mathbf{x} \in \mathbb{R}^{H \times W \times C}$ to a block, where H and W represent the feature height and width, and C denotes the channel number. Assuming a convolution stride of 1, the masker \mathcal{M}^s takes \mathbf{x} as input and generates a binary-valued spatial mask $\mathbf{M}^s = \mathcal{M}^s(\mathbf{x}) \in \{0,1\}^{H \times W}$. Each element in \mathbf{M}^s determines whether to perform convolution operations at the corresponding output location. Unselected regions are populated with values from skip connection [19], [20].

During inference, the current scheduling strategy for spatial-wise dynamic convolutions generally involve three steps [52] (Fig. 1 (b)): 1) *gathering*, which re-organizes the selected pixels (if the convolution kernel size is greater than 1 × 1, the neighbors are also required) along the *batch* dimension; 2) *computation*, which performs convolution on the gathered input; and 3) *scattering*, which fills the computed pixels on their corresponding locations of the output feature. Compared to performing convolutions on the entire feature map, this scheduling strategy reduces computation at the cost of overhead from mask generation and non-contiguous *memory access*. As a result, the overall latency could even be increased, particularly when the *granularity* of dynamic convolution is at the pixel level (Fig. 6).

Dynamic layer skipping [14], [15], [53] adaptively determines whether to execute each layer or block, leveraging the structural redundancy of deep models to achieve data-dependent network *depth*. The implementation of dynamic

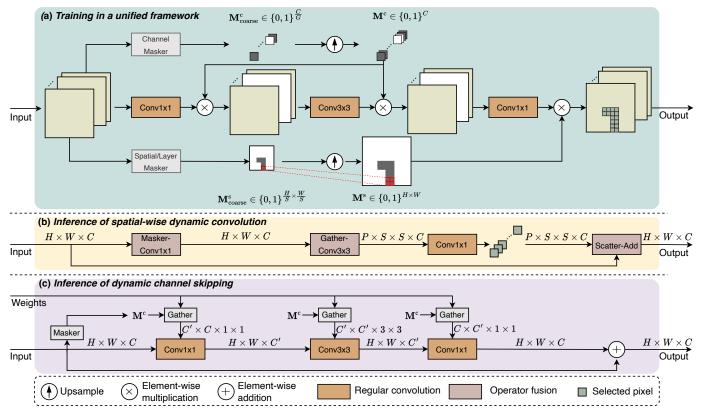


Fig. 2: Our proposed LAUDNet block. (a) we first use a lightweight module to generate the channel mask \mathbf{M}^c or the spatial/layer mask $\mathbf{M}^s/\mathbf{M}^l$. The granularity of dynamic inference is controlled by G (for channel skipping) and S (for spatially adaptive computation). During training, the channel mask is multiplied with the input and output of the 3×3 convolution, and the spatial mask is applied on the final output of the block. Layer skipping could be easily implemented by setting S equal to the feature resolution. The scheduling strategies in inference ((b) for spatial-wise dynamic convolution and (c) for channel skipping) is performed to decrease memory access and facilitate parallel computation (Sec. 3.4). Note that we omit layer skipping here due to its simplicity: the whole block will be executed if the layer masker produces a value of 1.

layer skipping is similar to spatially adaptive inference, but with a scalar 0,1 decision variable \mathbf{M}^l instead of a spatial $H\times W$ mask. Compared to spatially adaptive inference, layer skipping provides less flexibility but more regular computation patterns. Moreover, it generally does not require special scheduling strategies, as the original convolution operators remain unmodified.

Dynamic channel skipping [16], [17], [54] takes a more conservative approach to dynamic architecture versus full layer skipping. It uses a C-dimensional vector $\mathbf{M}^c \in \{0,1\}^C$ to adaptively determine the runtime width of a convolution layer with C output channels. For instance, the i-th $(1 \le i \le C)$ channel is computed only if $\mathbf{M}_i^c = 1$. The scheduling of dynamic channel skipping usually requires gathering convolution kernels instead of feature pixels as in spatially dynamic computation (compare Fig. 2 (b) and (c)) .

3.2 LAUDNet architecture

Overview. Our analysis in Sec.3.1 reveals that the three dynamic inference paradigms share a common "mask-and-compute" scheme, with the key difference being the mask shapes. Leveraging this insight, we propose a unified framework (Fig.2) where lightweight modules generate the channel mask \mathbf{M}^{c} and the spatial/layer mask $\mathbf{M}^{\mathrm{s/l}}$, respectively. Notably, layer skipping can be treated as a special case of spatially adaptive inference by introducing the concept of granularity in dynamic computation as follows.

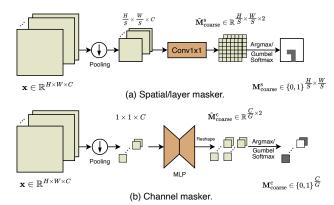


Fig. 3: The architecture design of two types of maskers. The spatial/layer masker (a) is composed of a an adaptive pooling layer and a 1×1 convolution. The channel maker (b) consists of a global average pooling and a 2-layer MLP. The argmax operation is directly applied to obtain the discrete decisions during inference, while Gumbel Softmax [55], [56] is utilized for end-to-end training (Sec. 3.5).

Dynamic granularity. As mentioned in Sec. 3.1, using *pixel*-level dynamic convolutions [19], [20], [21] poses substantial challenges for realistic speedup on multi-core processors due to non-contiguous memory access. To address this, we propose to optimize the *granularity* of dynamic computation. For spatially adaptive inference, instead of producing an $H \times W$ mask directly, we first generate a low-resolution

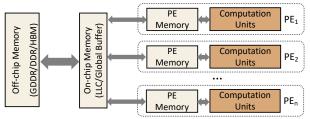


Fig. 4: Our hardware model, which allows us to model the latency of both data moving and computation.

mask $\mathbf{M}_{\mathrm{coarse}}^{\mathrm{s}} \in \{0,1\}^{\frac{H}{S} \times \frac{W}{S}}$, where S is the spatial granularity. Each element in $\mathbf{M}_{\mathrm{coarse}}^{\mathrm{s}}$ determines computation for a corresponding $S \times S$ feature patch. For instance, the first ResNet stage² deal with 56×56 features. Then the valid choices for S are $\{1,2,4,7,8,14,28,56\}$. The mask $\mathbf{M}_{\mathrm{coarse}}^{\mathrm{s}}$ is then upsampled to the size of $H \times W$. Notably, S=1 corresponds to pixel-level granularity [19], [20], [21], while S=56 naturally implements layer skipping.

Similarly, we introduce channel granularity G for channel skipping. Each element in $\mathbf{M}^{\mathrm{c}}_{\mathrm{coarse}} \in \{0,1\}^{\frac{C}{G}}$ determines computation for G feature channels. The choice of the spatial granularity S and the channel granularity G for each block will be guided by our latency predictor (Sec. 3.3) for balancing flexibility and efficiency. Note that we apply the channel mask at the first two convolution layers within a block. This design is compatible with various backbone architectures, including those with arbitrary bottleneck ratios or group convolutions [24].

Masker design. We design different structures for spatial (layer) and channel-wise dynamic computation. As shown in Fig. 3 (a), the spatial masker uses an adaptive pooling layer to downsample the input $\mathbf x$ to the size of $\frac{H}{S} \times \frac{W}{S} \times C$, followed by a 1×1 convolution layer producing the soft logits $\mathbf{M}^{\mathbf s}_{\mathrm{coarse}} \in \mathbb{R}^{\frac{H}{S} \times \frac{W}{S} \times 2}$. For the channel masker, we use a 2-layer MLP (Fig. 3 (b)) to produce channel-skipping decisions. Given input channels C the target mask dimension D = C/G, we set the hidden units in the MLP as $\max\{\lfloor D/16 \rfloor, 16\}$, where $\lfloor \cdot \rfloor$ denotes a round-down operation. Appendix C.1 shows this design effectively reduces the latency of channel maskers, especially in late stages with more channels.

Computational complexity. We first point out that the masker FLOPs are negligible compared to the backbone convolutions. Therefore, we mainly analyse the complexity of standard convolution blocks here.

For spatially adaptive computation, We define the *activation ratio* $r^{\mathrm{s}} = \frac{\sum_{i,j} \mathbf{M}_{i,j}^{\mathrm{s}}}{H \times W} \in [0,1]$ to denote the fraction of computed pixels. Following [20], we further compute $r_{\mathrm{dil}}^{\mathrm{s}}$ of a dilated spatial mask to represent the activation ratio of the first convolution in a block. It is observed in our experiments that $r_{\mathrm{dil}}^{\mathrm{s}}$ is generally close to r^{s} . With FLOPs F_1, F_2, F_3 for the three convolution layers, the *theoretial* speedup is $\frac{r_{\mathrm{dil}}^{\mathrm{s}} F_1 + r^{\mathrm{s}} F_2 + r^{\mathrm{s}} F_3}{F_1 + F_2 + F_3} \approx r^{\mathrm{s}}$.

For channel skipping, the activation ratio is $r^{\rm c}=\frac{\sum_j \mathbf{M}_i^{\rm c}}{C} \in [0,1]$. Apply the mask before and after the 3×3 convolution makes its complexity quadratic with respect to $r^{\rm c}$. The overall speedup is $\frac{r^{\rm c}F_1+(r^{\rm c})^2F_2+r^{\rm c}F_3}{F_1+F_2+F_3} \leq r^{\rm c}$.

2. Here we refer to a stage as the cascading of multiple blocks which process features with the same resolution.

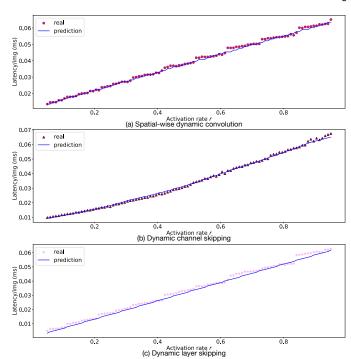


Fig. 5: Comparison between the real and predicted latency of a dynamic block in LAUD-ResNet-101.

Generalization in Transformer architectures. It is essential to highlight that the implementation of the three dynamic paradigms—namely spatial-wise adaptive computation, dynamic channel selection, and layer skipping—is inherently more straightforward in vision Transformers compared to CNNs. These paradigms are not only more amenable to hardware considerations, requiring minimal scheduling optimization, but also benefit from the inherent structure of vision Transformers. For instance, spatial-wise dynamic computation can be efficiently executed through token indexing and selection, thanks to the image tokenization process in vision Transformers, thereby avoiding the complex pixel gathering required in convolution layers (Fig. 2 (b)). From an algorithmic design perspective, the recent AdaViT framework [57] introduces a method for adaptively skipping tokens, heads/channels in multi-head attention, and layers, thus enabling dynamic computation across spatial, width, and depth dimensions simultaneously. However, despite theoretical comparisons presented in [57], the practical efficacy of these paradigms on hardware remains uncertain. This paper leverages the architectural design principles of AdaViT to circumvent the need for foundational redesigns and utilizes our proposed latency predictor to conduct a thorough examination of the practical performance of these dynamic paradigms in vision Transformers.

3.3 Latency predictor

As stated before, it is laborious to evaluate the latency of dynamic operators on different hardware platforms. To efficiently seek preferable dynamic paradigms and granularity settings on any target device, we propose a latency prediction model \mathcal{G} . Given hardware properties \mathbf{H} , layer parameters \mathbf{P} , dynamic paradigm \mathbf{D} , spatial/channel granularity S/C, and activation rates r^s/r^c , \mathcal{G} directly *predicts* block execution latency $\ell = \mathcal{G}(\mathbf{H}, \mathbf{P}, \mathbf{D}, S, C, r^s, r^c)$.

Hardware modeling. We model a device with multiple processing engines (PEs) for parallel computation (Fig. 4). The memory system has three levels [58]: 1) off-chip memory, 2) on-chip global memory, and 3) memory in PE. In practice, the latency mainly comes from two processes: *data movement* and *parallel computation*:

$$\ell = \ell_{\text{data}} + \ell_{\text{computation}} + \ell_{\text{Const}}, \tag{1}$$

where $\ell_{\rm Const}$ is a hardware-specific constant. This model accurately predicts both $\ell_{\rm data}$ and $\ell_{\rm computation}$, enabling more practical efficiency measurement than FLOPs.

Latency prediction. Given hardware properties and model parameters, adopting a proper *scheduling strategy* is key to maximizing resource utilization through increased parallelism and reduced memory access. We use Nvidia Cutlass [28] to *search* for the optimal scheduling (tiling and in-PE parallelism configurations) of dynamic operations. The data movement latency can then be easily obtained from data shapes and target device bandwidth. Furthermore, the computation latency is derived from hardware properties. Please refer to Appendix A for more details.

Empirical validation. We evaluate the performance of our latency predictor with a ResNet-101 block on an RTX3090 GPU, varying the activation rate r. The blue curves represent the predictions, and the scattered dots are obtained via *searching* for a proper scheduling strategy (implemented with custom CUDA code) using Nvidia Cutlass [28]. All the three dynamic paradigms are tested. Fig. 5 compares predictions to real GPU testing latency, showing accurate estimates across a wide range of activation rates.

3.4 Scheduling optimization

We use general optimization methods like fusing activation functions and batch normalization (BN) layers into convolution layers. We also optimize our dynamic convolution blocks as follows.

Operator fusion for spatial maskers. As mentioned in Sec. 3.2, spatial maskers have negligible computation but take the full feature map as input, making them *memory-bounded* (latency is dominated by memory access). Since the masker shares its input with the first 1×1 conv (Masker-Conv 1×1 in Figure 2 (b)), fusing them avoids repeated input reads. However, this makes the convolution spatially static, potentially increasing computation. For simplicity, we adopt such operator fusion in all tested models. In practice, we find that operator fusion improves efficiency in most scenarios.

Fusing gather and dynamic convolution. Traditional approaches first gather the input pixels of the first dynamic convolution in a block. The gather operation is also a *memory-bounded* operation. Furthermore, when the kernel size exceeds 1×1 , input patches overlap, leading to repeated loads/stores. We fuse gathering into dynamic convolution to reduce the memory access (Gather-Conv3x3 in Fig. 2 (b)).

Note that for dynamic channel skipping (Fig. 2 (c)), gathering is conducted on convolution kernels rather than features. The weight gather operations is also fused with convolution by our scheduling optimization.

Fusing scatter and add. Conventional methods scatter the final convolution outputs before the element-wise addition. We fuse these two operators (Scatter-Add in Fig. 2 (b)) to

reduce memory access costs. The ablation study in Sec. 4.2 validates the effectiveness of the proposed fusing methods. **Batching inference** is enabled by recording patch, location, and sample correspondences during gathering and scattering (Fig. 2 (b, c)). Inference with a larger batch size facilitates parallel computation, making latency more dependent on computation versus kernel launching or memory access. See Appendix C.1 for empirical analysis.

3.5 Training

Optimization of non-differentiable maskers. The masker modules produce binary variables for discrete decisions, and cannot be directly optimized with back-propagation. Following [20], [21], [23], we adopt straight-through Gumbel Softmax [55], [56] for end-to-end training. Take spatial-wise dynamic inference as an example, let $\tilde{\mathbf{M}}^{\mathbf{s}} \in \mathbb{R}^{H \times W \times 2}$ denote the output of the spatial mask generator $\mathcal{M}^{\mathbf{s}}$. The decisions are obtained with the argmax function during inference. Training uses a differentiable Softmax approximation:

$$\hat{\mathbf{M}}^{\mathbf{s}} = \frac{\exp\left\{ \left(\log \left(\tilde{\mathbf{M}}_{:,:,0}^{\mathbf{s}} \right) + \mathbf{G}_{:,:,0} \right) / \tau \right\}}{\sum_{k=0}^{1} \exp\left\{ \left(\log \left(\tilde{\mathbf{M}}_{:,:,k}^{\mathbf{s}} \right) + \mathbf{G}_{:,:,k} \right) / \tau \right\}} \in [0,1]^{H \times W}, \quad (2)$$

where τ is the Softmax temperature. Similarly, a channel masker \mathcal{M}^c produces a 2C-dimensional vector $\tilde{\mathbf{M}}^c \in \mathbb{R}^{2C}$, where C is the channel number of the 3×3 convolution in a block. We first reshape $\tilde{\mathbf{M}}^c$ into the size of $C \times 2$, and apply Gumbel Softmax along the second dimension to produce $\hat{\mathbf{M}}^c \in [0,1]^C$. Following [20], [23], we let τ decay exponentially from 5.0 to 0.1 in training to facilitate the optimization of maskers.

Training objective. As analyzed in Sec. 3.2, the FLOPs of each dynamic convolution block can be calculated based on our defined activation rate $r^{\rm s}$ (or $r^{\rm c}$). Let $F_{\rm dyn}$ and $F_{\rm stat}$ denote the overall dynamic and static network FLOPs. We optimize their ratio to approximate a target 0 < t < 1: $L_{\rm FLOPs} = (\frac{F_{\rm dyn}}{F_{\rm stat}} - t)^2$. In addition, we define $L_{\rm bounds}$ as in [20] to constrain the upper/lower bounds in early training epochs.

We further propose to leverage the static counterparts of our dynamic networks as "teachers" to guide the optimization procedure. Let y and y' denote the output logits of a dynamic "student" model and its static "teacher", respectively. Our final loss can be written as

$$L = L_{\rm task} + \alpha (L_{\rm FLOPs} + L_{\rm bounds}) + \beta T^2 \cdot \text{KL}(\sigma(\mathbf{y}/T) || \sigma(\mathbf{y}'/T)), \quad (3)$$

where $L_{\rm task}$ represents the task-related loss, e.g., cross-entropy loss in classification. ${\rm KL}(\cdot||\cdot)$ denotes the Kull-back–Leibler divergence, and α,β are the coefficients balancing these items. We use σ to denote the log-Softmax function, and T is the temperature for computing KL-divergence.

4 EXPERIMENTS

In this section, we first introduce the experiment settings in Sec. 4.1. Then the latency of different granularity settings are analyzed in Sec. 4.2. The performance of our LAUDNet on ImageNet is further evaluated in Sec. 4.3, followed by the visualization results in Sec. 4.4. We finally validate our method on the object detection and instance segmentation tasks (Sec. 4.5). For simplicity, we add "LAUD $^{\rm s/c/l}$ -" as a

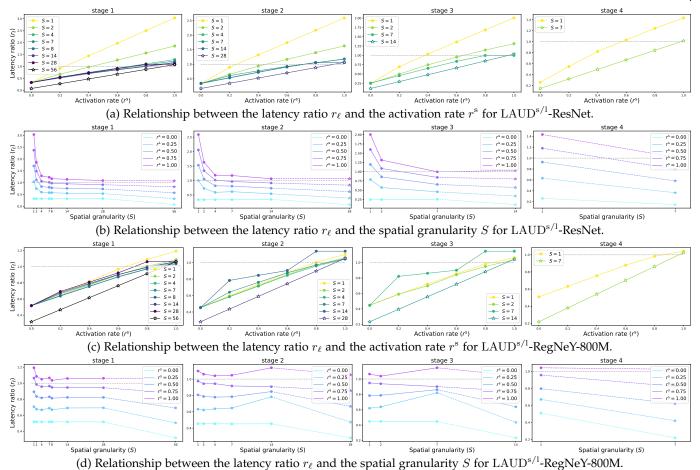


Fig. 6: Latency prediction results for LAUD^{s/l}-ResNet blocks on the Nvidia Tesla V100 GPU (a, b) and LAUD^{s/l}-RegNetY-800MF blocks on the Nvidia Jetson TX2 GPU (c, d). The circle markers (\bullet) represent spatial-wise dynamic computation, and the star markers (\star) denote layer skipping, which is implemented via the largest granularity S in each stage.

prefix before model names to denote our LAUDNet with different dynamic paradigms (s for spatial, c for channel and l for layer), *e.g.*, LAUD^s-ResNet-50.

4.1 Experiment setup

Image classification experiments are conducted on the ImageNet [1] dataset. We implement our LAUDNet on five representative architectures extending up to a broad spectrum of computational costs: four CNNs (ResNet-50, ResNet-101 [2], RegNetY-400M, RegNetY-800M [24]) and a vision Transformer, T2T-ViT [26]. Different training settings are used for CNNs and Transformers. For CNNs, As per the established methodology in [20], we initialize the backbone parameter from a torchvision pre-trained checkpoint (https://pytorch.org/vision/stable/models.html), and finetune the whole network for 100 epochs employing the loss function in Eq. (3). We fix $\alpha = 10$, $\beta = 0.5$ and T = 4.0 for all dynamic models. Note that we adopt the pretrain-fintune paradigm mainly to reduce the training cost, as Gumbel Softmax usually requires longer training for convergence. For our study on T2T-ViT, we use the same setup as described in AdaViT [57] and evaluate the efficiency of its various dynamic inference methods through our latency predictor. **Latency prediction.** We evaluate our LAUDNet on various types of hardware platforms, including two server GPUs (Tesla V100 and RTX3090), a desktop GPU (RTX3060) and two edge devices (e.g., Jetson TX2 and Nvidia Nano). The

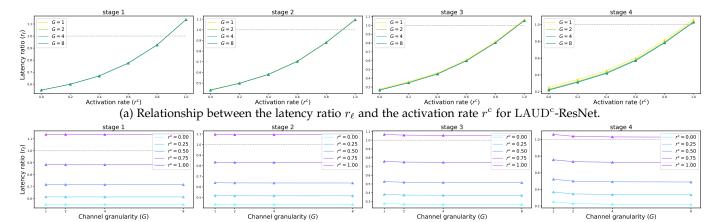
major properties considered by our latency prediction model include the number of processing engines (#PE), the floating-point computation in a processing engine (#FP32), the frequency and the bandwidth. It can be observed from Tab. 4 that server GPUs generally have a larger #PE than IoT devices. If not stated otherwise, the batch size is set as 128 for V100, RTX3090 and RTX3060 GPUs. On edge devices TX2 and Nano, tesing batch size is fixed as 1.

More details are provided in Appendix B.

4.2 Latency prediction results

This subsection presents the latency prediction results of dynamic convolutional blocks using two distinct backbones: ResNet-50 [2] (on V100) and RegNetY-800MF [24] (on TX2). Each block features a bottleneck structure with varying channel numbers and convolution groups, and the RegNetY employs Squeeze-and-Excitation (SE) [59] modules. We define $\ell_{\rm dyn}$ as the latency of a dynamic convolutional block and $\ell_{\rm stat}$ as the latency of a static block. The ratio of the two is denoted as $r_\ell = \frac{\ell_{\rm dyn}}{\ell_{\rm stat}}$, with a realistic speedup being achieved when $r_\ell < 1$.

Effect of spatial granularity. The primary objective here is to investigate how the *granularity* of dynamic computation impacts the latency ratio r_{ℓ} . We explore the correlation between r_{ℓ} and the activation rate $r^{\rm s}$ (refer to Sec. 3.2) for varying *granularity* settings. The results in Fig. 6a (ResNet on V100) and Fig. 6c (RegNetY-800M on TX2) demonstrate that:



(b) Relationship between the latency ratio r_{ℓ} and the channel granularity G for LAUD^c-ResNet. Fig. 7: Latency prediction results for LAUD^c-ResNet blocks on the Nvidia Tesla V100 GPU.

TABLE 1: Ablation studies on operator fusion.

Masker-Conv	Gather-Conv	Scatter-Add	Laten V100	cy (µs) TX2
X	×	×	162.4	1084.5
✓	X	×	135.1	1072.3
✓	✓	X	131.7	1024.7
✓	✓	✓	118.3	859.7

- Despite the implementation of our optimized scheduling strategies, pixel-level dynamic convolution (S=1) does not consistently enhance practical efficiency. This approach to fine-grained adaptive inference has been adopted in previous works [20], [21], [60]. Our findings help elucidate why these studies only managed to achieve realistic speedup on less potent CPUs [21] or specialized devices [60];
- By contrast, a coarse granularity setting (S>1) significantly mitigates this issue across both devices. Realistic speedup $(r_{\ell}<1)$ is attainable with larger activation values (r^s) when S>1.

The latency prediction results are further used to determine preferable spatial granularity settings for the first 3 stages. Note that for the final stage where the feature resolution is 7×7 , S=1 and S=7 correspond to two distinct dynamic paradigms (spatially adaptive inference and layer skipping). The relationship curves between r_ℓ and S depicted in Fig. 6b (ResNet on V100) and Fig. 6d (RegNetY-800M on TX2) reveal the following:

- The latency ratio r_{ℓ} generally decreases as S increases for a given r on V100;
- An excessively large S (indicating less flexible adaptive inference) provides negligible improvement on both devices. In particular, increasing S from 7 to 14 in the second stage of LAUD-RegNetY-800MF on TX2 detrimentally impacts efficiency. This is hypothesized to be due to the oversized patch size causing additional memory access costs on this device, which has fewer processing engines (PEs);
- Layer skipping (marked by ★) consistently outperforms spatial-wise dynamic computation (marked by
 •). We will analyze their performance across various vision tasks in Sec. 4.3 and Sec. 4.5.

Based on these results, we can strike a balance between flexibility and efficiency by choosing suitable S for different

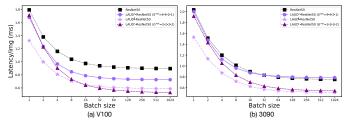


Fig. 8: Relationship between the latency per image and batch size of LAUD-ResNet-50 on V100 (a) and 3090 (b) GPUs.

models and devices. For instance, we can simply set S^{net} =4-4-2-1³ in a LAUD^s-ResNet-50 to achieve realistic speedup.

Effect of channel granularity. We further investigate how the channel granularity G influences the realistic latency of channel-skipping dynamic models. Using LAUD^c-ResNet as an example, results presented in Fig. 7 show that the performance of channel skipping is less sensitive to the channel granularity G. Setting G=2 improves efficiency only in deeper stages, while extending G beyond 2 offers diminishing benefits. This aligns with our understanding that channel skipping requires more regular operations compared to spatially sparse convolution, implying that G=1 can already employ impactful speedup. Moreover, the curves in Fig. 7a are generally convex, since the computation of the 3×3 convolution is quadratic in relation to r^c (Sec. 3.2).

Ablation study of operator fusion. In exploring the impact of our operator fusion, as detailed in Sec. 3.4, we focus on a convolutional block from the initial stage of LAUDs-ResNet-50 (S=4, rs=0.6) for our case study. The findings, presented in Tab. 1, reveal that operator fusion consistently aids in lowering the practical latency across different computing environments by minimizing memory access overhead. Notably, the fusion between the masker and the first convolution emerges as a significant factor in reducing latency on the server-end V100. In contrast, combining scattering and addition operations plays a pivotal role in latency reduction on the edge device TX2.

Ablation study of batch size. To establish a suitable testing batch size, we graph the relationship between latency per image and batch size for LAUD-ResNet-50 in Fig. 8. Two server-end GPUs (V100 and RTX3090) are tested. The results highlight that latency diminishes with an increase in batch

3. We use this form to represent the S settings for the 4 network stages.

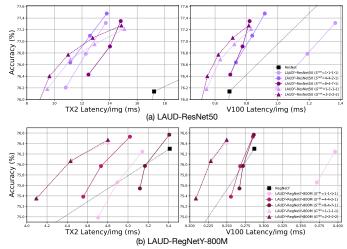


Fig. 9: Comparison of different granularities (*S* and *G*) in LAUD-ResNet-50 (a) and LAUD-RegNetY-800M (b). The latency on TX2 (left) and V100 (right) are presented.

size, eventually reaching a stable plateau when the batch size exceeds 128 on both platforms. This is comprehensible since a larger batch size favors enhanced computation parallelism, resulting in latency becoming more dependent on theoretical computation. The results on the desktop-level GPU, RTX3060 (Fig. 12 in Appendix C.1), show a similar phenomenon. Based on these observations, we report the latency on server-end and desktop-level GPUs with a batch size of 128 henceforth.

4.3 ImageNet classification

4.3.1 Comparison of spatial/channel granularities

We begin by comparing different granularities for spatial and channel-wise dynamic computation. Based on the analysis in Sec. 4.2, the candidates for spatial and channel granularities are $S^{\rm net} \in \{1\text{-}1\text{-}1\text{-}1\text{, 4-4-2-1}, 8\text{-}4\text{-}7\text{-}1\}$ and $G^{\rm net} \in \{1\text{-}1\text{-}1\text{-}1\text{, 2-2-2-2}\}$ respectively. We select ResNet-50 and RegNetY-800M as backbones, and compare various settings on TX2 and V100. The results in Fig. 9 reveal that:

- Regarding spatially dynamic computation, the optimal granularity $S^{\rm net}$ is contingent on both network structures and hardware devices. For instance, $S^{\rm net}$ =8-4-7-1 achieves a preferable performance on V100 for both models, yet incurs substantial inefficiency on TX2. This corresponds to our results in Fig. 6.
- Elevating the channel granularity *G* from 1 to 2 does yield sort of speedup for ResNet-50, but renders comparable performance in the case of RegNetY-800M. We hypothesize that a larger *G* is only beneficial for models with more extensive channel numbers, which also aligns with observations from Fig. 7.

4.3.2 Comparison of dynamic paradigms

Having decided on the optimal granularities, we submit different dynamic paradigms to a more detailed comparison. Additionally, our LAUDNet is compared to various competitive baselines. The findings are illustrated in Fig. 10. **Standard baseline comparison: ResNets.** The compared baselines include various types of dynamic inference approaches: 1) layer skipping (SkipNet [14] and Conv-AIG [15]);

2) channel skipping (BAS [17]); and 3) pixel-level spatial-wise dynamic network (DynConv [20]). For our LAUDNet, we select the best granularity settings for spatial-wise and channel-wise dynamic inference. Layer skipping implemented in our framework is also included. We set training targets (cf. Sec. 3.5) $t \in \{0, 4, \cdots, 0.8\}$ for our dynamic models to evaluate their performance across different sparsity regimes. We apply scheduling optimization (Sec. 3.4) uniformly across all models [15], [20] for a fair comparison.

The results are exhibited in Fig. 10 (a). On the left we plot the relationship between accuracy and FLOPs. It becomes obvious that our LAUD-ResNets, with various granularity settings, considerably outperform competing dynamic networks. Moreover, on ResNet-101, the three paradigms seem fairly comparable, whereas, on ResNet-50, layer skipping falls behind, especially when the training target is small. This is understandable because layer skipping might be overly aggressive for more shallow models.

Interestingly, the scenario alters as we explore real latency (middle on TX2 and right on V100). On the less potent TX2, latency generally exhibits a stronger correlation with theoretical FLOPs, given that it is computation-bounded (that means, the latency is primarily focused around computation) on such IoT devices. However, different dynamic paradigms yield varying acceleration impacts on server-end GPU, V100, as latency could be impacted by the memory access cost. For instance, layer skipping takes precedence over the other two paradigms on the deeper ResNet-101. With the target activation rate t = 0.4, our LAUD¹-ResNet-101 reduces the inference latency of its static counterpart by \sim 53%. On the shallower ResNet-50, channel skipping keeps pace with layer skipping on some low-FLOPs models. Although our proposed course-grained spatially adaptive inference trails behind the other two schemes, it significantly outclasses the previous work using pixel-level dynamic computation [20]. The additional results in Appendix C.2 also demonstrate the preferable efficiency of layer skipping on RTX3060 and RTX3090. Channel skipping outperforms the other two paradigms only on the edge device, Nvidia Nano.

Lightweight baseline comparison: RegNets. We further evaluate our LAUDNet in lightweight CNN architectures, *i.e.* RegNets-Y [24]. Two different sized models are tested: RegNetY-400MF and RegNetY-800MF. Compared baselines include other types of efficient models, *e.g.*, MobileNets-v2 [30], ShuffletNets-v2 [32] and CondenseNets [35].

The results are presented in Fig. 10 (b). We observe that while channel skipping surpasses the other two paradigms substantially in the accuracy-FLOPs trade-off, it is less efficient than layer skipping on most models except RegNet-Y-800M. Remarkably, layer skipping emerges as the most dominant paradigm. We theorize that this is due to the model width (number of channels) of RegNet-Y being limited, and the inference latency still being bounded by memory access. Moreover, layer skipping enables skipping the memory-bounded SE operation [59]. The results on desktop-level and server-end GPUs (Appendix C.2) further showcase the superiority of layer skipping.

Experiments on vision Transformers. Building on the foundation laid out in Sec. 3.2, our LAUDNet seamlessly integrates with vision Transformers using the AdaViT [57] framework. Despite the absence of direct comparisons among

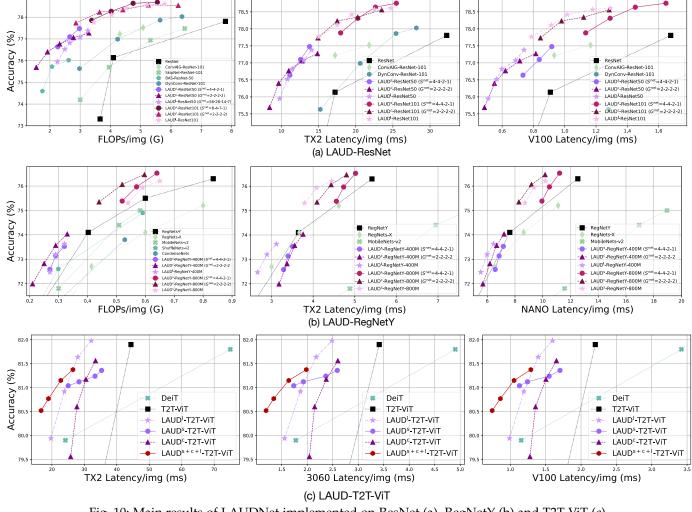


Fig. 10: Main results of LAUDNet implemented on ResNet (a), RegNetY (b) and T2T-ViT (c).



Fig. 11: Visualization results of activation rates $r^{s/c/l}$ and selected patches by LAUD^s-ResNet-101.

the three dynamic paradigms in existing studies, with [57] employing all three simultaneously, it leaves open the question of which paradigm offers the best balance between accuracy and efficiency. We address this by showcasing the accuracy-latency trade-off curves for LAUD-T2T-ViT across various platforms—TX2, RTX3060, and V100 (the performance on RTX3090 is similar to that on V100)—in Fig. 10 (c). The findings highlight several key insights:

 Layer skipping and head (channel) skipping are more advantageous for maintaining high accuracy at high activation rates, though both experience a significant accuracy decline at reduced activation rates.

- When evaluating the balance between practical latency and accuracy, layer skipping consistently outperforms head (channel) skipping on all platforms.
- Despite its lower theoretical upper-bound of accuracy, spatial-wise adaptive computation (token skipping) might excel over the other paradigms at lower activation rates, attributing its practical latency benefits to the straightforward implementation of indexing and selection operations on GPUs, without necessitating specialized operators as in CNNs.
- A synergistic application of all three paradigms further enhances the accuracy-efficiency trade-off, show-

TABLE 2: Object detection results on the COCO dataset.

Detection	Backbone	Backbone Backbone Latency (ms)						
Framework	Dackbone	FLOPs (G)	V100	3090	3060	TX2	Nano	. IIIAI (70)
	ResNet-101 (Baseline)	141.2	33.9	29.8	44.8	586.4	1600.4	39.4
E-ster D CNN	LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.6) LAUD ^s -ResNet-101 (S^{net} =4-4-7-1, t =0.5) LAUD ^s -ResNet-101 (S^{net} =4-4-7-1, t =0.4)	90.7 79.5 67.9	32.4 30.4 27.4	36.8 29.4 26.2	40.4 38.2 34.5	402.2 390.4 340.0	1082.4 1050.7 911.4	40.3 40.0 39.5
Faster R-CNN	LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.8) LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.7) LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.6)	112.37 96.42 80.73	30.6 27.9 23.9	30.0 27.3 24.6	42.0 37.8 33.9	471.6 400.4 335.7	1264.3 1065.4 884.0	40.2 40.0 39.7
	LAUD ¹ -ResNet-101 (<i>t</i> =0.5) LAUD ¹ -ResNet-101 (<i>t</i> =0.4)	97.97 86.71	24.2 19.8	22.1 18.2	32.2 26.5	409.2 331.2	1114.1 899.9	40.2 39.5
	ResNet-101 (Baseline)	141.2	33.9	29.8	44.8	586.4	1600.4	38.5
RetinaNet	LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.5) LAUD ^s -ResNet-101 (S^{net} =4-4-7-1, t =0.4)	77.8 66.4	29.0 28.1	32.7 26.0	36.7 35.2	350.1 335.0	937.1 897.1	39.3 38.9
	LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.6) LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.5)	79.6 65.5	23.7 20.9	24.4 22.1	33.7 30.4	331.2 278.7	871.4 724.6	39.3 38.5
	LAUD ¹ -ResNet-101 (t =0.5) LAUD ¹ -ResNet-101 (t =0.3)	95.1 74.4	23.6 18.7	21.5 17.3	31.4 25.0	397.7 311.4	1082.5 846.3	39.4 38.6
Deformable-DETR DINO-DETR Rank-DETR Stable-DINO	ResNet-50 (Baseline)	73.3	18.4	16.2	25.0	313.6	851.4	46.9 49.0 50.2 50.4
	ResNet-50 (Baseline)	73.3	18.4	16.2	25.0	313.6	851.4	51.1
DDQ-DETR	LAUD ^s -ResNet-50 (S^{net} =8-4-7-1, t =0.6) LAUD ^s -ResNet-50 (S^{net} =8-4-7-1, t =0.5)	61.9 56.8	21.3 19.9	22.7 20.9	27.6 25.8	287.9 264.5	776.4 711.6	51.3 51.1
	LAUD ^c -ResNet-50 (C^{net} =2-2-2-2, t =0.7) LAUD ^c -ResNet-50 (C^{net} =2-2-2-2, t =0.6)	50.3 42.5	15.0 13.3	15.2 13.8	21.7 19.6	222.0 186.6	581.1 488.1	50.7 50.5
	LAUD ¹ -ResNet-50 (t =0.5) LAUD ¹ -ResNet-50 (t =0.3)	62.2 54.4	15.9 13.5	14.5 12.6	21.5 18.0	265.8 226.1	720.8 614.7	51.1 50.9
	ResNet-101 (Baseline)	141.2	33.9	29.8	44.8	586.4	1600.4	51.8
	LAUDs-ResNet-101 (S^{net} =4-4-2-1, t =0.5) LAUDs-ResNet-101 (S^{net} =4-4-2-1, t =0.4)	93.3 85.7	33.7 31.5	38.3 35.7	41.8 39.2	417.9 385.5	1125.7 1036.7	52.4 51.9
	LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.8) LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.6) LAUD ^c -ResNet-101 (C^{net} =1-1-1-1, t =0.5)	111.8 80.8 62.4	30.8 24.1 20.5	30.1 24.7 21.7	42.1 34.1 29.9	474.1 338.5 270.2	1271.8 891.9 701.0	52.3 52.0 51.8
	LAUD ¹ -ResNet-101 (t =0.4) LAUD ¹ -ResNet-101 (t =0.3)	104.5 101.9	26.0 25.4	23.6 23.1	34.4 33.6	439.8 429.0	1197.8 1168.3	52.2 51.9

ing the complementary strengths of each approach.

4.4 Visualization and interpretability

We present visualization results of LAUDNet to delve into its interpretability from the perspectives of networks' structural redundancy and images' spatial redundancy.

Activation rate. Fig. 11 (a) illustrates the average activation rates $r^{\rm s/c/l}$ of each block in LAUD^{s/c/l}-ResNet-101 (t=0.5) on the ImageNet validation set. The results uncover that

- The activation rate patterns for spatially dynamic convolution and layer skipping are similar. The activation rates $r^{\rm s}$ and $r^{\rm l}$ seem more binarized (close to 0 or 1) in stages 1, 2, and 4. The dynamic region/layer selection predominantly occurs in stage 3;
- These two paradigms tend to maintain the entire feature map ($r^{s/l}$ =1.0) at the first block of stages 2, 3, and 4, where the convolutional stride is 1. This aligns with the settings in [15], [54], where the training targets for these blocks are manually set to

- 1. Notably, we train our LAUDNet to meet an overall computational target, rather than confining the targets for different blocks as done in [15], [54].
- Channel skipping results in activation rates that are more centered around 0.5 throughout the network.

Dynamic patch selection. We visualize the spatial masks generated by our third block of a LAUD^s-ResNet-101 ($S^{\rm net}$ =4-4-2-1) in Fig. 11 (b). The highlighted areas denote the locations of 1 elements in a mask, while computations in the dimmed regions are skipped by our dynamic model. It becomes evident that the masker is adept at pinpointing the most task-related areas, even minutiae such as the tiny aircraft at the corner, thereby trimming unnecessary computations in background zones. Such findings imply that, a granularity of S=4 is aptly flexible for identifying crucial regions, paving the way for a harmonious balance between accuracy and efficiency. Intriguingly, the masker is able to pick out objects which are *not labeled* for that particular sample - for instance, the flower next to the hummingbird or the person clutching the camera. This signals that our spatially dynamic networks

TABLE 3: Instance Segmentation results on the COCO dataset.

Segmentation	Backbone	Backbone	Backbone Latency (ms)				AP^{mask}	$\mathrm{AP^{box}}$	
Framework	Buchbone	FLOPs (G)	V100	3090	3060	TX2	Nano	(%)	(%)
	ResNet-101 (Baseline)	141.2	33.9	29.8	44.8	586.4	1600.4	36.1	40.0
Mask R-CNN	LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.5) LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.4)	80.5 69.2	29.7 26.4	33.5 29.6	37.5 33.7	361.9 314.3	969.9 838.8	37.0 36.1	41.0 40.0
	$ \begin{array}{l} {\rm LAUD^c\text{-}ResNet\text{-}101}~(C^{\rm net}\text{=}2\text{-}2\text{-}2\text{-}2,}~t\text{=}0.8) \\ {\rm LAUD^c\text{-}ResNet\text{-}101}~(C^{\rm net}\text{=}2\text{-}2\text{-}2\text{-}2,}~t\text{=}0.7) \\ {\rm LAUD^c\text{-}ResNet\text{-}101}~(C^{\rm net}\text{=}2\text{-}2\text{-}2\text{-}2,}~t\text{=}0.6) \end{array}$	112.7 95.9 80.8	30.7 27.1 23.9	30.0 27.2 24.6	42.1 37.7 33.9	473.1 397.8 335.7	1269.3 1057.5 883.9	36.9 36.6 36.4	40.9 40.6 40.3
	LAUD ¹ -ResNet-101 (t =0.5) LAUD ¹ -ResNet-101 (t =0.4) LAUD ¹ -ResNet-101 (t =0.3)	101.7 91.8 82.2	25.1 22.8 20.6	22.9 20.9 18.9	33.3 30.4 27.5	424.4 384.3 345.3	1155.7 1045.4 938.5	36.7 36.4 36.2	40.7 40.4 40.0
	ResNet-101 (Baseline)	141.2	33.9	29.8	44.8	586.4	1600.4	44.0	46.7
Mask2Former	LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.5) LAUD ^s -ResNet-101 (S^{net} =4-4-2-1, t =0.4)	109.7 98.8	37.2 34.0	43.8 39.9	47.1 43.2	481.8 436.0	1301.9 1176.1	44.0 43.8	47.1 46.7
	LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.8) LAUD ^c -ResNet-101 (C^{net} =2-2-2-2, t =0.7)	111.9 94.9	30.5 26.8	29.9 27.0	41.8 37.4	469.0 393.1	1257.6 1044.5	44.0 43.9	46.9 46.8
	LAUD ¹ -ResNet-101 (<i>t</i> =0.5) LAUD ¹ -ResNet-101 (<i>t</i> =0.4)	112.8 109.9	27.7 27.0	25.1 24.5	36.6 35.7	469.4 457.5	1279.2 1246.6	44.0 43.9	47.0 46.8

inherently discern regions imbued with semantic significance, and their prowess isn't shackled by mere classification labels. Such a trait is invaluable for a slew of downstream tasks, like object detection and instance segmentation (Sec. 4.5), tasks which necessitate the identification of various classes and objects within an image. For a broader range of visualization results, readers can refer to Appendix C.3.

4.5 Dense prediction tasks

Our LAUDNet is further put to test on downstream tasks, i.e. COCO [61] object detection (as seen in Table 2) and instance segmentation (presented in Table 3). For object detection, the mean average precision (mAP) stands as the barometer for network efficacy. For instance segmentation, the AP^{mask} dives deeper to gauge the nuance of dense prediction. The average backbone FLOPs, and the average backbone latency on the validation set are used to measure the network efficiency. Due to LAUDNet's versatile nature, we can seamlessly replace the backbones in various detection and segmentation frameworks with our pre-trained models on ImageNet, then fine-tune them on the COCO dataset under the standard protocol for 12 epochs—except for models based on Mask2Former [62], which are trained for 50 epochs in line with the baseline configurations (detailed settings are elaborated in Appendix B.3). In the domain of object detection, our experimentation covers three frameworks: the two-stage Faster R-CNN [63] with Feature Pyramid Network [64], the one-stage RetinaNet [65], and a DETR [66]-based model, namely Dense Distinct Query (DDQ)-DETR [67]. We compare our results against a range of recent advancements, such as Deformable DETR [68], DINO-DETR [69], Rank-DETR [70], and Stable-DINO [71]. For instance segmentation, we utilize the well-established Mask R-CNN [72] and the query-based Mask2Former [62]. The results are presented in Tab. 2 (for object detection) and Tab. 3 (for instance segmentation), unequivocally demonstrating that LAUD-Net consistently boosts both mAP and efficiency across classic and state-of-the-art (SOTA) frameworks. Notably, while channel and layer skipping generally surpass spatialwise dynamic computation in efficiency, the ideal dynamic

paradigm may vary depending on the specific detection framework, backbone architecture, and hardware platforms.

5 CONCLUSION

In this paper, we propose to build latency-aware unified dynamic networks (LAUDNet) under the guidance of a latency prediction model. By collectively considering the algorithm, scheduling strategy, and hardware properties, we can accurately estimate the practical latency of different dynamic operators on any computing platforms. Based on an empirical analysis of the correlation between latency and the granularity of spatial-wise and channel-wise adaptive inference, the algorithm and scheduling strategies are optimized to attain realistic speedup on a range of multi-core processors, such as Tesla V100 and Jetson TX2. Our experiments on image classification, object detection, and instance segmentation tasks affirm that the proposed method markedly boosts the practical efficiency of deep CNNs and surpasses numerous competing approaches. We believe our research brings useful insights into the design of dynamic networks. Future works include explorations on more types of model architectures (e.g. Transformers, large language models) and tasks (e.g. low-level vision tasks and vision-language tasks).

ACKNOWLEDGMENTS

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REFERENCES

- Jia Deng, Wei Dong, Richard Socher, Li-Jia Li, Kai Li, and Li Fei-Fei. Imagenet: A large-scale hierarchical image database. In CVPR, 2009.
- [2] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. Deep residual learning for image recognition. In *CVPR*, 2016.

- [3] Gao Huang, Zhuang Liu, Geoff Pleiss, Laurens Van Der Maaten, and Kilian Weinberger. Densely connected convolutional networks. TPAMI. 2019.
- Alexey Dosovitskiy, Lucas Beyer, Alexander Kolesnikov, Dirk Weissenborn, Xiaohua Zhai, Thomas Unterthiner, Mostafa Dehghani, Matthias Minderer, Georg Heigold, Sylvain Gelly, Jakob Uszkoreit, and Neil Houlsby. An image is worth 16x16 words: Transformers for image recognition at scale. In ICLR, 2021.
- Alexander Kirillov, Eric Mintun, Nikhila Ravi, Hanzi Mao, Chloe Rolland, Laura Gustafson, Tete Xiao, Spencer Whitehead, Alexander C Berg, Wan-Yen Lo, et al. Segment anything. arXiv preprint arXiv:2304.02643, 2023.
- Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N Gomez, Łukasz Kaiser, and Illia Polosukhin. Attention is all you need. In NeurIPS, 2017.
- Jacob Devlin, Ming-Wei Chang, Kenton Lee, and Kristina Toutanova. BERT: Pre-training of Deep Bidirectional Transformers for Language Understanding. In ACL, 2019.
- Alec Radford, Karthik Narasimhan, Tim Salimans, Ilya Sutskever, et al. Improving language understanding by generative pretraining. 2018.
- Alec Radford, Jeffrey Wu, Rewon Child, David Luan, Dario Amodei, and Ilya Sutskever. Language models are unsupervised multitask learners. OpenAI blog, 2019.
- [10] OpenAI. Gpt-4 technical report, 2023.
- [11] Yizeng Han, Gao Huang, Shiji Song, Le Yang, Honghui Wang, and Yulin Wang. Dynamic neural networks: A survey. *TPAMI*, 2021.
- Gao Huang, Danlu Chen, Tianhong Li, Felix Wu, Laurens van der Maaten, and Kilian Weinberger. Multi-scale dense networks for resource efficient image classification. In ICLR, 2018.
- [13] Yizeng Han, Yifan Pu, Zihang Lai, Chaofei Wang, Shiji Song, Junfen Cao, Wenhui Huang, Chao Deng, and Gao Huang. Learning to weight samples for dynamic early-exiting networks. In ECCV, 2022.
- [14] Xin Wang, Fisher Yu, Zi-Yi Dou, Trevor Darrell, and Joseph E Gonzalez. Skipnet: Learning dynamic routing in convolutional networks. In ECCV, 2018.
- [15] Andreas Veit and Serge Belongie. Convolutional networks with adaptive inference graphs. In ECCV, 2018.
- [16] Ji Lin, Yongming Rao, Jiwen Lu, and Jie Zhou. Runtime neural pruning. In NeurIPS, 2017.
- [17] Babak Ehteshami Bejnordi, Tijmen Blankevoort, and Max Welling. Batch-shaping for learning conditional channel gated networks. In ICLR. 2020.
- [18] Michael Figurnov, Maxwell D Collins, Yukun Zhu, Li Zhang, Jonathan Huang, Dmitry Vetrov, and Ruslan Salakhutdinov. Spatially adaptive computation time for residual networks. In CVPR,
- [19] Xuanyi Dong, Junshi Huang, Yi Yang, and Shuicheng Yan. More is less: A more complicated network with less inference complexity. In CVPR, 2017.
- [20] Thomas Verelst and Tinne Tuytelaars. Dynamic convolutions: Exploiting Spatial Sparsity for Faster Inference. In CVPR, 2020.
- [21] Zhenda Xie, Zheng Zhang, Xizhou Zhu, Gao Huang, and Stephen Lin. Spatially adaptive inference with stochastic feature sampling and interpolation. In ECCV, 2020.
- [22] Yulin Wang, Kangchen Lv, Rui Huang, Shiji Song, Le Yang, and Gao Huang. Glance and focus: a dynamic approach to reducing spatial redundancy in image classification. In NeurIPS, 2020.
- [23] Yizeng Han, Gao Huang, Shiji Song, Le Yang, Yitian Zhang, and Haojun Jiang. Spatially adaptive feature refinement for efficient inference. *TIP*, 2021.
- [24] Ilija Radosavovic, Raj Prateek Kosaraju, Ross Girshick, Kaiming He, and Piotr Dollár. Designing network design spaces. In CVPR,
- [25] Hugo Touvron, Matthieu Cord, Matthijs Douze, Francisco Massa, Alexandre Sablayrolles, and Hervé Jégou. Training data-efficient image transformers & distillation through attention. In ICML, 2021.
- [26] Li Yuan, Yunpeng Chen, Tao Wang, Weihao Yu, Yujun Shi, Zi-Hang Jiang, Francis EH Tay, Jiashi Feng, and Shuicheng Yan. Tokens-totoken vit: Training vision transformers from scratch on imagenet. In ICCV, 2021.
- [27] Yizeng Han, Zhihang Yuan, Yifan Pu, Chenhao Xue, Shiji Song, Guangyu Sun, and Gao Huang. Latency-aware spatial-wise dynamic networks. In NeurIPS, 2022.
- [28] Nvidia. Cutlass. https://www.github.com/NVIDIA/cutlass.[29] Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto,

- and Hartwig Adam. Mobilenets: Efficient convolutional neural networks for mobile vision applications. arXiv preprint arXiv:1704.04861, 2017.
- [30] Mark Sandler, Andrew Howard, Menglong Zhu, Andrey Zhmoginov, and Liang-Chieh Chen. Mobilenetv2: Inverted residuals and linear bottlenecks. In CVPR, 2018.
- Xiangyu Zhang, Xinyu Zhou, Mengxiao Lin, and Jian Sun. Shufflenet: An extremely efficient convolutional neural network for mobile devices. In CVPR, 2018.
- Ningning Ma, Xiangyu Zhang, Hai-Tao Zheng, and Jian Sun. Shufflenet v2: Practical guidelines for efficient cnn architecture design. In ECCV, 2018.
- Song Han, Huizi Mao, and William J Dally. Deep compression: Compressing deep neural networks with pruning, trained quantization and huffman coding. 2016.
- [34] Yang He, Ping Liu, Ziwei Wang, Zhilan Hu, and Yi Yang. Filter pruning via geometric median for deep convolutional neural networks acceleration. In CVPR, 2019.
- Gao Huang, Shichen Liu, Laurens Van der Maaten, and Kilian Q Weinberger. Condensenet: An efficient densenet using learned group convolutions. In CVPR, 2018.
- Le Yang, Haojun Jiang, Ruojin Cai, Yulin Wang, Shiji Song, Gao Huang, and Qi Tian. Condensenet v2: Sparse feature reactivation for deep networks. In CVPR, 2021.
- [37] Itay Hubara, Matthieu Courbariaux, Daniel Soudry, Ran El-Yaniv, and Yoshua Bengio. Binarized neural networks. In NeurIPS, 2016.
- Jungwook Choi, Zhuo Wang, Swagath Venkataramani, Pierce I-Jen Chuang, Vijayalakshmi Srinivasan, and Kailash Gopalakrishnan. Pact: Parameterized clipping activation for quantized neural networks. arXiv preprint arXiv:1805.06085, 2018.
- Sangil Jung, Changyong Son, Seohyung Lee, Jinwoo Son, Jae-Joon Han, Youngjun Kwak, Sung Ju Hwang, and Changkyu Choi. Learning to quantize deep networks by optimizing quantization intervals with task loss. In CVPR, 2019.
- Zhihang Yuan, Chenhao Xue, Yiqi Chen, Qiang Wu, and Guangyu Sun. Ptq4vit: Post-training quantization for vision transformers with twin uniform quantization. In ECCV, 2022.
- [41] Geoffrey Hinton, Oriol Vinyals, and Jeff Dean. Distilling the knowledge in a neural network. In NeurIPS Workshop, 2014.
- [42] Chaofei Wang, Qisen Yang, Rui Huang, Shiji Song, and Gao Huang. Efficient knowledge distillation from model checkpoints. In NeurIPS, 2022
- Alex Graves. Adaptive computation time for recurrent neural networks. arXiv preprint arXiv:1603.08983, 2016.
- Le Yang, Yizeng Han, Xi Chen, Shiji Song, Jifeng Dai, and Gao Huang. Resolution adaptive networks for efficient inference. In CVPR, 2020.
- [45] Xitong Gao, Yiren Zhao, Łukasz Dudziak, Robert Mullins, and Cheng zhong Xu. Dynamic channel pruning: Feature boosting and suppression. In ICLR, 2019.
- [46] Han Cai, Ligeng Zhu, and Song Han. Proxylessnas: Direct neural architecture search on target task and hardware. In ICLR, 2019.
- Mingxing Tan, Bo Chen, Ruoming Pang, Vijay Vasudevan, Mark Sandler, Andrew Howard, and Quoc V Le. Mnasnet: Platformaware neural architecture search for mobile. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 2820-2828, 2019.
- [48] Bichen Wu, Xiaoliang Dai, Peizhao Zhang, Yanghan Wang, Fei Sun, Yiming Wu, Yuandong Tian, Peter Vajda, Yangqing Jia, and Kurt Keutzer. Fbnet: Hardware-aware efficient convnet design via differentiable neural architecture search. In CVPR, 2019.
- [49] Han Cai, Chuang Gan, Tianzhe Wang, Zhekai Zhang, and Song Han. Once-for-all: Train one network and specialize it for efficient deployment. In ICLR, 2019.
- [50] Barret Zoph and Quoc V Le. Neural architecture search with reinforcement learning. In ICLR, 2017.
- [51] Hanxiao Liu, Karen Simonyan, and Yiming Yang. DARTS: Differentiable Architecture Search. In ICLR, 2018.
- [52] Mengye Ren, Andrei Pokrovsky, Bin Yang, and Raquel Urtasun. SBNet: Sparse Blocks Network for Fast Inference. CVPR, 2018.
- Zuxuan Wu, Tushar Nagarajan, Abhishek Kumar, Steven Rennie, Larry S Davis, Kristen Grauman, and Rogerio Feris. Blockdrop: Dynamic inference paths in residual networks. In CVPR, 2018.
- Charles Herrmann, Richard Strong Bowen, and Ramin Zabih. Channel selection using gumbel softmax. In ECCV, 2020.
- Eric Jang, Shixiang Gu, and Ben Poole. Categorical reparameterization with gumbel-softmax. In ICLR, 2017.

- [56] Chris J Maddison, Andriy Mnih, and Yee Whye Teh. The concrete distribution: A continuous relaxation of discrete random variables. In ICLR, 2017.
- [57] Lingchen Meng, Hengduo Li, Bor-Chun Chen, Shiyi Lan, Zuxuan Wu, Yu-Gang Jiang, and Ser-Nam Lim. Adavit: Adaptive vision transformers for efficient image recognition. In CVPR, 2022.
- [58] John L Hennessy and David A Patterson. *Computer architecture: a quantitative approach.* Elsevier, 2011.
- [59] Jie Hu, Li Shen, and Gang Sun. Squeeze-and-excitation networks. In CVPR, 2018.
- [60] Steven Colleman, Thomas Verelst, Linyan Mei, Tinne Tuytelaars, and Marian Verhelst. Processor architecture optimization for spatially dynamic neural networks. In VLSI-SoC, 2021.
- [61] Tsung-Yi Lin, Michael Maire, Serge Belongie, James Hays, Pietro Perona, Deva Ramanan, Piotr Dollár, and C Lawrence Zitnick. Microsoft coco: Common objects in context. In ECCV, 2014.
- [62] Bowen Cheng, Ishan Misra, Alexander G Schwing, Alexander Kirillov, and Rohit Girdhar. Masked-attention mask transformer for universal image segmentation. In CVPR, 2022.
- [63] Shaoqing Ren, Kaiming He, Ross Girshick, and Jian Sun. Faster r-cnn: Towards real-time object detection with region proposal networks. In *NeurIPS*, 2015.
- [64] Tsung-Yi Lin, Piotr Dollár, Ross Girshick, Kaiming He, Bharath Hariharan, and Serge Belongie. Feature pyramid networks for object detection. In CVPR, 2017.
- [65] Tsung-Yi Lin, Priya Goyal, Ross Girshick, Kaiming He, and Piotr Dollár. Focal loss for dense object detection. In ICCV, 2017.
- [66] Nicolas Carion, Francisco Massa, Gabriel Synnaeve, Nicolas Usunier, Alexander Kirillov, and Sergey Zagoruyko. End-to-end object detection with transformers. In ECCV, 2020.
- [67] Shilong Zhang, Xinjiang Wang, Jiaqi Wang, Jiangmiao Pang, Chengqi Lyu, Wenwei Zhang, Ping Luo, and Kai Chen. Dense distinct query for end-to-end object detection. In CVPR, 2023.
- [68] Xizhou Zhu, Weijie Su, Lewei Lu, Bin Li, Xiaogang Wang, and Jifeng Dai. Deformable detr: Deformable transformers for end-toend object detection. In *ICLR*, 2020.
- [69] Hao Zhang, Feng Li, Shilong Liu, Lei Zhang, Hang Su, Jun Zhu, Lionel Ni, and Heung-Yeung Shum. Dino: Detr with improved denoising anchor boxes for end-to-end object detection. In *ICLR*, 2022.
- [70] Yifan Pu, Weicong Liang, Yiduo Hao, Yuhui Yuan, Yukang Yang, Chao Zhang, Han Hu, and Gao Huang. Rank-detr for high quality object detection. In *NeurIPS*, 2023.
- [71] Shilong Liu, Tianhe Ren, Jiayu Chen, Zhaoyang Zeng, Hao Zhang, Feng Li, Hongyang Li, Jun Huang, Hang Su, Jun Zhu, et al. Detection transformer with stable matching. *arXiv preprint arXiv:*2304.04742, 2023.
- [72] Kaiming He, Georgia Gkioxari, Piotr Dollár, and Ross Girshick. Mask r-cnn. In ICCV, pages 2961–2969, 2017.

APPENDIX A LATENCY PREDICTION MODEL.

As the dynamic operators in our method have not been supported by current deep learning libraries, we propose a latency prediction model to efficiently estimate the real latency of these operators on hardware device. The inputs of the latency prediction model include: 1) the structural configuration and dynamic paradigm of a convolution block, 2) its activation rate r which decides the computation amount, 3) the spatial (channel) granularity $S\left(G\right)$, and 4) the hardware properties mentioned in Table 4. The latency of a dynamic block is predicted as follows.

Input/output shape definition. The first step of predicting the latency of an operation is to calculate the shape of input and output. Taking the gather-conv2 operation in LAUD's-ResNets as an example, the input of this operation is the activation with the shape of $C_{\rm in} \times H \times W$, where $C_{\rm in}$ is the number of input channels, and H and W are the resolution of the feature map. The shape of the output tensor is $P \times C_{\rm out} \times S \times S$, where P is the number of output patches, $C_{\rm out}$ is the number of output channels and S is the spatial granularity. Note that P is obtained based on the output of our maskers.

Operation-to-hardware mapping. Next, we map the operations to hardware. As illustrated in Fig. 4, we model a hardware

TABLE 4: Hardware properties.

Name	#PE	#FP32	Frequency	Bandwidth
Nvidia Tesla V100	80	64	1500MHz	700G
Nvidia RTX3090	82	128	1695MHz	936G
Nvidia RTX3060	28	128	1777MHz	360G
Nvidia Jetson TX2	2	128	1300MHz	59.7G
Nvidia Nano	1	128	921MHz	25.6G

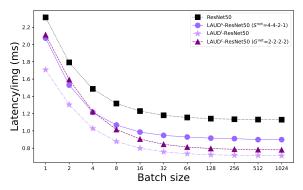


Fig. 12: Relationship between the inference latency per image and batch size of LAUD-ResNet-50 on RTX3060.

device as multiple processing engines (PEs). We assign the computation of each element in the output feature map to a PE. Specifically, we consecutively split the output feature map into multiple *tiles*. The shape of each tile is $T_P \times T_C \times T_{S1} \times T_{S2}$. These split tiles are assigned to multiple PEs. The computation of the elements in each tile is executed in a PE. We can configure different shapes of tiles. In order to determine the optimal shape of the tile, we make a search space of different tile shapes. The tile shape has 4 dimensions. The candidates of each dimension are power-of-2 and do not exceed the corresponding dimension of the feature map.

Latency estimation. Then, we evaluate the latency of each tile shape in the search space and select the optimal tile shape with the lowest latency. The latency includes the *data movement* latency and the *computation* latency:

$$\ell = \ell_{\rm data} + \ell_{\rm computation}.$$
 (4)

1) Data movement latency $\ell_{\rm data}$. The estimation of the latency for data movement requires us to model the memory system of a hardware device. We model the memory system of hardware as a three-level architecture [58]: off-chip memory, on-chip global memory, and local memory in PE. The input data and weight data are first transferred from the off-chip memory to the on-chip global memory. We assume the hardware can make full use of the off-chip memory bandwidth to simplify the latency prediction model.

After that, the data used to compute the output tiles is transferred from on-chip global memory to the local memory of each PE. The latency of data movement to local memory is estimated by its bandwidth and efficiency. We assume each PE only moves the corresponding input feature maps and weights once to compute a output tile so as to simplify the prediction model. The input data movement latency $\ell_{\rm in}$ is calculated by adding the time from off-chip memory to on-chip global memory and the time from on-chip global memory to local-memory together: $\ell_{\rm in} = \ell_{\rm off2on} + \ell_{\rm global2local}$. Contrary to the input data, the output data $\ell_{\rm out}$ are moved from local memory to on-chip global memory and then to off-chip memory: $\ell_{\rm out} = \ell_{\rm local2global} + \ell_{\rm on2off}$. We calculate the total data movement latency by adding the input and output data movement latency together:

$$\ell_{\rm data} = \ell_{\rm in} + \ell_{\rm out}. \tag{5}$$

TABLE 5: Ablation study of channel masker.

Stage	1		2		3		4	
	Latency (ms)	Ratio Lat	ency (ms)	Ratio	Latency (ms)	Ratio	Latency (ms)	Ratio
1-layer	0.21	14.9%	0.29	16.5%	0.58	21.7%	0.72	33.6%
2-layer (ours)	0.22	15.8%	0.27	15.6%	0.31	12.8%	0.19	11.6%

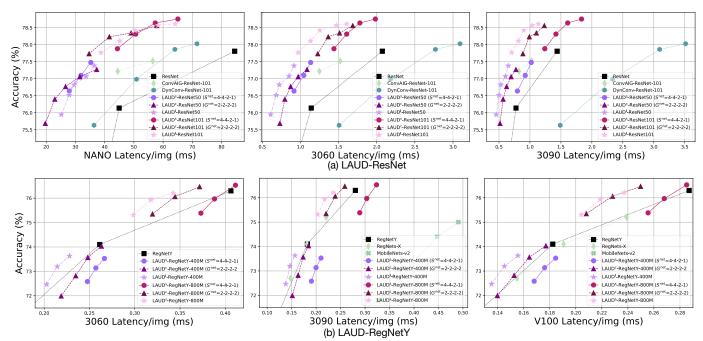


Fig. 13: Additional results on more hardware devices. (a) for ResNets and (b) for RegNets.

The latency of data movement is affected by the granularity S or G: when the granularity is small, the same input data has a higher probability of being sent to multiple PEs to compute different output patches, which significantly increases the number of on-chip memory movement. And due to the small amount of data transmitted each time and the data is randomly distributed, the efficiency of data movement will be low. This accounts for our experiment results in the paper that a larger S will effectively improve the practical efficiency.

2) Computation latency $\ell_{\rm computation}$. The computation latency of each tile is estimated using the PE's maximum throughput of FP32 computation and the FLOPs of computing an output tile. The total computation latency can be obtained according to the number of tiles and the number of PEs.

To summarize, our latency prediction model can predict the real latency of dynamic operators by considering both the *data movement* cost and the *computation* cost. Guided by the latency prediction model, we propose our LAUDNet with coarsegrained spatially adaptive inference (S>1) and G>1. It is validated in our paper that LAUDNet achieve better efficiency than previous approaches [20], [21] (S=1), as it effectively reduces the data movement latency, which is rarely considered by other researchers.

APPENDIX B DETAILED EXPERIMENTAL SETTINGS

In this section, we present the detailed experiment settings which are not provided in the main paper due to the page limit.

B.1 Latency prediction

Hardware properties considered by our latency prediction model include the number of processing engines (#PE), the floating-point computation in a processing engine (#FP32), the frequency and the bandwidth. We test four types of hardware devices, and their properties are listed in Table 4.

It could be found that the server-end GPUs V100 and RTX3090 are more powerful hardware devices, especially with the largest number of processing engines (#PE). Therefore, spatially adaptive inference and dynamic channel skipping could easily fall into a *memory-bounded* operation on these GPUs. Our experiment results in Fig. 6 and Fig. 9 in the paper can reflect this phenomenon: the more flexibility the computation is, the harder to improve the practical efficiency.

Operator fusion.

1) Fusing the masker and the first convolution. We mentioned in Sec. 3.4 of the paper that the masker operation is fused with the first 1×1 convolution in a block to reduce the cost on memory access. This is feasible because the two operators share the same input feature, and their convolution kernel sizes are both 1×1 .

Note that during the inference stage, we only need to perform $\arg\max$ along the channel dimension of a mask $\mathbf{M} \in \mathbb{R}^{2 \times H \times W}$ to obtain the positions of the gathered pixels. Therefore, we can reduce the output channel number of our maskers from 2 to 1 since the convolution is a linear operation:

$$[\mathbf{x} * \mathbf{W}]_{:,:,0} > [\mathbf{x} * \mathbf{W}]_{:,:,1} \Longleftrightarrow \mathbf{x} * (\mathbf{W}_{:,:,0} - \mathbf{W}_{:,:,1}) > 0.$$
 (6)

Afterwards, we fuse the masker with the first convolution by performing once convolution whose output channel number is C+1, where C is the original output width of the first convolution. The output of this step is split into a feature map (for further computation) and a mask (for obtaining the index for gathering). Such operator fusion avoids the repeated reading the input feature, and helps reduce the inference latency (Tab. 1).

2) Fusing the gather operation and the dynamic convolution. To facilitate the scheduling on hardware devices with multiple PEs, the masker generates the indices of activated patches instead of sparse mask at inference time. In this way, it is easy to evenly distribute the computation of output patches to different PEs, thus avoiding unbalanced computation of PEs. Each element in

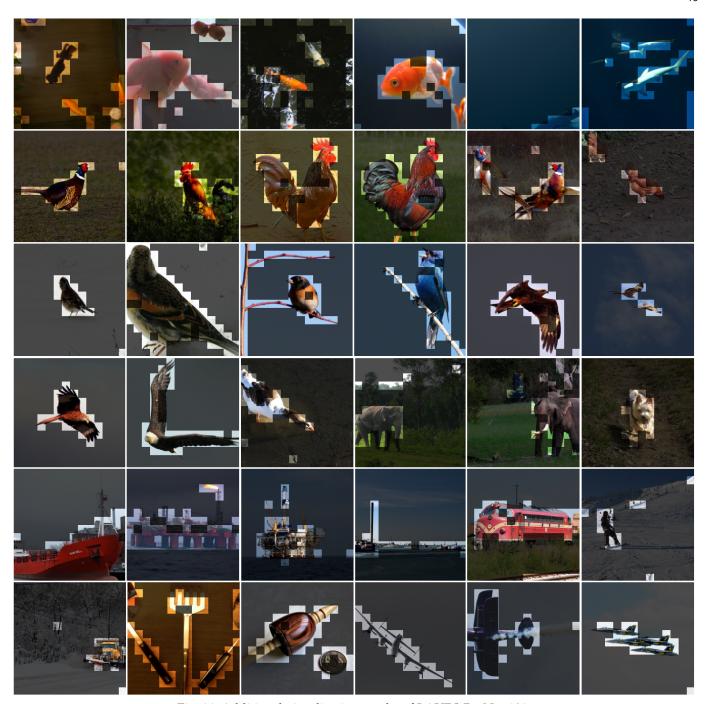


Fig. 14: Additional visualization results of LAUDs-ResNet-101.

the indices represents the index of an activated patch. PE fetches the input data from the corresponding positions on the feature map according to the index. The output patches could be densely stored in memory. Such operator fusion benefits the contiguous memory access and parallel computation on multiple PEs.

3) Fusing the scatter operation and the add operation. Similar to the previous operation, each PE fetches a tile of data from the residual feature map according to the index, adds them with the corresponding feature map from previous dynamic convolution, and then stores the results to the corresponding position on the residual feature map according to the index. This optimization can significantly reduce the costs on memory access.

Speed test. We test the latency on real hardware devices to evaluate the accuracy of our latency prediction model. On GPUs, we use Nvidia Cutlass (https://github.com/NVIDIA/cutlass) and CUDA (version 11.6) for code generation and compilation

respectively. The results in Fig. 5 of the paper validate that the predictions obtained from our latency predictor effectively align with the real-test values.

B.2 ImageNet classification

We use pre-trained CNN models in the official torchvision website to initialize our backbone parameters, and finetune the overall models for 100 epochs. The initial learning rate is set as $0.01 \times \text{batch size}/128$, and decays with a cosine shape. The training batch size is determined on the model size and the GPU memory. For example, we train our LAUD-ResNet-101 on 8 RTX 3090 GPUs with the batch size of 512, and the batch size for LAUD-ResNet-50 is doubled. We use the same weight decay and the standard data augmentation as in the RegNet paper [24]. For our own hyper-parameter τ in Eq. (1) of the paper, this Gumbel temperature τ exponentially decreases from 5 to 0.1 in

the training procedure. For the training hyper-parameter in Eq. (2), we simply fix $\alpha=10,\beta=0.5$ and T=4.0 for all dynamic models. We conduct a very simple grid search with a RegNet for $\beta\in\{0.3,0.5\}$ and $T\in\{1.0,4.0\}$ to determine their values.

B.3 COCO object detection & instance segmentation

We use the standard setting suggested in [62], [64], [65], [67], [72], except that we decrease the learning rate for our pre-trained backbone network. We simply set a learning rate multiplier 0.5 for Faster R-CNN [63], 0.2 for RetinaNet [65] and 0.5 for Mask R-CNN [72]. For DDQ-DETR and Mask2Former, we follow the standard setting and set the learning rate multiplier to 0.1. As for the additional loss items, the hyper-parameters are kept the same as training our classification models, except that the temperature is fixed as 0.1 in the 12 training epochs. The input images are resized to a short side of 800 with a long side not exceeding 1333.

APPENDIX C MORE EXPERIMENTAL RESULTS

In this section, we report more experimental results which are not presented in the main paper.

C.1 Latency prediction

Design of channel masker. We mentioned in Sec. 3.2 that our channel maskers are designed as a 2-layer MLP with reduced hidden units. This design is determined under the guidance of our latency predictor. Specifically, we compare the latency of two choices with a a LAUD^c-ResNet-101 on TX2: 1 linear layer and our 2-layer MLP. The latency numbers of the channel maskers in 4 stages and their ratios to those of ResNet blocks are reported in Table 5. The results reveal that in late stages where channel numbers are large, our 2-layer MLP with reduced hidden units significantly reduces the latency.

Batch size. The relationship between inference latency and batch size of LAUD-ResNet-50 on the desktop-level GPU, RTX3060, is presented in Fig. 12. The phenomenon is similar to the servenend GPUs we present in the main paper (Figure 8).

C.2 ImageNet classification

Results on more hardware devices. In Fig. 10 of the paper, we report the ImageNet classification results of LAUD-ResNet on V100 and TX2, and those of LAUD-RegNet-Y on TX2 and Nano. Here we present the results on other hardware platforms. From the results in Fig. 13, we can find that the optimal dynamic-inference paradigms can depend on the backbone and hardware devices. For example, channel skip demonstrate its advantages on Nano for LAUD-ResNet-50 and ResNet-101, while layer skipping significantly outperform the other two schemes on the more powerful devices, RTX3060 and RTX3090.

C.3 Visualization results

Here we present more visualization results of the regions selected by our masker in the 3-rd block of a LAUDs-ResNet-101 ($S_{\rm net}$ =4-4-2-1) in Fig. 14, which demonstrate that our spatially adaptive inference paradigm can effectively locate the most task-related areas in image features, and reduce the unnecessary computation on those background areas.



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