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High Resolution I_{DDQ} Characterization and Testing - Practical Issues

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ABSTRACT: I_{DDQ} testing has become an important contributor to quality improvement of CMOS ICs. This paper describes high resolution I_{DDQ} characterization and testing (from the sub-nA to μA level) and outlines test hardware and software issues. The physical basis of I_{DDQ} is discussed. Methods for statistical analysis of I_{DDQ} data are examined, as interpretation of the data is often as important as the measurement itself. Applications of these methods to set reasonable test limits for detecting defective product are demonstrated.

I. INTRODUCTION

Improved I_{DDQ} testing for defect detection in CMOS ICs requires that I_{DDQ} be measured to high resolution. This requires understanding of the physical contributions to I_{DDQ}, as well as how seriously the test environment can affect the measurement. Once data are collected, analysis is very important to determine true IC behavior and to improve the process. Sandia National Laboratories has performed high resolution I_{DDQ} measurements and correlated results with similar measurements taken from production IC test equipment. This paper is intended as a guide to making the most accurate I_{DDQ} measurements possible, resulting in enhanced detection of defects such as the microprocessor gate oxide short in Fig. 1.

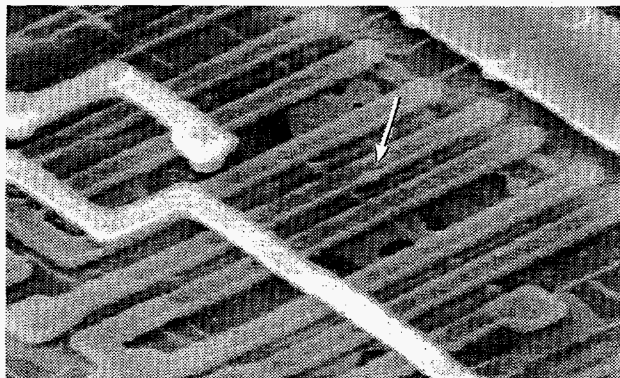

Fig. 1. Gate oxide short of a microprocessor passing all tests except I_{DDQ} (69 uA).

This paper is also a guide to determine what data to obtain, how to display results, and how to compensate for limitations.

The following sections describe various aspects of high resolution I_{DDQ} testing. Section II outlines physical origins of I_{DDQ} and provides data on how voltage and temperature affect the measurement. Section III reviews tester hardware and software issues that affect accurate I_{DDQ} measurement. Section III also describes a characterization procedure used prior to production testing to determine how the production test environment affects the I_{DDQ} measurement. Section IV describes different statistical techniques used to evaluate ICs based on I_{DDQ} values and also suggests options for data analysis to maximize results with reduced data storage. Section V and the Appendix compare data with theory.

II. PHYSICS OF I_{DDQ} - EXAMPLE DATA

I_{DDQ} and Reverse Bias pn Junction Saturation Current

Transistor off-state current (I_{off}) is the drain current when the gate-to-source and source-to-substrate bias voltages (V_{GS} and V_{SB}) are zero. Long channel transistors, approximately defined as those above 0.5 μm channel length, have one dominant and one secondary off-state leakage mechanism. The dominant leakage mechanism is the diode reverse bias saturation current of the drain-substrate (well) and substrate-well *pn* junctions. The secondary leakage mechanism is source-to-drain current due to the weak inversion bias state. At the higher threshold voltages (V_t) of long channel transistors, the weak inversion leakage current is in the femtoamp range while the reverse bias saturation contribution can be three orders of magnitude higher (in the 1-3 pA range). For long channel transistors, the contribution from weak inversion current is usually negligible.

I_{DDQ} of a nondefective CMOS IC is the sum of all individual transistor off-state currents, the reverse bias saturation current of the well-to-substrate junctions, plus any parasitic leakage. In any logic state, slightly more than half of the transistors in a CMOS IC are usually off.

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Combinational CMOS circuits typically have half of the transistors off, but sequential circuits may use access and CMOS transmission gates that place more than half of the transistors in the off-state. If parasitic current mechanisms are controlled to a negligible contribution, a CMOS IC with long channel transistors can be electrically represented in the logical quiescent state by a reverse-biased diode (Fig. 2). The diode equation is

$$I_D = I_{sat}\left[\exp\left(\frac{V_D}{V_t}\right) - 1\right] \qquad (1)$$

where V_D is the diode voltage, V_t is the thermal voltage (kT/q), and I_{sat} is the diode reverse bias saturation current [1]. Typically $I_D = - I_{sat}$ for the reverse biased junctions.

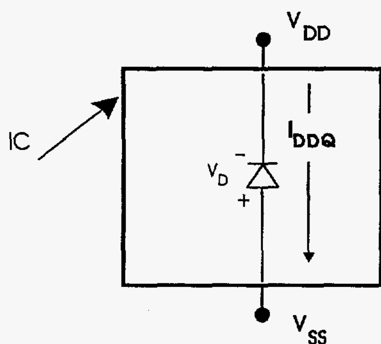

Fig. 2. IC equivalent diode circuit for long channel geometries.

I_{DDQ} of an IC is the sum of individual I_{sat} contributions from well-substrate and drain-substrate (well) *pn* junctions. The dependence of I_{DDQ} on IC junction area A, depletion region width W_D, doping constant N_A, and temperature is shown in (2) for an n^+p junction [1].

$$I_{sat} = Aq \times \left[\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} + \frac{n_i W_D}{\tau_e}\right] \qquad (2)$$

$$= R_1 \text{ (diffusion)} + R_2 \text{ (generation)}$$

The first right-hand side term (R_1) is the diffusion current across the junction and the second (R_2) is generation current from electron-hole pairs that are subsequently ejected from the high electric field of the depletion region. τ_e is an effective electron-hole lifetime constant and τ_n is the minority carrier lifetime.

Junction area A is the major term in (2) when comparing nominal I_{DDQ} for different IC designs since doping levels and reverse bias voltages have tended to be approximately the same for various commercial CMOS ICs. SSI, MSI, and LSI circuits have relatively small total *pn* junction areas with measured I_{DDQ} values in the tens to hundreds of pA's. VLSI circuits with relatively large *pn* junction areas have normal I_{DDQ} values ranging from 1 nA to hundreds of nA's. I_{DDQ} has not increased linearly with the number of transistors since total chip *pn* junction area has risen slowly as transistor dimensions have decreased. The Intel386™EX embedded processor IC with 360,000 transistors (0.6 µm L_{eff}) has a room temperature I_{DDQ} of 50 nA [2,3]. A Hewlett-Packard PA RISC microprocessor with 906,000 transistors has a minimum I_{DDQ} of about 20 nA [4]. A 256K-bit SRAM has a mean I_{DDQ} of about 220 nA while a 1M-bit SRAM from a second manufacturer (over six million transistors) has a mean I_{DDQ} of just over 900 nA. Mean I_{DDQ} for a Sandia radiation-hardened 78k transistor Intel 80C51 emulation (1.2 µm, 8-bit micro-controller) is about 500 pA.

I_{DDQ} Temperature and Voltage Variation

Fig. 3 shows a I_{DDQ} temperature and voltage dependence for two types of CMOS ICs. One is the SA3865 (the Sandia 80C51 above). The 25 °C I_{DDQ} value for this IC at V_{DD} = 5.5 V is approximately 500 pA. The values from -5 °C and higher follow a log distribution while the values below -5 °C tend to flatten out. This is due to the input pins having voltages with just enough offset from V_{DD} or V_{SS} to contribute positively or negatively to I_{DDQ} and to affect the accuracy of the overall measurement at low temperature.

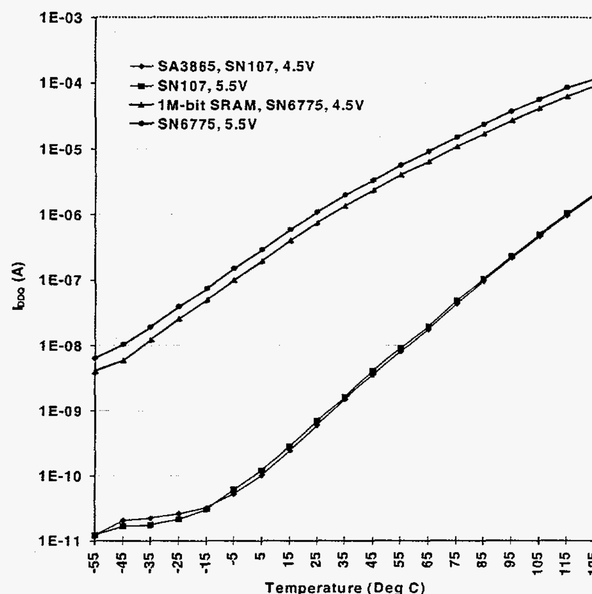

Fig. 3. I_{DDQ} vs. V_{DD} and temperature for two different CMOS IC technologies.

The I_{DDQ} values for a 1M-bit SRAM are also shown in Fig. 3. They also follow a log distribution; however, the slope does not flatten out at low temperatures. Section V and the Appendix discuss these data and show equations comparing the behavior of reverse bias leakage current with subthreshold current.

For large transistor count, small geometry ICs, there is concern (and limited supporting data) that the subthreshold current leakage at room temperature increases so much that it masks the contribution to I_{DDQ} of many defects. The data in Fig. 3 suggest that I_{DDQ} measurement at lower temperature (down to -55 °C) may be practical for those ICs with I_{DDQ} of 2 uA or more at room temperature.

III. TESTER ENVIRONMENT ISSUES FOR HIGH RESOLUTION I_{DDQ} TESTING

The tester environment must be controlled to minimize errors caused by measurement offset. Examples of methods for optimizing the tester environment include the following.

- A low impedance connection between the IC ground pins and tester ground is essential to minimize ground bounce resulting from high current transients during switching of the input and output pins. Ground bounce settling time affects the I_{DDQ} measurement.

- During I_{DDQ} measurement, the input high and low voltage levels must match the power and ground potentials as closely as possible. Condition 1 (input driver voltage having higher voltage than V_{DD} or lower than V_{SS}) can affect I_{DDQ} due to circuitry such as protection diodes being slightly biased relative to V_{DD} or V_{SS}. Condition 2 (input driver voltage lower than V_{DD} or higher than V_{SS}) can increase I_{DDQ} because the normally off input buffer transistors to become slightly more conductive, particularly for smaller geometry input buffers.

Evaluation of condition 1 for the SA3865 unidirectional inputs revealed negligible effect on I_{DDQ} (and I_{SSQ}) for input pin voltage offset of ±50 mV from V_{DD} or V_{SS}. However, the SA3865 bidirectional pins have holding latches, so any input voltage offset from V_{DD} or V_{SS} causes a significant contribution to I_{DDQ} (I_{SSQ}) due to the low impedance of the conducting latch transistors. Condition 2 was evaluated for both the SA3865 and the 1M-bit SRAM. The input voltages were changed in 20 mV increments from -100 mV to +100 mV from each rail, over the temperature range from -55 to 125 °C. For both types of ICs, I_{DDQ} did not change significantly over the input offset and temperature range, indicating the threshold voltages of the input buffer transistors were not low enough to cause appreciable subthreshold leakage for these experiments.

- If possible, all outputs, I/O pins in the output state, and I/O pins in the input state with holding latches for a particular vector should be disconnected from the tester pin electronics prior to the I_{DDQ} measurement strobe using high impedance switches such as mechanical or solid state relays. This reduces the contributions of tester resistive, capacitive and inductive currents to ground. Tester comparator resistances to ground can vary widely (testers used in this study had resistances ranging from 10 kΩ to well over 10 MΩ). The tester I/O circuitry has a capacitance from about 30 to 50 pF per pin. A tester that will be used for I_{DDQ} measurement should have either a very high comparator impedance to ground or have circuitry to rapidly switch to a high impedance comparator.

- Time set switching "on the fly" (test vector rate variation from one vector to the next) is useful when running a vector set to precondition ICs for I_{DDQ} measurement states, such as performing an initialization or reset sequence prior to functional vectors. For example, functional test vectors can be run at full speed until an I_{DDQ}-testable vector is reached. The vector rate is then reduced to enable I_{DDQ} measurement (similar to using a single vector "wait state"). The higher functional rate is then applied until the next I_{DDQ} vector is reached.

- The I_{DDQ} measurement strobe should be placed as close to the end of the vector period as possible for maximum settling time. However, the measurement instrument enable signal controlled by the strobe must not have its trailing edge interfere with the logical switching of the next cycle. For I_{DDQ} measurement instruments that convert current into a voltage, this enable signal voltage should be checked with an oscilloscope to assure I_{DDQ} has settled and to check for any early or late switching pulses.

Even with these precautions, the tester environment can still affect I_{DDQ} testing as shown by the following experiment. Forty-nine 8-bit microcontrollers were used to evaluate the ability to acquire and use I_{DDQ} data. This microcontroller was the SA3865 (described previously). The 49 ICs were divided into two groups: a low I_{DDQ} group (< 50 μA) and a high I_{DDQ} group (> 50 μA). Data were acquired from a production digital tester (Advantest T3342) and analyzed in a variety of ways to compare measurement accuracy and analysis techniques.

The Advantest T3342 has three test circuit options for I_{DDQ} testing: (1) pass/fail testing using a test head-mounted circuit called the "bit current" option [5], (2) measurement using the A-D converter (ADC) on the bit current board, or (3) measurement using the mainframe- mounted precision measurement unit called the "universal DC measurement unit" (UDC). Because I_{DDQ} measurements for each test vector were desired, the measurement

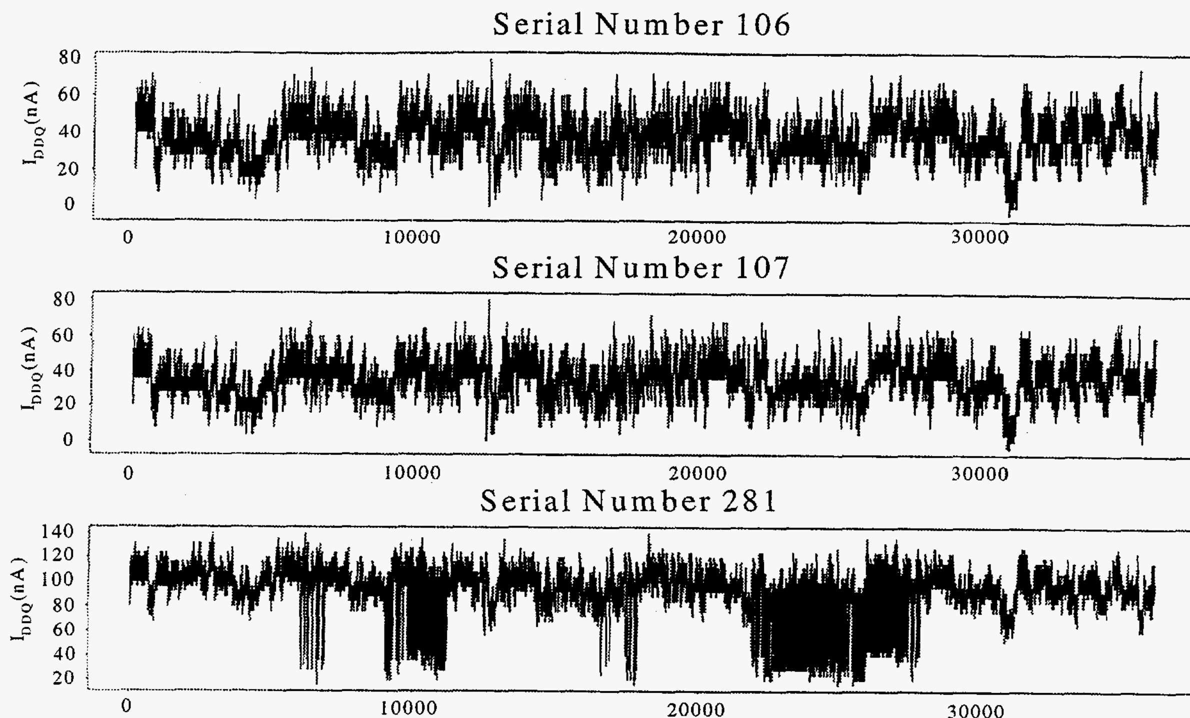

Fig. 4. Advantest T3342 A-D converter I_{DDQ} measurement of three SA3865 ICs.

study compared the capabilities and precision of options 2 and 3.*

The I_{DDQ} ADC measurement circuitry supplied with the tester had a specified I_{DDQ} measurement resolution of ± 4 nA and an accuracy of about ± 50 nA for the 6 μA range. The UDC resolution and accuracy were 0.2 nA and about ± 5 nA, respectively. The use of the ADC was preferred because its test rate of about 1 kHz was considerably greater than the UDC test rate of about 1 Hz. However, there was concern that the ADC might not provide sufficiently precise data.

The first experiment used the commercial Advantest T3342 ADC to make I_{DDQ} measurements. 36,178 test vectors from the production test program were used. These test vectors had a node toggle coverage of 97.03%, which provided a high level of logic activity within the SA3865, assuring that the majority of randomly occurring defects could be detected.

A vector sequence provides more information than a histogram. Fig. 4 compresses the 36,178 I_{DDQ} values (the horizontal axis shows the test vector number, ranging from 0 to 36,177). It shows values for three Sandia ICs: two low I_{DDQ} ICs (SNs 106 and 107) and a slightly higher current IC (SN 281). Some of the variation in the readouts in Fig. 4 was due to the ± 50 nA ADC accuracy. Measurement accuracy was improved by using the (UDC). Three ICs from the low I_{DDQ} group were repeatedly tested with the UDC using a small vector set. It was concluded that the actual I_{DDQ} values for these three ICs were below the current resolution of the UDC.

A higher resolution instrument, a Keithley 236 picoammeter, was interfaced to the T3342. The Keithley 236 is a source/measure unit capable of measurements below 1 pA. It has a resolution of ±100 femtoamperes (fA) in the 1 nA range. This instrument was switched into the V_{DD} circuit node after the T3342 conditioned the IC to a desired measurement vector (Fig. 5). It was used to source V_{DD} and measure I_{DDQ} while under T3342 program control. In order for the 236 to accurately measure I_{DDQ}, a tester subroutine was written that evaluated every vector prior to measurement to ensure that all IC pins in the output state (output pins and I/O pins operating as outputs) were disconnected from their tester comparators. This setup was used to test two of the SA3865s (SN's 106 and 107) tested previously. These ICs were tested at V_{DD} = 5.5 V and room ambient temperature. The data show an improvement factor of at least 10 (the new setup provided I_{DDQ} data in the 300 to 500 pA range versus about 5 nA

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* Precision is a measure of the ability of a measurement method to repeat its measurements. Resolution is the minimum interval between readings at a given range. Accuracy is the ability to measure the true value.

for the UDC). Measurements taken with an HP4145 parameter analyzer and a completely shielded, triaxial environment capable of 1 pA accuracy supported the conclusion that the Keithley/Advantest I_{DDQ} measurements were within ±10 % of their true values.

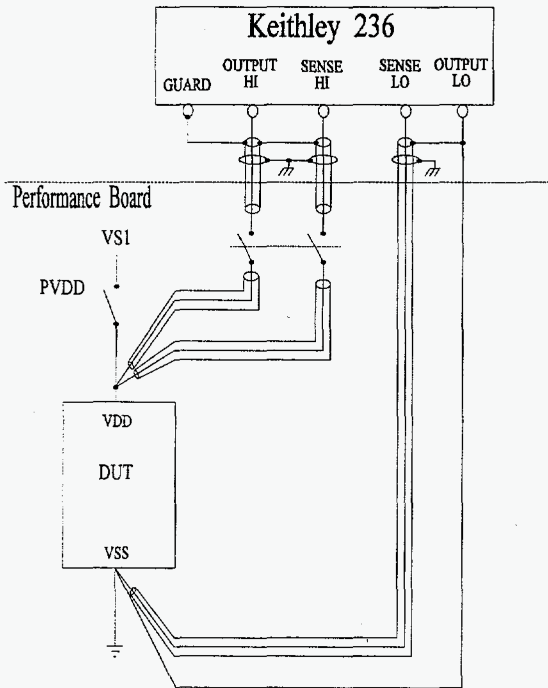

Fig. 5. High-resolution I_{DDQ} setup using a Keithley 236 Picoammeter.

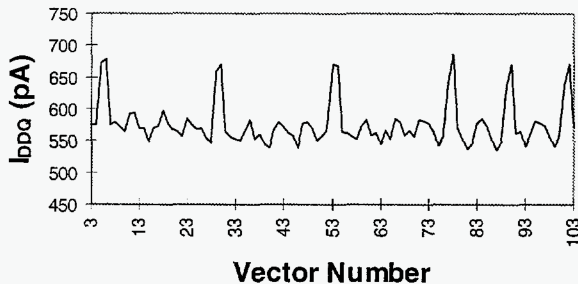

Fig. 6. Keithley 236 I_{DDQ} measurements of SN 106.

The data in Figs. 6 and 7 show the first 100 I_{DDQ} vectors of SN 106 and SN 107 using the Keithley setup. The vector states that had slightly higher I_{DDQ} than others are believed to be due to activation of large *n*-channel paths in the programmable logic array during initial instruction decode. The first three intervals (vectors 3-26, 27-50, and 51-74) show the measurement precision because they repeat the same vector set three times (these vector groups consist of three similar opcode instructions of two cyclesduration and two single-cycle instructions). The measurement of SN 107 in Fig. 7 shows an interesting feature that was a result of temperature stabilization from room temperature (23 °C) to 25 °C during the first 10 to 15 vectors.

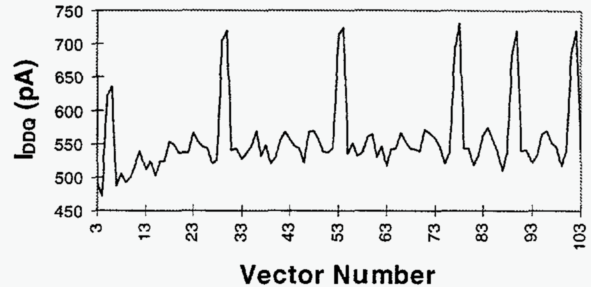

Fig. 7. Keithley 236 I_{DDQ} measurements of SN 107 showing a 2 °C temperature drift in the first minute of measurement.

After stabilization, the temperature was controlled to ± 0.5 °C. The I_{DDQ} information from these three different measurement methods can be used to determine if the lowest accuracy measurement instrument (in this case, the bit current option) provides sufficiently accurate IC current or if the tester environment error dominates. The production test limit setting for I_{DDQ} must take this into account, along with two other details: 1) a knowledge of I_{DDQ} variations resulting from defects and 2) initial pre-production data taken on a sample of product. For this IC, an I_{DDQ} limit of 300 nA at 5 V was used for I_{DDQ} testing with the ADC.

Production I_{DDQ} Testing Issues

During another test experiment, a DIP handler was used to automatically control delivery of the next IC to be tested. Experience with this handler revealed a continuity and a high temperature problem, both of which were found by the I_{DDQ} test. The continuity problem was detected not only by the continuity test itself but also because the I_{DDQ} values had much more variation about a mean value than I_{DDQ} values obtained using a tester DUT board with manual IC insertion.

The high temperature problem was caused by heat radiating up the handler support arm from the lower motor and control assembly to the IC conveyor. The symptom was that the first IC to enter the test area had low I_{DDQ} but subsequent ICs had I_{DDQ} ranging from one to three orders of magnitude above the nominal 350 nA measurements.

Also, if an IC remained in the test area and was repeatedly tested, I_{DDQ} for that IC was initially at a normal low value but then began to increase, often to over 100 µA. Even if temperature control in the IC staging area and test area was used, I_{DDQ} rose by a factor of 10X or more. This occurred during a test which had a long test time (several minutes per IC). This problem is reduced for handler test times under 30 seconds. If a handler is used for I_{DDQ} testing, I_{DDQ} and handler characterization should be performed prior to production testing.

Another issue involves Type II test errors (when a test passes an IC that should be rejected) that can be caused by accuracy skew during test instrument autoranging. For example, I_{DDQ} data from an autoranging instrument (that was changing up into the 600 µA range) were below a limit of 2.8 µA. However, this instrument takes its first sample measurement in the lowest (6 µA) range, then autoranges to the 600 µA range only if the sample measurement exceeds 6 µA. The measurements in the 600 µA range were used by the tester to determine the pass/fail condition using the 2.8 µA limit. The accuracy of the 6 uA range was ± 50 nA while the accuracy of the 600 uA range was ± 4 µA. Since the accuracy of the 600 uA range was near the true I_{DDQ} value, the result was acceptance of ICs that should have been rejected.

IV. STATISTICS

Different I_{DDQ} limits may be selected depending on how the data is interpreted. Subtle differences in I_{DDQ} may not be seen without proper statistical analysis. A careful measurement of the IC (section III) to obtain true baseline I_{DDQ} data is very important.

Statistical presentation of I_{DDQ} data usually is more descriptive on a logarithmic scale than a linear scale. Some sample data are used here for illustration. Fig. 8 shows mostly 1-2 nA data points with one I_{DDQ} value at 1 mA, plotted on a linear scale (data points are connected with straight lines). Fig. 9 shows a logarithmic scale of the same data and the linear average and standard deviation of the data. While the variation in the nA data can now be seen, the mA measurement seems to have an inordinate effect on the mean and standard deviation when plotted in this manner.

Fig. 10 is an alternate data presentation. The average is calculated by taking the average of the logarithms of the data points and then taking the anti-log of this average. An intuitive standard deviation representation on this plot was obtained by taking the standard deviation of the logarithms of the data, adding this to the average of the logarithms of the data, then taking the anti-log of the result and plotting it on a log scale along with the data and log average. This intuitive representation has been used at Sandia when data range widely.

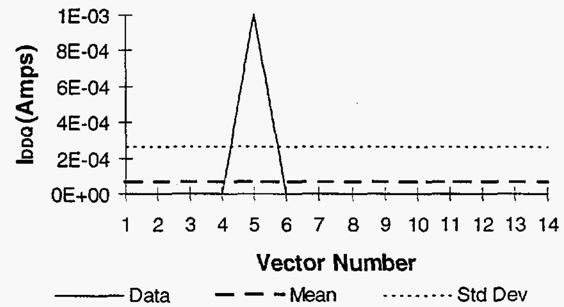

Fig. 8. Linear scale I_{DDQ} data presentation.

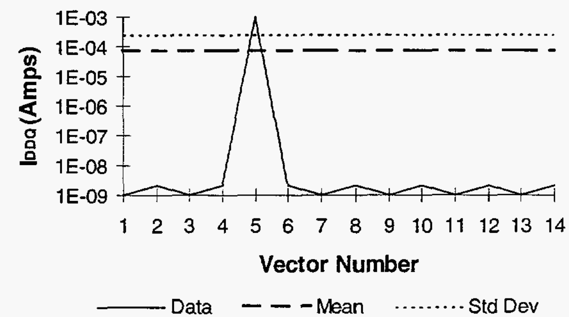

Fig. 9. Same data as in Fig. 8 shown on a log scale.

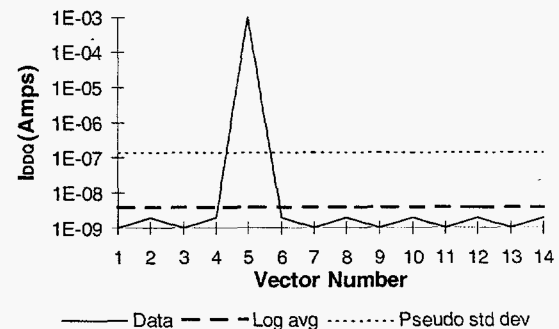

Fig. 10. Data showing log statistics on a log I_{DDQ} scale.

Many companies report graphical data showing maximum I_{DDQ} per IC on the X-axis and number of ICs on the Y-axis. The lowest bar often has the highest number of ICs. These data are typical of those reported in the literature [6-9]. An example of these data is shown in Fig. 11 which shows the maximum I_{DDQ} values for a group of 2635 ICs tested at Sandia. The portion of the chart showing the distribution within the lowest bar (< 750 nA) is not

expanded, giving the appearance of an exponential distribution. However, it is important to know the entire I_{DDQ} distribution including those in the lowest range because these values can reveal problems, either due to the IC or the test environment. For example, a tester resistive path may mask the true I_{DDQ}.

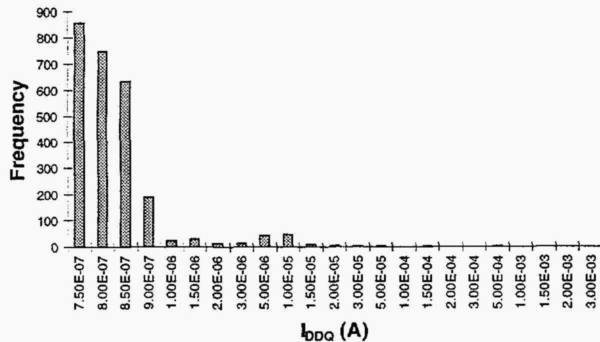

Fig. 11. Histogram of maximum I_{DDQ} for 2635 ICs.

A defect-free sample lot of I_{DDQ}-testable ICs whose currents follow the behavior of those shown in Fig. 3 often has an I_{DDQ} distribution that is approximately Gaussian. Such a data distribution using a sample of ICs is given in Fig. 12. This histogram shows mean I_{DDQ} for 376 ICs. Each IC had 128K I_{DDQ} vectors used to calculate the mean I_{DDQ} values. The shape appears to be Gaussian and includes several outlier ICs outside the apparent normal distribution.

Some companies reject product whose I_{DDQ} values exceed an upper 3σ limit from the mean of the maximum values for a sample of that product. It is our experience that defects that eventually cause IC "reliability" failures do not correlate to I_{DDQ} above a 3σ upper limit for the maximum I_{DDQ} values. Gate oxide shorts, for example, often initially contribute as little as several hundred nanoamps to the overall measurement [10]. Some defects initially contribute very little current, but later cause IC functional failure, along with I_{DDQ} readings several orders of magnitude above the initial reading. If a 3σ limit approach is used, it is better to apply the 3σ deviation to the mean of the Gaussian portion of the mean histogram of the sample than to the mean of the maximum I_{DDQ} readings of the sample. This provides a better representation of the actual background I_{DDQ}.

In Fig. 12, the Gaussian region has an maximum value of 1.2 µA with a mean of 912 nA and a standard deviation σ of 71 nA. This resulted in a upper 3σ limit of 1.13 µA. Allowing for 150 nA of noise (switching transients and

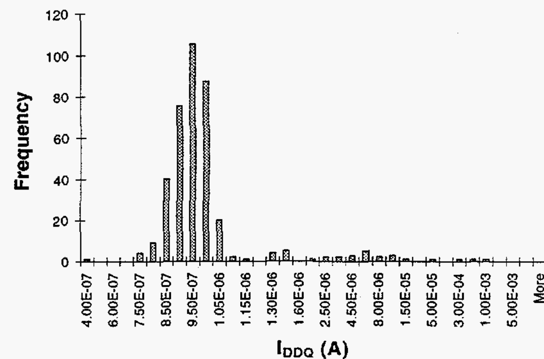

Fig. 12. Gaussian distribution of mean I_{DDQ} over 376 ICs.

instrument limitations of the bit current option I_{DDQ} measurement circuit), the limit was set at 1.3 µA. (Note that limits based on the mean and standard deviation of the mean population will result in tighter limits than those based on individual values).

A bridge defect is shown in Fig. 13. This defect caused an initial I_{DDQ} of 1.6 µA, just over the upper 3σ limit using the Gaussian region method as described above and below the upper 3σ limit for the maximum (exponential-like as in Fig. 11) I_{DDQ} values.

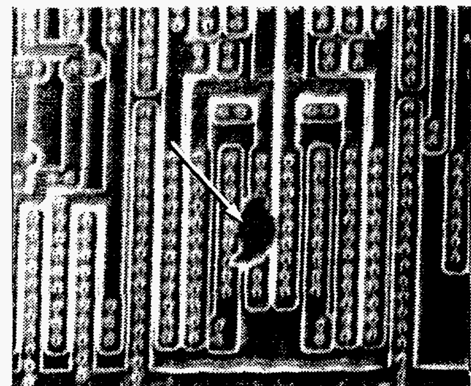

Fig. 13. Bridge defect that caused failure of only the I_{DDQ} test (1.6 µA), but eventually caused functional failure during simulated operation.

The setting of the limit using the recommended method detected this defect. This IC passed all functional tests but later failed in operation with a large increase in I_{DDQ}. Several ICs have exhibited a similar type of behavior.

During production testing, companies often report I_{DDQ} data graphically in bins (meaning the maximum value for

that IC falls between two predetermined I_{DDQ} ranges). At the other extreme, vector number and I_{DDQ} data are recorded for every vector in the vector set. Obviously, the latter method would provide more detail about the process, but the tester time and cost to store these data can cost up to 100 times that of taking binned data.

One compromise method compresses the data using software routines. All vectors are measured and the maximum, minimum, and mean values are determined, and the first few I_{DDQ} values are written to the test data file. This allows analysis of per-vector measurements and also provides a basis for statistical analysis towards IC statistical process control and improvement. The maximum value needs to be associated with the vector number of that measured value to enable diagnosis of rejected ICs.

V. DISCUSSION

Knowledge of the IC being tested and its underlying contributions to I_{DDQ} enable characterization test development for high resolution I_{DDQ} testing. Using a setup similar to the one presented here, high resolution data can be compared with IC tester data to determine tester environment offsets. This can be supplemented with knowledge of input voltage offsets. An initial limit for I_{DDQ} can be selected for pre-production evaluation. If an IC tester is used that can measure I_{DDQ} rapidly for a high coverage functional test set, the data can be analyzed using statistics described in Section IV, where an intelligent choice can be made for the upper 3σ limit from the mean.

A common question about I_{DDQ} test data is: Is I_{DDQ} dominated by reverse bias leakage current or other causes, such as subthreshold leakage current, design-related current, or defect current? The rest of this section discusses how to answer these questions.

If I_{DDQ} is elevated for all ICs, the reason may be design-related (e.g. bus contention), or process-related (e.g. incorrect doping levels). High I_{DDQ} due to the design, layout, process, or defects is often logic state dependent.

Fig. 3 showed the I_{DDQ} variation of two defect-free I_{DDQ}-testable ICs over voltage and temperature. It is outside the scope of this study to exactly fit these data to modeling equations, but these equations and their physical basis help explain the data. In the Appendix, the different effects modeled by equations are analyzed to help explain these I_{DDQ} data. Using these equations, the SA3865 data tend to support normal reverse-bias junction leakage as the dominant mechanism, while subthreshold current may be an additional contributor to the SRAM I_{DDQ}. This may be an indication that short channel effects are beginning to contribute to I_{DDQ} for the SRAM (other 0.5 µm technologies may have higher or lower contribution from short channel effects).

VI. CONCLUSION

This paper describes methods to realize high resolution I_{DDQ} testing. An understanding of both IC physics and tester environment is necessary to get I_{DDQ} measurements that have minimal dependence on the tester environment and that have relevance in characterization of ICs. It is important to fully characterize I_{DDQ} using a sensitive setup before production testing to determine precisely the tester environment contribution to I_{DDQ} measurement. Once this is done, statistics are more meaningful in detection of defective product based on mean I_{DDQ} of good ICs rather than maximum I_{DDQ}.

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APPENDIX

The curves in Fig. 3 for the SA3865 and the 1M-bit SRAM differ greatly in magnitude and somewhat in slope (the SA3865 I_{DDQ} values increase more rapidly over temperature). The equations in Section II are repeated here:

$$I_D = I_{sat}\left[\exp\left(\frac{V_D}{V_t}\right) - 1\right] \qquad (1)$$

$$I_{sat} = Aq \times \left[\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} + \frac{n_i W_D}{\tau_e}\right] \qquad (2)$$

$$= R_1\,(\text{diffusion}) + R_2\,(\text{generation})$$

When reverse bias is applied to a diode, the current saturates at I_{sat}. However, measurement of I_{DDQ} of an IC may not represent an ideal case. To explain data with modeling equations, effects of individual variables must be considered.

First, n_i (the intrinsic carrier concentration) has a temperature dependence [11]

$$n_i = MT^{3/2}\exp\left(\frac{-E_g}{2kT}\right) \qquad (3)$$

where M is a constant containing effective mass terms. n_i at 25 °C for Si is 1.5 x 10^{10}/cm^3. The Si bandgap at 25°C is 1.1 eV, and varies less than 2% over the temperature range -55 to 125 °C. This makes M equal to 5 x 10^{15}/cm^3.

Using (3), n_i at -55 °C is calculated to be 4.1 x 10^6/cm^3 and n_i at 125 °C is calculated to be 4.3 x 10^{12}/cm^3. Therefore n_i increases by a factor of 3.7 x 10^3 from -55 to 25 °C and by a factor of 2.8 x 10^2 from 25 to 125 °C.

Effective electron-hole lifetime τ_e (for the generation term) also varies with temperature as exp[C/kT]. Constant C is dependent on trap levels, junction capture cross-sections and is positive. As the temperature increases, τ_e decreases, but it is theorized as only slowly varying with temperature [1] and thus would have less of an effect on I_{sat} than n_i.

I_{DDQ} for the SA3865 increases linearly on the log plot by 3 x 10^3 from 25 to 125 °C (below about -5 °C I_{DDQ} does not decrease as rapidly due to tester offset). However, for the SRAM the increase in I_{DDQ} from -55 to 25 °C is only a factor of 1.7 x 10^2 and the increase from 25 to 125 °C is only 1.1 x 10^2. This is much less variation than the diffusion term in (2) would predict, since the square root of the diffusion constant divided by electron lifetime would also increase with temperature. This suggests that the R_1 term in (2) does not contribute significantly to I_{DDQ} for either the SRAM or the SA3865.

Depletion width (W_D) of abrupt *pn* junctions found in ICs increases with reverse bias ($V_D = -V_{DD}$) by [1]

$$W_D = \sqrt{\frac{2\varepsilon_s\left(V_{bi} - V_D\right)}{qN_A}} \qquad (4)$$

Since W_D varies only as $(V_{bi} + V_{DD})^{1/2}$, the increase in V_{DD} from 4.5 V to 5.5 V has little effect.

The generation term dominates in Si [1]. The effect of temperature on the n_i term and the τ_e term together could explain the effect of temperature on I_{DDQ} for the SA3865. However, another effect is that as temperature increases the threshold voltage V_{th} decreases. The V_{th} range for an Si/SiO_2 transistor has been measured to be linear over the temperature range -55 to 125 °C and is -4 mV/°C at doping levels of 3 x10^{16}/cm^3 [12]. This could enhance the increase in I_{DDQ} resulting from n_i and τ_e variation.

Thermal voltage, V_t = kT/q, varies also. At 25 °C V_t is 25.8 mV. At -55 °C, V_t is 19 mV and at 125 °C, V_t is 34.5 mV. However, in the ideal case for (1) with V_{DD} = 3.3 to 5.5 V, the exponential term is negligible. This is more evident in the SA3865 curves in Fig. 3, where I_{DDQ} varies little whether V_{DD} = 4.5 V or 5.5 V. This supports reverse bias junction leakage generation as the dominant I_{DDQ} mechanism for the SA3865. The change in current with voltage observed for the SRAM in Fig. 3 depends either on the R_2 term of (2) or some other factor.

For long channel silicon ICs, reverse-bias leakage current is dominated by the R_2 (generation) term in (2) [1]. If the

data at 25 °C from Fig. 3 are used, the ratio of the SRAM current to that of the SA3865 current is approximately 2 x 10^3. Assuming long-channel behavior and approximately equal junction doping concentrations, this translates to

$$\frac{(W_D A)_{SRAM}}{(W_D A)_{SA3865}} = 2 \times 10^3 \qquad (5)$$

The die areas of the SRAM and SA3865 are about the same (within 10%; the SA3865 having slightly less area than the SRAM). The SRAM transistor count is a factor of 80 greater than the SA3865 transistor count. However, the total junction area of the SRAM would not increase by a factor of 80 over that of the SA3865. It would increase, perhaps by a factor of 5 to 10, due to the junction area increase of the slightly longer die. W_D of the junctions for both devices would not vary more than 20% for doping concentrations in the 10^{16} - 10^{17} range. Taking all these into account, the ratio in (5) should still be much less than 2 x 10^3 (in the 10-50 range). This suggests there is another cause for the increased I_{DDQ} of the SRAM.

L_{eff} for the SA3865 is approximately 1.0 µm and for the SRAM is approximately 0.5 µm. V_{th} for the SA3865 is approximately 1.0 V and V_{th} for the SRAM is about 0.8 V at room temperature (taken from I_{DD} vs. V_{DD} curves of the bridge defect in Fig. 13). It is theorized that, as transistor channel lengths decrease to 0.5 µm and below, short-channel effects begin to increase. These effects manifest themselves when for V_{GS} = 0 V and V_{SB} = 0 V the subthreshold current begins to affect the overall I_{DDQ} measurement.

Subthreshold current is dependent on n_i^2 and φ_s [12]. φ_s is linearly related to gate voltage V_{GS}. The subthreshold swing S_t (defined as the change in gate voltage required to effect a decade change in the drain current) varies linearly with temperature. As temperature increases, a greater change in gate voltage is required to cause a decade change in drain current, so S_t increases.

Subthreshold current is independent of drain voltage for V_D > 3kT/q for long-channel devices (e.g. for the off transistor in an inverter). However, for short-channel devices, drain voltage increase has the same effect as raising S_t [13], increasing subthreshold current in the weak inversion region.

The SRAM data in Fig. 3 indicate that the percentage difference in I_{DDQ} caused by the change in V_{DD} (not V_{GS}) from 4.5 to 5.5 V decreases from low to high temperature (from 60% at -55 °C to 25% at 125 °C). The percentage difference for the SA3865 is much less (between 5% and 17% over the temperature range, even though I_{DDQ} for the SA3865 is about three orders of magnitude lower than I_{DDQ} for the SRAM). While V_{th} does decrease with temperature, this does not explain the change in I_{DDQ} with drain voltage for the SRAM. This suggests that subthreshold current may contribute significantly to the SRAM I_{DDQ}.