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A Time-Mode LDI-Based Resonator for a Band-Pass $\Delta\Sigma$ TDC

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***Abstract*—In this paper, a time-mode resonator is presented that is used to realize a second-order bandpass $\Delta\Sigma$ time-to-digital converter (TDC). The resonator is constructed as a cascade of two lossless discrete-time integrators implemented using time-latches and some digital logic in a negative feedback configuration. This paper presents for the very first time the means in which time-mode circuits are used in a negative feedback loop. This achieves high-speed time-mode signal processing without the limitations imposed by switched-capacitor (SC) circuit techniques such as the matching of capacitors to realize precise signal gains. Instead, circuit precision is realized using an on-chip calibration circuit referenced to the main system clock to adjust for timing variations in the time-mode circuits. The operation of the time-mode resonator is verified by realizing a second-order BP $\Delta\Sigma$ TDC. The bandpass noise-shaping is validated with transistor-level simulations.**

***Keywords*—BP$\Delta\Sigma$TDC, noise-shaping, SDU, TLatch, time-mode resonator, time-mode negative feedback.**

I. Introduction

The demand for low-power mixed-signal circuits that can be integrated into nanoscale CMOS technologies is rising constantly. This is driven by the need for longer-lasting portable computing and sensory applications, like smart phones, tablets, IoT, etc.. However, the performance of analog circuits in nanoscaled CMOS processes is degraded due to numerous technological challenges such as a reduction in the intrinsic gain of transistors, increased switching noise because of the closer proximity of circuits, and increased power consumption to maintain the same level of performance as that achieved in older CMOS technologies [1].

An alternative approach to minimize the aforementioned issues is time-mode signal processing (TMSP) whose performance scales well with advanced CMOS technology as it relies exclusively on the switching principle of digital logic circuits. In this approach, signal information is encoded as the time-difference between the rising edges of two independent digital step-like signals, with one of the digital signals acting as the reference. As a consequence, the TMSP technique provides analog signal processing capabilities in advanced CMOS technologies such as FinFET technology that are digitally-enhanced using on-chip calibration techniques, phase-locked to the incoming reference signal. By doing so, CMOS circuits that are robust to process variations, supply level changes and temperature excursions, i.e., PVT effects, can be realized. Moreover, TMSP provides a circuit technique whose dynamic range improves with process scaling. For instance, the upper limit to the dynamic range (DR) of a voltage mode circuit can be quantified as the ratio of the power supply level V_{DD} to the voltage noise limit, $\sqrt{KT/C}$. With advances in technology scaling, V_{DD} must be reduced, hence the DR falls in a voltage mode circuit. In contrast, the DR of a TM circuit, being the ratio of reference clock period T_S to the clock jitter, falls at a much slower rate than VM circuits [2].

Numerous works have proposed various low-pass (LP) architectures of time-based $\Delta\Sigma$ modulators for data conversion applications [3]–[5]. To operate at higher frequencies, a time-mode (TM) bandpass (BP) architecture is required. At the core of this modulator is the need for a second-order TM resonator circuit. In this paper, we introduce a TM resonator to introduce this TM resonator and to demonstrate its application in a BP $\Delta\Sigma$ modulator. While calibration techniques are used to enhance the manufacturability of TM circuits, due to space limitations, these will be the subject of future publication.

An outline of the paper is as follows: Section II will describe the basic TM building blocks that we shall be using for this BP TM resonator. Section III will describe the BP TM resonator using a block diagram perspective. This will be followed in Section IV with a detailed circuit description that we use for our implementation. Section V will provide transistor simulation results for the BP TM resonator incorporated into a Verilog-A realization of the remaining BP time-based $\Delta\Sigma$ modulator. Finally, our conclusions are summarized in section VI.

II. TM Building Blocks And LDI Integrator

The primitive TM element used to construct the 2nd-order BP resonator is the TLatch - a TM memory cell that can store (or write) the time-difference between two step-like digital signals, with one acting as the reference signal [6]. For the sake of clarity, the TM signals will be denoted as $\phi_{in,ref}$ and $\phi_{in,sig}$. For our BP $\Delta\Sigma$ modulator application involving a periodic sampling process, $\phi_{in,ref}$ is assumed to be a two-phase periodic signal with period T_S. Further, the time-difference can be retrieved some time later as the time-difference between two output signals, denoted as $\phi_{out,ref}$ and $\phi_{out,sig}$, through the use of read control signals, denoted as $\overline{R_{sig}}$ and $\overline{R_{ref}}$. The latter signal, $\overline{R_{ref}}$ is triggered or synchronized by the falling edge of the reference signal, $\phi_{in,ref}$. Collectively, the output time-difference ΔT_{out} will be equal to a half-period delayed version of the input time difference ΔT_{in} plus the time-difference between the two read signals, ΔT_R, i.e.,

$$\Delta T_{out}[n] = \Delta T_{in}[n - \frac{1}{2}] \pm \Delta T_R[n] \tag{1}$$

As any TM signal can take on both positive and negative values, it is important to note that the TLatch can perform

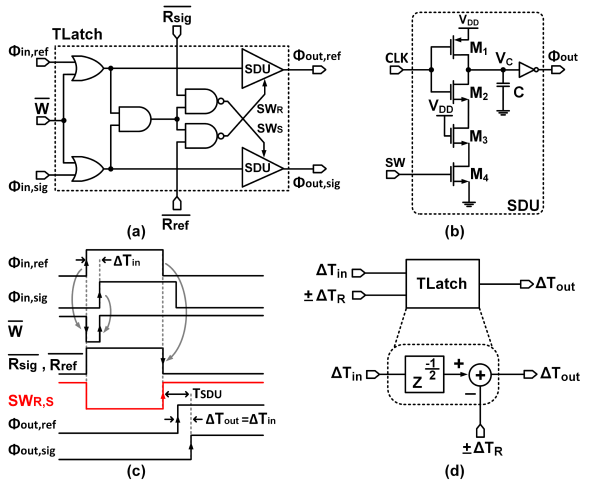

Fig. 1: (a) Schematic of SDU, (b) block diagram of TLatch, (c) timing diagram of TLatch, and (d) z-domain TLatch equivalent representation.

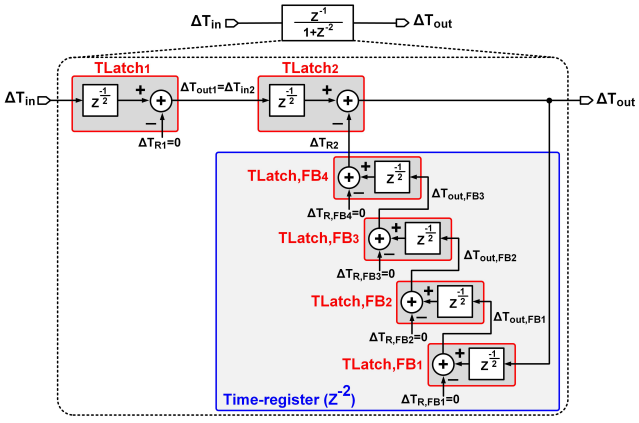

Fig. 2: Block diagram of the proposed TM BP resonator.

both addition or subtraction. In (1), we have listed both cases using the $\pm$ symbol.

A block diagram illustrating the components of the TLatch is shown in Fig. 1(a). Inside the Tlatch is an inverter-like structure called the Switched-Delay Unit (SDU), together with some general logic blocks, such as OR, AND, and NAND gates. The circuit of the SDU is implemented with two inverters; one consisting on a four transistor stack M_1-M_4, and a second simple inverter attached to the output node of the first inverter. Also, connected to this node is a shunt capacitor C that stores the corresponding charge associated with a TM signal. This TM signal is equal to the time difference between the rising edges of the SW control signal and the CLK signal seen in Fig. 1(b).

To illustrate the operation of the TLatch, a timing diagram is provided in Fig. 1(c). In this particular situation, a write signal $\overline{W}$ is activated on the rising edge of the input reference signal $\phi_{in,ref}$. This prepares the TLatch to capture the time-difference between $\phi_{in,ref}$ and $\phi_{in,sig}$, denoted as ΔT_{in}. Correspondingly, a charge is stored on the internal capacitors of the two SDUs and held constant until the falling edge of a read signal has been activated. In this case, the time difference between the two read signals has been set to zero. Hence, an output TM signal equal to the input time-difference appears at the output of the TLatch after some internal delays, designated T_{SDU}.

The TLatch can be represented by the equivalent z-domain model shown in Fig. 1(d) involving the input, output and read signals. Here the feedforward gain between the input and output is represented by a delay $z^{-1/2}$. In digital and SC design literature [7], such a building block is used as an important component of a lossless discrete integrator (LDI).

III. Block Diagram of the BP TM Resonator

A second-order BP resonator can be described with an input-output transfer function given by

$$T(z) = \frac{z^{-1}}{1+z^{-2}} \tag{2}$$

where there is a zero at the origin of the z-plane and two poles at $\pm j1$. According to the block diagram for the TLatch, shown in Fig. 1(d), the TLatch can realize a transfer function with multiples of a half-period delay. A BP resonator with transfer function described in (2) can be realized using six individual TLatches, interconnected as shown in Fig. 2. Two TLatches, TLatch_1 and TLatch_2, are placed in the feedforward path of the resonator. These two elements provide the numerator term of the input-output transfer function. The remaining four TLatches, TLatch_{FB1}, ... TLatch_{FB4} are connected in a single-loop feedback path from the output of the resonator and the read input to TLatch_2. This cascade of four TLatches will be referred to as a *time-register* because its only function is to register the output signal and allow for later retrieval; it does not provide any gain. By doing so, the denominator term $1+z^{-2}$ is realized. It is important to note that the read inputs to all but TLatch_2 are set to zero. This implies that the two read signals, $\overline{R_{sig}}$ and $\overline{R_{ref}}$ for each TLatch are tied together, and all are triggered on the falling edge of the input reference signal $\phi_{in,ref}$ to each TLatch.

Therefore, a TM resonator can be implemented using six TLatches and digital logic gates. It can provide accurate notch-frequency and noise shaping in BP $\Delta\Sigma$ TDC as will be shown in Section IV.

IV. Circuit Implementation of BP TM Resonator

The circuit diagram of the proposed TM LDI resonator is shown in Fig. 3(a), which has a one-to-one correspondance with the block diagram shown in Fig. 2. Each TLatch is assumed to be constructed as shown in Fig. 1(a). Some additional logic gates are used to synchronize the feedback signal from the resonator output with the input reference signal $\phi_{in,ref}$ before applying the read signal to TLatch_2. In addition, the write signals for each of the six TLatches are generated with some additional logic, collectively identified in the diagram as "write signal producer". The circuits details for this block will be explained below.

The timing behavior of the resonator is displayed in Fig. 3(b). The input and the output signals of the resonator, together with the output signals of the six TLatches are shown. In addition, the read signals for TLatch_2 is displayed. All TM signals shown consists of two signals superimposed on each other. This provides a smaller timing diagram, but most importantly, allows one to see the time difference more clearly in the diagram between two signals used to carry the TM information. For example, the read signals shown for TLatch_2

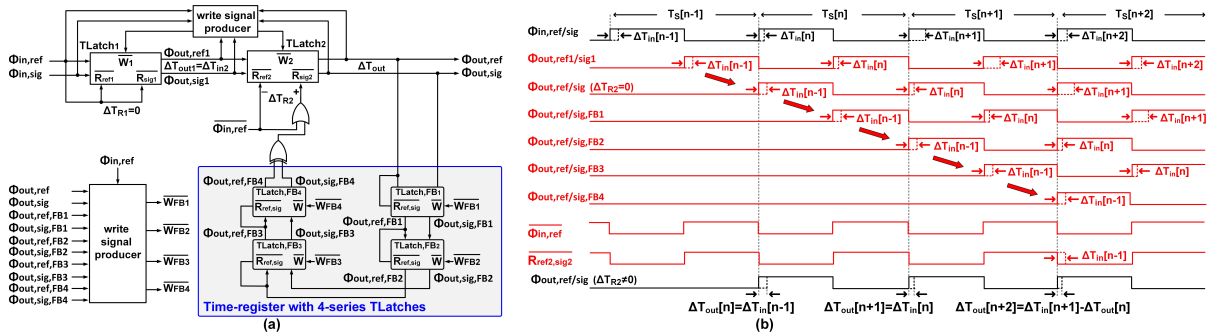

Fig. 3: (a) Simplified circuit schematic of the proposed TM BP resonator, and (b) corresponding timing diagram.

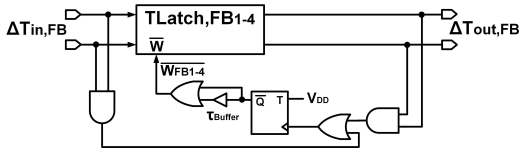

Fig. 4: Write signal producer for a single TLatch stage in the time register.

consists of $\overline{R_{sig}}$ and $\overline{R_{ref}}$ superimposed on one another. The same can be said for all other signals shown.

At the top of the timing diagram is the TM signal corresponding to the time-difference between digital signals $\phi_{in,ref}$ and $\phi_{in,sig}$. Each period of the reference input signal $\phi_{in,ref}$ has been identified with a specific time instant, n, ranging from $n-1$ to $n+2$. In each period, a sample of the time-difference is captured and stored in TLatch$_1$. For instance, the samples shown are $\Delta T_{in}[n-1]$, $\Delta T_{in}[n]$, $\Delta T_{in}[n+1]$ and $\Delta T_{in}[n+2]$. Subsequently, the TM samples captured by TLatch$_1$ are applied as the input to TLatch$_2$ but delayed by 1/2 clock period. If the time-register in the feedback path of the resonator was eliminated, then the output of the resonator, i.e., $\phi_{out,ref}$ and $\phi_{out,sig}$, would be a one clock period delay of the input TM sample. This is captured by the third signal from the top, denoted as $\phi_{out,ref,sig}$. However, the time-register plays an important part at realizing the second-order operation of the BP resonator. To see its effect, consider the TM output of the resonator, i.e., $\phi_{out,ref}$ and $\phi_{out,sig}$, as input to TLatch$_{FB1}$, and its output as input to TLatch$_{FB2}$, and so down the line to TLatch$_{FB4}$. So after two full clock periods, the first sample entering TLatch$_{FB1}$ appears at the output of TLatch$_{FB4}$. This output, after some inversion and resynchronization (not shown), would appear as the read inputs to TLatch$_2$. Subsequently, the feedback signal will contribute to the final output sample value according to the inverse z-transform of (2) and produce an output value given by

$$\Delta T_{out}[n+2] = \Delta T_{in}[n+1] - \Delta T_{out}[n] \qquad (3)$$

In the proposed resonator shown in Fig. 3(a), an important block for synchronizations is the write signal producer. The role of this block is to assert the write signal $\overline{W}$ for each TLatch in the appropriate time sequence. As described in Section II, in the Tlatch, a write signal must be activated once the rising edge of $\phi_{in,ref}$ occurs. Under ideal conditions, i.e., logic assertion can be performed instantaneously, however, in practice, any propagation delay would introduce errors into the TM input sample. To avoid these errors, the write signal $\overline{W}$ should be asserted low as soon as the TM signal in the TLatch has been read completely. This occurs a short time after the rising edge of either $\phi_{out,ref}$ or $\phi_{out,sig}$ is activated,

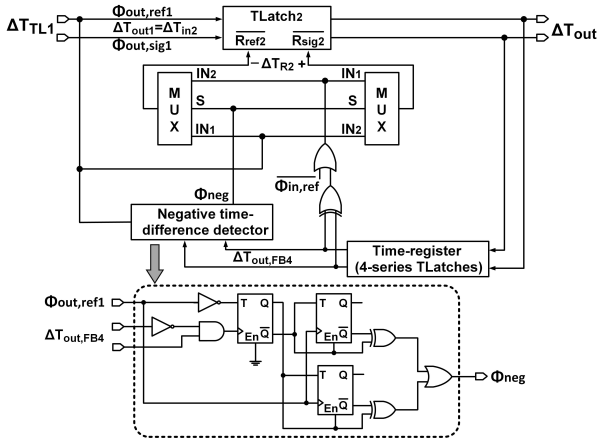

Fig. 5: A portion of the BP resonator with negative signal detect circuitry.

depending on the sign of the output TM variable. The logic diagram corresponding to the write signal produced for each TLatch is shown in Fig. 4. It consists of a few logic gates and a single T-type flip-flop.

A. Challenges of Negative Feedback Loops in a TM Circuit

An important development with this work is the incorporation of a single negative feedback loop in a TM circuit. To our knowledge, such a a realization has never been done before. However, an important issue that arises with the use of a negative feedback loop in the resonator is the creation of a signal that falls outside the synchronization range of TLatch$_2$; in particular, negative TM signals. Consider the timing diagram for the proposed resonator shown in Fig. 3(b). The bottom-most signal conveys the output sampled TM samples from the resonator. Initially, at time instant n, the output is equal to $\Delta T_{in}[n-1]$, but over two cycles of the clock reference, the feedback signal eventually reduces this signal to a smaller TM value corresponding to $\Delta T_{out}[n+2] = \Delta T_{in}[n+1] - \Delta T_{out}[n]$. Depending on the polarity of the samples $\Delta T_{in}[n+1]$ and $\Delta T_{out}[n]$, the output signal $\Delta T_{out}[n+2]$ could go negative. Unfortunately, this implies that the rising edge of the output signal component $\phi_{out,sig}$ would occur before $\phi_{out,ref}$. As the timing of the read and write signals are referenced with respect to this signal, processing errors will result.

To accommodate negative TM signals, the sign of the TM quantity being fed back to the read input of TLatch$_2$ is identified; if negative, the read inputs to TLatch$_2$ are interchanged, otherwise they remain the same. By doing so, the TLatch subtracts the TM read signal from its stored quantity instead of adding it. Fig. 5 illustrates the circuit used to

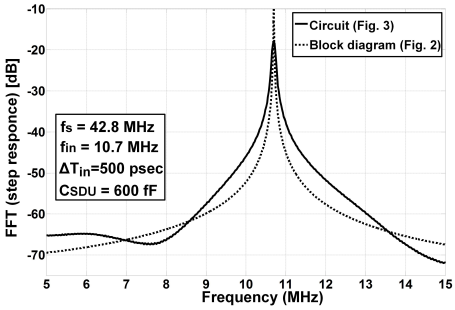

Fig. 6: A comparison of the FFT of the step response of the system-level realization of Fig. 2 vs. the digital circuit realization of Fig. 3.

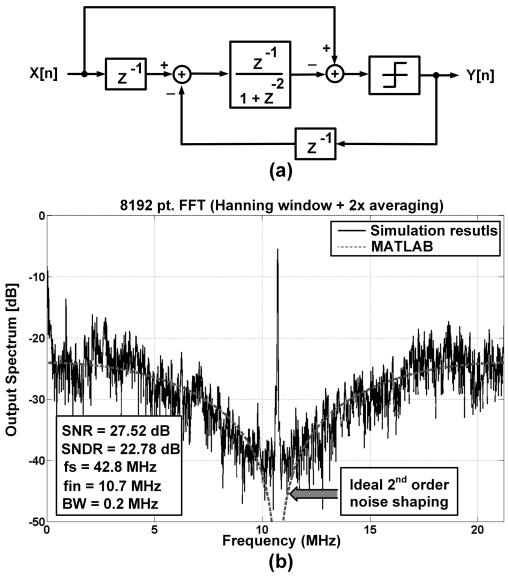

Fig. 7: (a) Second-order BP $\Delta\Sigma$ modulator implementation, (b) output PSD of the BP $\Delta\Sigma$ modulator using the TM LDI-based resonator.

accomplish this task. In this implementation, the negative time-difference (ϕ_{neg}) is detected at each sampling instant by the digital circuit shown in the lower portion of this diagram; if negative, the roles of $\overline{R_{sig2}}$ and $\overline{R_{ref2}}$ are interchanged by the two multiplexers shown in front of the read ports of the TLatch.

V. Simulation Results

The digital circuit implementation of the TM LDI-based resonator was realized in the 1.2 V 0.13-μm IBM CMOS process. Through Spectre and Verilog-A simulations, the TM resonator was found to operate over a signal range from 120 ps to 4 ns with a sampling rate of 42.8 MHz. This LDI resonator was implemented in a BP $\Delta\Sigma$ modulator, which operates at a signal frequency of 1/4 the sampling rate, specifically 10.7 MHz. The static power consumption varies between 4.2 mW to 5.1 mW for DC (steps) inputs that range between 120 ps to 4 ns.

Fig. 6 shows the FFT of the step response of the TM LDI-based resonator for a 500 ps step input operating at a sampling frequency of 42.8 MHz. Here the step response for the system-level realization shown in Fig. 2 and the digital circuit implementation shown in Fig. 3 are compared. A step response was used to compare these two system behaviours, as a sinusoidal excitation near or at 10.8 MHz would cause the resonator output to saturate and produce erroneous behaviour. From Fig. 6, it is evident that the frequency behaviour of the resonator are similar, whereby they both have a resonance peak at the desired frequency of 10.7 MHz and they each have a Q value higher than 10. We attribute the differences to mis-matches in the feed-forward and feedback timing paths of the TM LDI-based resonator. A calibration circuit can be used to correct for these timing mis-matches.

In order to show the ability of the TM LDI-based resonator to be used for noise-shaping applications, the resonator was incorporated into the BP $\Delta\Sigma$ modulator circuit shown in Fig. 7(a). The BP modulator was then excited with a 10.7 MHz sine wave, slightly off the $f_s/4$ quantity (10.8 MHz). The sine wave had a DC value of 0.6 relative to the quantizer output levels of ± 1 and an amplitude of 0.5 V. This signal level was converted into a corresponding TM signal using an ideal voltage-to-time converter whose DC value is 1 ns and with an amplitude of 0.5 ns. The output bit stream was then captured and an FFT was performed. The corresponding PSD was calculated and displayed in Fig. 7(b). As is clearly evident, the quantization noise from the quantizer is noise-shaped in a BP manner centered around 10.8 MHz and a single tone of 10.7 MHz is present in the passband region. An SNR of 27.52 dB and a SNDR of 22.78 dB over a bandwidth of 200 kHz is obtained.

VI. Conclusion

In this paper, an all-digital realization of a TM LDI was presented. It is based on the TM memory cell called the TLatch. For the very first time in time-mode signal processing, a single feedback loop was incorporated into a TM circuit. This enabled the LDI to realize an all-digital second-order TM resonator. Subsequently, it was shown that this resonator could be used to realize a BP $\Delta\Sigma$ modulator for applications in IF data conversion. The fundamental architecture of the proposed design is highly digital and scalable, which makes it very attractive for advanced CMOS process technologies.

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