Manufacturable Nanometer Designs using Standard Cells with Regular Layout

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***Abstract*—In addition to performance considerations, designing VLSI circuits at nanometer-scale process technology nodes demands considerations related to manufacturability and cost. Regular layout patterns are known to enhance resilience to random as well as certain types of systematic variations. In this contribution we assess the implications of this layout regularity using design automation for Critical Feature Analysis (CFA) and raw metrics, such as via count. Using the ISCAS'89 benchmark suite, for each benchmark circuit we compare place-and-route implementations that are based on semi-regular and ultra-regular cell layouts. While the CFA counter-intuitively suggests that implementations using ultra-regular layouts have lower Design for Manufacturability (DFM) scores than those using semi-regular layouts, we find that ultra-regular layouts yield implementations with an average of 22% fewer vias at the cost of a small wire length increase.**

***Index Terms*—Regularity, Regular Fabrics, Standard Cells, Manufacturability, DFM, Lithography.**

I. Introduction

Standard cells are used as a level of abstraction in the design of digital circuits to obtain a robust cost-effort tradeoff in the product development life cycle. In the context of a design flow, they are applied as pre-designed entities, characterized to meet certain performance goals dictated by the technology node.

Traditionally, the constraints involved in the design of standard cells were related primarily to area and performance. With transistor geometries approaching 16 nm, additional factors must be taken into account while designing standard cells in order to compensate for the effects induced by such small geometries. One such factor that must now be considered is the limitation posed by lithography. The lack of light sources less than 193 nm in wavelength has meant that the lithography process is applied alongside costly correction measures (like resolution enhancement techniques) and incremental process improvements (like immersion lithography). This affects the printability of fine layout geometries. It is easy to extend this argument with the observation that a simplification of the layout geometries mitigates the effect of this limitation.

The study of the tradeoffs of implementing regularity led us to study regularity in the implementation of standard cells and existing techniques to assess their manufacturability. Enforcing placement regularity *ad hoc* on designs using foundry-provided standard cells exposes the impact on routability when heuristics are used to perform the routing [1], [2]. The work presented here aims to assess how layout regularity influences manufacturability when it is incorporated into an industrial standard cell-based design flow.

The rest of this paper is organized as follows: Prior work in the area will first be presented followed by a look at the implementation methodology and the results of the study. Conclusions from the study will then be presented and we will present a brief look at future directions for the research.

II. Related Work

In the context of the options available in the design landscape, regularity of layout has been a topic of research since the 1990s. Kutzschebauch *et al.* considered the extraction of regularity at the logic synthesis stage [3]. They applied regularity in conjunction with a driver-transform concept using global information to guide local transformation. The results published in that work are not directly comparable to our own, owing to a large difference in technology node, yet the principles are applicable when regularity at a higher level of abstraction can be extracted.

More recently, work carried out by Menezes *et al.* proposes regular layouts based on a single type of cell to investigate the effects of regularity [4], [5]. Using a custom synthesis tool, they show results indicating an improvement of delay at the expense of area and wire length. Heineken *et al.* [6] used the Poisson yield model proposed by Maly and Deszczka [7], using wafer productivity, defined as the number of working dies per wafer, as a metric to assess the manufacturability of standard cells. Their results showed that standard cells designed with process constraints related to device and interconnect geometries and number of vias/contacts displayed better wafer productivity. Muta *et al.* [8] demonstrated the benefits of regular gate-forming polysilicon (poly) structures on the variation of gate length[1]. They explored the effect of regular gate-forming structures and single orientation; their results, supported using lithography simulations, further underline the benefits of regularity. Similar to this effort, Sunagawa *et al.* [9] study the benefits of regular layout structures on nodes from the 90-nm to the 45-nm technology. Their results underscore the growing need to incorporate regular geometries in standard-cell design flows as the technology nodes scale.

[1]The general variation in the variation of widths in interconnect lines is referred to as Across the Chip Line width Variation (ACLV) when the variation is computed within the die.

In their extensive coverage of regular fabrics, Jhaveri *et al.* propose different implementation strategies [10]. Their work proposes the use of logic "bricks" to implement commonly occurring logic functions in the design, while co-optimizing the yield-limiting layout patterns. Other optimization strategies, aimed at significantly reducing the area overheads in a wider design context, are also proposed. Their results indicate that adopting regularity has no significant impact on circuit performance either. However, co-optimization requires support from the foundry and predictive assessment has not been possible in any other simplified form. The work by Jhaveri *et al.* has been inspired by the highly dense and regular SRAM cell arrays. The styles and the associated restrictions of the SRAM arrays have also been migrated to logic layouts. It should be noted that the density achieved in state-of-the art SRAMs is a result of highly optimized generators specifically created for this purpose by the memory manufacturers. Our work explores more generalized design techniques and methods applicable to standard industrial ASIC flows.

Efforts at Intel propose an approach to designing regular logic blocks using pre-generated layout templates [11] and using extremely regular diffusion structures extending the so-called Lithographers Dream Pattern paradigm [12]. The study by Talalay *et al.* also proposes a possible definition for repeatable block and switch transistor logic model to describe functionality [11]. This will be important when automated means for managing layout complexity at small geometries are desired. The efforts of Ryzhenko *et al.* [12], carried out in the more advanced 32-nm node, feature automatic cell synthesis onto the regular fabric and propose simultaneous cell synthesis and Metal1 routing resulting in area advantages, but incurring a small leakage penalty. In our work, we use Metal2 to complete internal cell connections in the extremely regular cells created for this study.

III. Method of Evaluation

The sections presented so far make extensive use of the terms *regular* and *regularity*. While these terms have been used to refer to structural symmetry as well as geometric symmetry, henceforth any use of these terms refer to symmetry in geometric patterns of VLSI layouts.

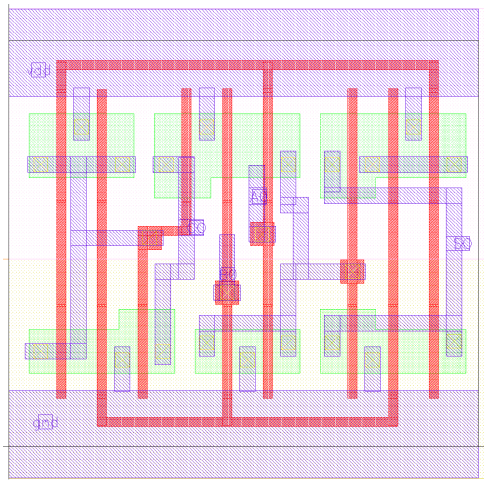
To assess the impact of regularity on standard cell-based implementations, cell libraries with different physical geometries, that is, different degrees of regularity, must be available. While foundry-provided cells are not completely regular, the degree of regularity cannot be ascertained since the full layouts are not available. Beside this lack of observability, foundry-provided cells will not allow for systematic evaluations of variations in the degree of layout regularity. Thus, any assessment of the influence of cell-level regularity using foundry-provided cells would be questionable. In fact, any metric for manufacturability produced by the integrated Design for Manufacturability (DFM) tools would only be manufacturability of the metal layers. In order to carry out assessment of the influence of regular geometries on manufacturability, we implemented standard cells displaying different degrees of regularity [13] for this work using a commercially available 65-nm process. The cells are called semi-regular and ultra-regular cells.

A. Implementation

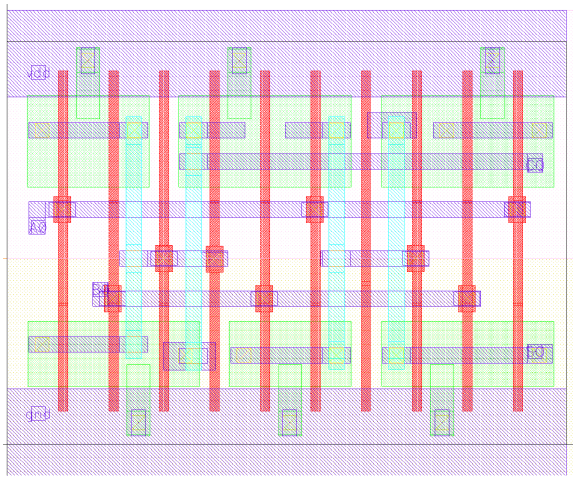
Ultra-regular layouts are implemented using a single device orientation and constant poly pitch, and the directions of the local routing resources are also fixed. In a *semi-regular layout*, widths and spacings for the layout geometries are held as constant as allowed by area considerations, but minor deviations are allowed. Poly pitch is constant across devices with multiple fingers, but routing in poly is allowed. The local routing resources are constrained in the number of layers used (no Metal2 is allowed) but not in the direction. Another difference between the two classes arises when the drive strength is considered. Ultra-regular layouts use a single width for the diffusion layer in order to ease the burden on mask creation. Since single lines of diffusion are used as far as possible, this indicates that, in the absence of transistor stacking, the width of diffusion layers is uniformly increased when higher drive strengths are desired. The impact on performance due to this style of increasing drive strength is not considered in this work, but careful tuning of the width is necessary so that diffusion capacitance is not disproportionately increased. Higher drive strengths are achieved in semi-regular layouts by increasing the widths of diffusion layers for devices in the output stages of gates, inducing some corners in the diffusion layer thereby disturbing the regularity. Fig. 1 shows adder cells implemented using the semi-regular and ultra-regular styles.

In order to focus the assessment effort, only combinational cells are implemented in the variants described above. A total of eight combinational gates are implemented to form a logically complete set. All the standard cells implemented in the semi-regular and ultra-regular libraries for this work are shown in Table I. The variants are noted under the *Comments* column. The libraries do not include And-Or-Invert (AOI) gates, but include a few inverters and buffers. Half- and full-adders are available in another drive strength (designated X4 in the *Comments* column in Table I) in both libraries. For all other logic functions, cells with X4 drive strength are available only in the semi-regular library. In addition to this, the half- and full-adders in the semi-regular library have one additional variant with their inputs ordered in reverse (flipped). For sequential logic, the foundry provided flip-flops are used. The cells are implemented in the Cadence Virtuoso environment [14], [15] and Design Rule Checks (DRCs) are carried out with the Calibre nm-DRC tool [16]. Layout Versus Schematic (LVS) checks are carried out using the Calibre nm-LVS tool [16]. Parasitic extraction is carried out using Synopsys' Star-RCXT tool [17]. The cells are characterized for low power under standard-threshold voltage conditions[2] for an operating voltage of 1.2 V. In addition to the timing data, created in the *.lib* format using Cadence Encounter Library

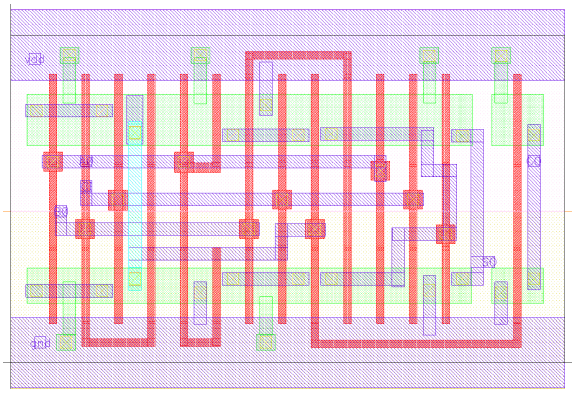
[2]Low-power standard-threshold voltage characterization describes the combination of threshold voltage value and physical geometric features like oxide thickness which influence the threshold voltage and simultaneously results in low static power.



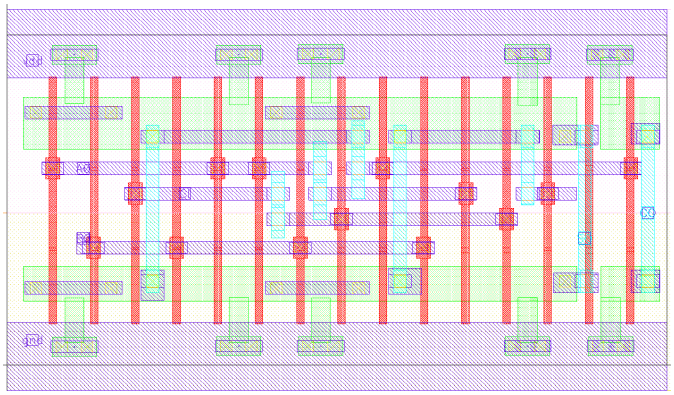
(a) **Semi-regular half-adder**



(b) **Ultra-regular half-adder**



(c) **Semi-regular full-adder**



(d) **Ultra-regular full-adder**

Fig. 1. Custom characterized adders.

TABLE I
IMPLEMENTED STANDARD CELLS

Cell	Comments
AND	X4 available in semi-regular library only.
Buffer	X4 available in semi-regular library only.
Full adder	X4 available in both. Variant with flipped inputs available only in the semi-regular library in both drive strengths.
Half adder	X4 available in both. Variant with flipped inputs available only in the semi-regular library in both drive strengths.
Inverter	X4 available in semi-regular library only.
NAND	X4 available in semi-regular library only.
NOR	X4 available in semi-regular library only.
XOR	X4 available in semi-regular library only.

Characterizer [18], geometry abstracts (in the *.lef* format) are also created using Cadence Abstract Generator [19] for use in a industrial standard cell flow using the Cadence Encounter Digital Implementation (EDI) system [20].

B. Methodology

The ISCAS'89 benchmark circuit suite [21] is used as evaluation vehicle. These benchmark circuits range from a few gates to a few thousand gates and consist of varied functionality. The thirty odd circuits that form this suite offer insights into the behavior of automated synthesis and place-and-route tools. Though all the circuits are physically implemented, six of the benchmark circuits representing different sizes are chosen for the study on manufacturability metrics. The reason for this is that this work focuses on the interactions between device level geometries and the impact they have on manufacturability as indicated by DFM tools, when design automation software is employed to carry out the physical implementation. This being the goal, a sample of representative circuit sizes sufficiently represents the different device level geometries and their interactions.

While it can be viewed as a shortcoming that AOI cells are not available during implementation, this work concentrates on the impact of regular geometries. Observing that AOI gates are simply compound functions of basic gates, created to achieve area density, their absence does not in any way influence the goal of this work. AOI gates will be used in future work in order to save area.

The designs are implemented using common area constraints for each variant; the constraints only specify a target

TABLE II
PHYSICAL IMPLEMENTATION METRICS FOR ISCAS'89 BENCHMARK CIRCUITS

BM	Clock Period (ns)			Slack (ns)			Wire Length (μm)			Via Count		
	SR	SRX4	UR	SR	SRX4	UR	SR	SRX4	UR	SR	SRX4	UR
s27	1.50	1.50	1.50	0.74	0.79	0.70	90.27	97.39	101.36	41	43	40
s208_1	2.00	1.75	2.00	0.73	0.31	0.52	336.05	270.40	294.02	176	160	135
s298	2.00	1.75	1.75	0.35	0.30	0.25	871.89	861.89	932.89	422	389	313
s386	2.00	2.00	2.00	0.43	0.46	0.30	924.89	908.05	989.80	475	487	344
s420_1	2.00	2.00	2.25	0.40	0.54	0.51	762.35	851.63	753.61	433	469	320
s382	2.00	1.75	2.00	0.56	0.39	0.43	922.75	952.61	933.75	499	511	401
s400	1.75	1.75	1.75	0.13	0.31	0.24	1002.35	1070.92	1028.67	540	560	410
s444	2.00	1.75	1.75	0.47	0.33	0.37	979.75	885.61	1075.72	580	567	470
s344	2.00	2.00	2.00	0.06	0.45	0.42	1209.83	962.47	986.83	561	453	330
s641	2.00	2.00	2.25	0.56	0.29	0.60	980.65	1078.12	923.87	515	582	350
s349	2.00	2.00	2.00	0.07	0.47	0.47	1142.09	900.18	1009.46	513	436	367
s713	2.00	2.00	2.00	0.56	0.44	0.48	1017.72	1062.94	867.11	533	577	334
s526n	2.00	1.75	2.00	0.24	0.25	0.32	1199.01	1279.02	1146.40	691	730	499
s526	2.00	2.00	2.00	0.23	0.40	0.30	1356.70	1238.68	1128.09	730	723	560
s838_1	2.50	3.00	2.75	0.31	0.21	0.20	1465.59	1392.78	1617.32	877	834	736
s510	2.00	2.00	2.25	0.05	0.15	0.33	2121.82	1625.75	1848.41	1078	872	740
s820	2.25	2.25	2.25	0.08	0.33	0.21	2160.01	2125.22	2263.58	1084	1123	935
s832	2.25	2.00	2.50	0.19	0.13	0.40	2127.97	2129.82	1991.57	1047	1152	803
s1196	2.75	2.50	2.75	0.24	0.10	0.24	4217.88	4262.70	4347.30	2060	2083	1655
s15850	2.50	2.25	2.50	0.39	0.39	0.51	3605.64	3844.79	3762.77	2145	2259	1730
s1238	2.75	2.50	2.75	0.22	0.18	0.27	4318.40	4647.31	4084.36	2175	2175	1650
s1494	2.75	2.25	2.50	0.00	0.07	0.07	5384.68	5836.41	6052.03	2465	2735	2051
s1488	2.50	2.50	2.50	0.04	0.06	0.05	5864.42	5474.43	6774.21	2689	2521	2266
s1423	3.50	3.00	3.25	0.12	0.28	0.09	4284.82	4177.75	4095.99	2375	2401	1839
s9234_1	2.75	2.75	2.75	0.08	0.33	0.18	7025.85	7378.69	7266.98	3639	3847	2937
s13207	2.25	2.00	2.25	0.38	0.32	0.35	6530.01	6478.76	6033.10	3893	3890	3060
s5378	2.50	2.25	2.50	0.08	0.02	0.08	11177.23	11524.20	10751.32	4773	4949	3810
s35932	6.00	5.50	6.75	0.10	0.10	-0.02	103407.10	108943.43	117733.90	30493	32742	29025
s38417	7.25	6.75	6.50	0.12	0.04	0.05	114400.34	119298.42	109440.71	41087	43979	33174
s38584	7.00	6.25	6.75	-0.32	0.05	0.48	153099.04	104280.03	112528.89	44627	39819	33680

utilization and row density. A common slack constraint of 750 ps is also applied to all designs during logic synthesis. This value represents a realistic target that could be fulfilled by even the largest designs in the suite. The slack constraint is primarily applied in order to obtain a realistic clock period for each design before physical implementation and is achieved by refining the clock period applied to the design during synthesis based on the slack constraint applied. Furthermore, this artificial retiming technique avoids tool-inserted registers from clouding the findings.

In the physical implementations, the metal stripes for the power rails are vertical in the implementations using semi-regular cells and horizontal in the implementations using ultra-regular cells. This style of implementing the stripes is adopted since the ultra-regular standard cells make use of Metal2 to complete internal routing. In the case of semi-regular layouts, with the exception of the full-adder, Metal1 is used exclusively to complete internal routing.

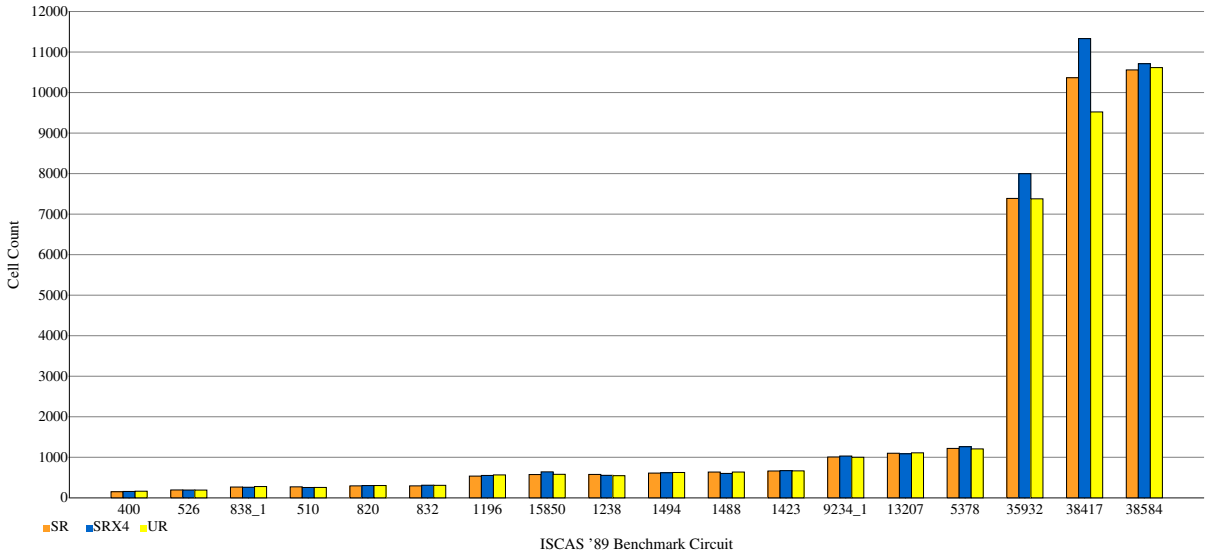
The physical implementation culminates with the GDSII stream produced by Encounter. Raw implementation statistics, such as the number of cells, number of vias, wire length, and slack, are indicative of the quality of implementation and are extracted before proceeding to the manufacturability assessment.

The standard industrial flow relies on traditional full-custom DRC checks at the signoff stage. It is also at this level that DFM checks are incorporated into the verification scheme. In this study, DFM checks are carried out using the Calibre Critical Feature Analysis (CFA) tool [22] using foundry-provided rule sets. This tool is integrated with other DRC and LVS tools belonging to the Calibre suite and relies on detailed rule-based checks to provide metrics on resilience to particle defects, modeling accuracy and process margins[3]. Scores from individual (categorized) rules are cumulated to form the Weighted DFM Metric (WDM) and this value is normalized using a value based on the number of devices in the design. Negative exponentiation of the normalized value results in the Normalized DFM Score (NDS). The WDM can have any value from 0 to infinity, while the negative exponentiation restricts the value of the NDS between 0 and 1. Being cumulative, a lower WDM is desirable for manufacturability or, conversely, a design with a NDS approaching 1 has greater resilience to defects arising out of the manufacturing process. The results of the implementations are shown in the following section.

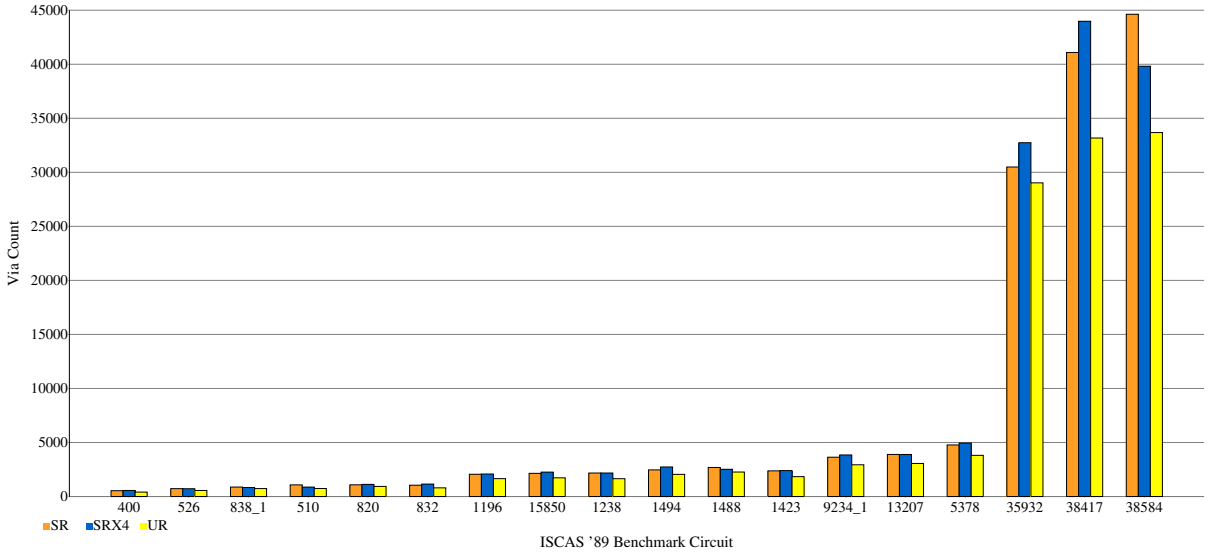
IV. RESULTS

Results are gathered at two different levels of abstraction in order to assess the impact of regularity on manufacturability as indicated in Sec. III-B. Raw metrics are extracted from

[3]"Process margin" is a term indicating tolerances that layout features exhibit to defects induced due to the manufacturing process steps like lithography, optical proximity correction (OPC) and chemical-mechanical polishing (CMP).



(a) **Cell Count**



(b) **Via Count**

Fig. 2. Cell and via counts for some ISCAS'89 benchmarks.

the place-and-route implementation to be representative of the quality of implementation. Manufacturability metrics are then extracted at the signoff stage using the integrated Calibre CFA tools.

A. Raw Implementation Metrics

The ISCAS'89 [21] benchmark circuits have been implemented using the semi-regular and ultra-regular layouts developed for this purpose. Since the semi-regular library is richer in terms of cell drive-strength diversity at this point, altogether three variants have been implemented. The first—designated SR—consists of the basic set of cells from Sec. III-A and has the lowest drive strength. The implementation designated SRX4 includes cells with higher drive strength and the flipped variants, in addition to the basic cells. The SRX4 implementation is used to assess the implications of drive-strength diversity. Both SR and SRX4 are implemented using semi-regular layout geometries. The implementation designated UR consists of all the cells with ultra-regular layout geometries.

All the design variants have been implemented using the same density and aspect-ratio constraints, resulting in little (and therefore un-tabulated) variation of the core area. The clock period for the designs in the benchmark suite (after synthesis) are shown in the first column of Table II. The designs in the suite range from a few gates to a few thousand gates as can be seen from Fig. 2a. The implementation related statistics—the wire length and the number of vias—are also shown in Table II along with the slack after physical implementation.

The slack shows wide variation depending on the size of the design in spite of applying a synthesis slack constraint.

TABLE III
TOTAL DFM METRICS FOR SOME REPRESENTATIVE ISCAS'89 BENCHMARK CIRCUITS

BM	SR				SRX4				UR			
	NoPC	WDM	NDS_T	NDS_{LO}	NoPC	WDM	NDS_T	NDS_{LO}	NoPC	WDM	NDS_T	NDS_{LO}
s27	17	21.72	0.25	0.17	17	24.61	0.27	0.19	17	24.06	0.20	0.13
s400	150	173.21	0.42	0.32	157	187.47	0.47	0.38	163	196.59	0.37	0.28
s820	295	366.71	0.38	0.27	302	374.09	0.46	0.37	303	376.92	0.38	0.29
s5378	1219	1624.21	0.38	0.26	1261	1739.00	0.44	0.32	1207	1772.78	0.37	0.24
s35932	7388	12361.56	0.38	0.24	7998	12999.52	0.43	0.30	7378	15101.28	0.34	0.20
s38584	10559	16576.11	0.28	0.13	10712	13602.82	0.43	0.31	10616	14500.95	0.32	0.20

Looking a little more closely, Table II shows that the slack also depends on cell diversity more and more as the size of the design grows. Although it would appear that the UR and SR implementations outperform the SRX4 implementation, it should be noted that the difference in clock periods and the particular physical implementation iteration influence the slack. The lack of cell and buffer diversity affects the optimization steps of the physical implementation flow negatively and this is evident in the case of the larger designs. The use of heuristics during place and route means that additional variation is introduced into the performance. The variation across the different implementations, given the constituent set of cells, is thus an inexact prediction of performance. In terms of the metal layers used to achieve DRC-compliant routing solutions, the largest designs are routed with Metal5 being the highest layer used. The metal usage for wiring is not excessive since the designs are not too big.

The vias in the interconnect stack have the highest reliability concerns [23], [24], [25], [26], [27] and incorporating regularity at the lower levels of abstraction shows clear benefits with the UR implementations using the lowest number of vias as is evident from Fig. 2b. This reduction in via count can be viewed as a benefit even though it could result in longer wires for the UR implementations, since vias contribute to absolute failures as well as parametric variations. Other variations in the interconnect stack such as wire width and thickness variations may be dealt with using techniques like wire spreading and wire widening, to ensure minimal impact on parametric variation. Those techniques are not considered in the present study.

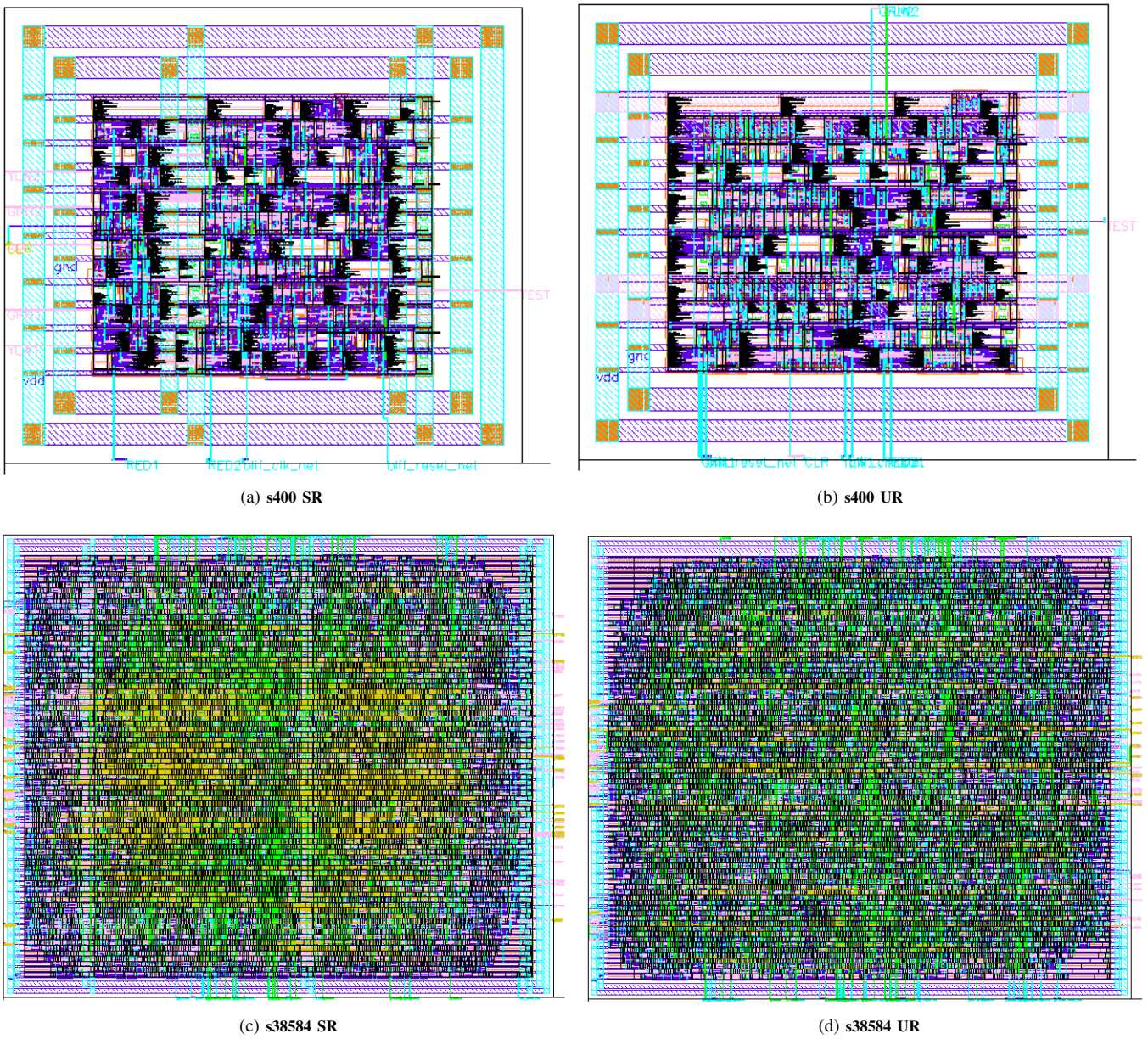
A comparison of wire length of the UR variants against the SRX4 variants (for the tabulated benchmarks) shows an average increase of 0.01%. An average *decrease* of 2.9% is observed when the wire length of the UR variants are compared against the SR variants. In some individual cases, more drastic decreases of wire length can be seen indicating the impact of heuristic routing. For the other designs, however, the change in wire length varies greatly but fewer vias are still used. On average, the use of ultra-regular layout styles results in a 22% reduction in the number of vias compared against the SR and the SRX4 variants, for the tabulated results in Table II. Note that the numbers given here are the result of averaging the percentage increase of the wire length and the percentage decrease of the number of vias computed for each design.

B. CFA Metrics

The raw implementation metrics predict better manufacturability from the point of view of the interconnect stack for the UR implementations since, on average, 22% fewer vias are used for the benchmark circuits considered in this study. This, however, says nothing about the densely packed device geometries that are typically the smallest dimensions in a layout and pose the greatest challenges to manufacturability. In order to form a complete picture of the factors impacting manufacturability, it is necessary to assess all geometries that make up the layout. This is accomplished by importing a GDSII stream produced by Encounter into the Virtuoso environment (Fig. 3) and running DFM checks on it. Having formed a rather general picture of the manufacturability at a higher level of abstraction, where the interconnect stack is prominent, only a few representative layout patterns need be assessed in order to determine the impact of ultra-regular layouts has on a standard cell-based design.

Table III shows the CFA metrics along with the number of physical cells (abbreviated to *NoPC* in the table). As indicated in Sec. III-B this table shows the results for a representative set of the benchmark circuits. The total WDM appears in the column following the number of physical cells. The column designated NDS_T is the total NDS resulting from the WDM in the earlier columns and the normalizor computed for the design. As noted in Sec. III-B, an NDS approaching 1 is better.

Considering only the NDS as a metric of manufacturability indicates the SR and UR variants to be equally manufacturable. However, note that there is a potential weakness in the computation. The UR variants and SR variants display similar NDS values in spite of the fact that the normalizors for the UR implementations are comparable or larger than the normalizors for the SR implementations. The explanation for this lies in the computation method itself. For a given UR implementation, a large number of low weighted scores could lead to a large WDM; however the normalization process could still result in a NDS that is comparable to the NDS of the SR implementation of the same benchmark circuit. Since weights are assigned to potential defects based on foundry experience, one cannot interpret this data without familiarity with the specific fabrication step involved. It is worthwhile to observe also that CFA produces totals for *all* manufacturability-related checks individually. In addition to checks related to the lithography process (affected most by the layout decisions), other potential weaknesses, like SPICE



(a) **s400 SR** (b) **s400 UR**

(c) **s38584 SR** (d) **s38584 UR**

Fig. 3. ISCAS'89 benchmark circuits viewed in Virtuoso.

accuracy, particle defects, and CMP, are also included in the various totals. This in turn influences the total NDS value computed by CFA.

NDS values for only the lithography/OPC-related checks are also presented in Table III (abbreviated to NDS_{LO} in the table). It should be noted here that there are overlapping checks related to particle defects affecting the lithography step that are included here as well. Fig. 4 shows a partial screenshot of one of the CFA runs. It can be seen from Fig. 4 that a fair number of checks are in the defect category and check interconnect layout geometries. The NDS for the LithoOPC group of checks reveals a similar trend to the overall totals.

Quite counter-intuitively, the SRX4 implementations show the best manufacturability based on the NDS as a score, indicating that cell diversity aids manufacturability indirectly given the dominance of interconnect-related checks.

V. Conclusions

This work presents the ISCAS'89 benchmark circuits implemented using standard cells designed with varying degrees of regularity in a commercial 65-nm process. A standard industrial flow is adopted in order to assess the impact regularity has on the manufacturability of a digital design. On average, 22% fewer vias are used by ultra-regular implementations. The DFM metrics measured at the signoff stage using integrated DFM tools, however, indicate relatively less manufacturability for the ultra-regular implementations. The primary reason for this seems to lie in the structure of the rule deck used to

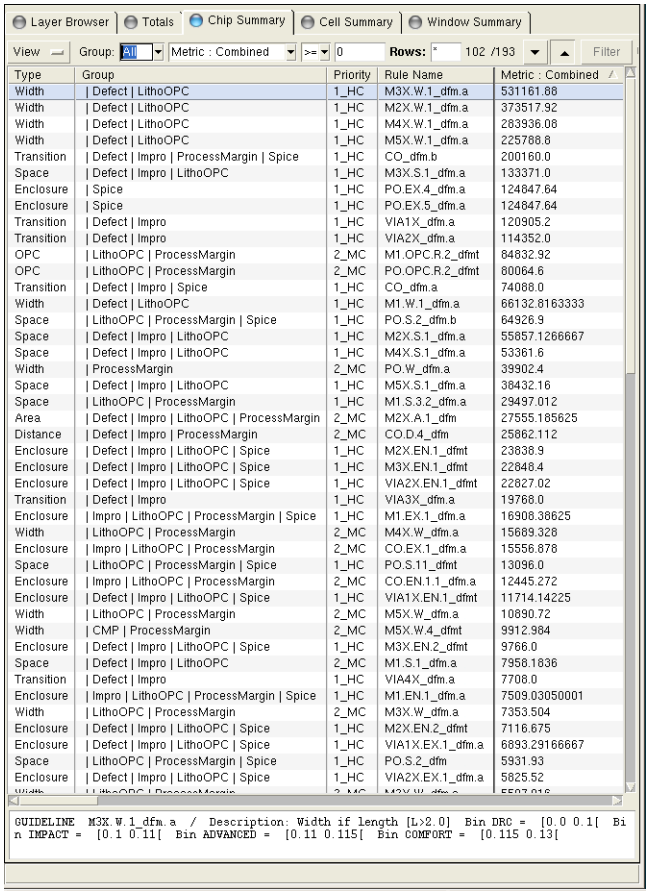


Fig. 4. Individual CFA rule contributions for the various checks.

carry out DFM checks. There is a dominance of defect-related checks targeting the interconnect stack in the various (overlapping) categories. The lithography-related checks show similar trends.

An essential need, therefore, is to reconcile the estimations carried out at design time with the actual manufacturing capabilities available. In order to enable predictive manufacturability assessment it is imperative that metrics be applicable across different levels of abstraction. This presents itself as a clear avenue for future work: identifying the exact nature of the gaps in the manufacturability assessment methods applied prior to signoff. Investigations of the causes can then be incorporated into improved methods for assessing manufacturability.

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