A 10-Bit Algorithmic A/D Converter for Cytosensor Application

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Abstract

A novel 10-bit algorithmic A/D converter for cytosensor applications is described in this paper. The converter is capable of a conversion rate of 1.5-bits/phase. It has advantages compared with conventional architectures with respect to nonideal effects.

I. Introduction

Analog-to-digital converters have been used in many sensor and instrumentation applications to analyse and store data. There is considerable interest in developing a low-cost, portable and generic cytosensor capable of serving as an ecological canary in various applications in order to provide an early warning regarding the presence of life-threatening agents in the environment. Previous research done on this rely on monitoring various responses of living organisms[1]. Most of the existing state-of-the-art sensors are too selective and require extensive use of pattern recognition and skilled human observers that reduce the efficiency. A simple and robust cytosensor system using a novel A/D converter was developed. The embedded converter is described in this paper. The block diagram of the sensor system is shown in Fig.1.

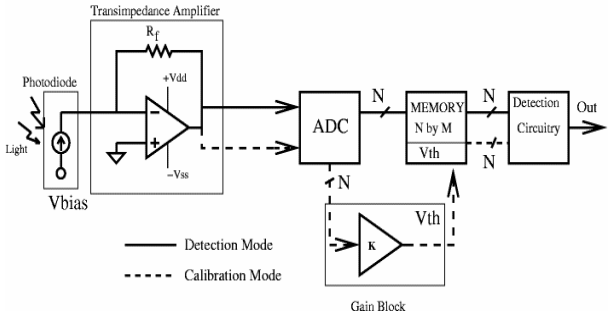

Figure 1. Sensor block diagram

The aggregation or the dispersion behaviour (which controls the intensity of light falling on the photodiode) of fish chromatophores (*Betta Splendens*-siamese fighting fish) is converted into current using a photodiode. The transimpedance amplifier converts the current thus generated into a voltage that is digitized by the A/D converter and stored in memory. Since the cytosensor is designed to be a low-cost, portable sensor, the A/D converter should consume low power and occupy low area. Section II describes the choice of converter and some of the existing algorithmic converter architectures. Section III introduces the novel algorithmic A/D converter. Section IV describes non-ideal effects in the converter, and compares it with the conventional approach and Section V describes needed components and simulation result.

II. Choice of Converter Architecture

A. Choice of Converter

The signal from the photodiode and the transimpedance amplifier are slow and can be considered as DC signals. Its resolution was determined by experimentation. Some of the low and medium speed converters can be used for the design. Successive approximation converters need a 10-bit accurate DAC. Charge redistribution converters have binary weighted capacitances that make the area large. Also, load on the amplifier is high which leads to high power consumption. First-order incremental converters are very slow, and higher-order incremental converters need complex digital and analog circuitry. Algorithmic converters have the simplest circuitry and consume the least power among all the converters.

B. Existing Algorithmic Converters

Most conventional algorithmic converters[3][4][5] employ a 1-bit pipeline stage or a 1.5-bit pipeline stage as their core circuitry. The multiply-by-2 circuit in the architectures is shown in figure 2.

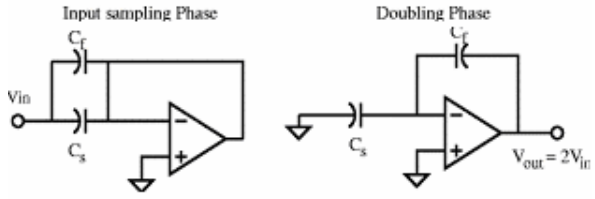

Figure 2. Multiply-by-2 circuit

The architecture in [2] is capable of giving 1.5-bits per phase. The operation of this architecture is as follows: during the reset phase (figure 3a), capacitors C_1 and C_2 are charged to the input voltage and the op-amp is connected in unity gain feedback (op-amp is in reset). Capacitors C_3 and C_4 are the load to the amplifier. The DAC voltage for the next conversion is also obtained during this phase using the 2 comparators.

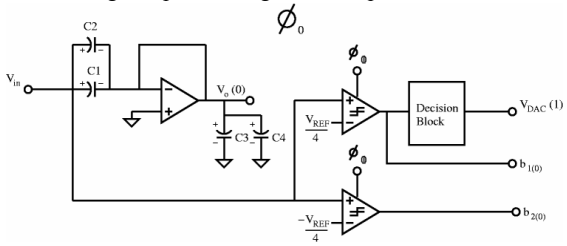

Figure 3a. Reset

During phase 1 (figure 3b), Capacitor C_2 is connected across the op-amp and C_1 discharges into C_2 to produce the desired residue, while C_3 and C_4 act as load capacitors and store the residual output. During phase 2 (figure 3c), C_1 and C_2 are connected as

the load to the amplifier. C_4 is connected across the amplifier, and C_3 discharges into C_4 to produce the residue.

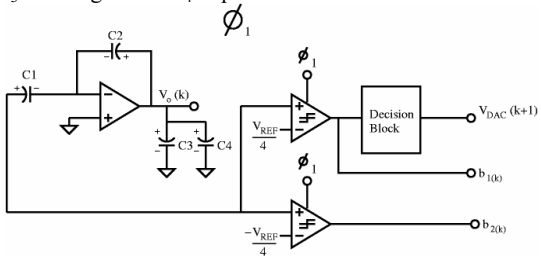

Figure 3b. Phase 1

Phases 1 and 2 are repeated until the required resolution is obtained.

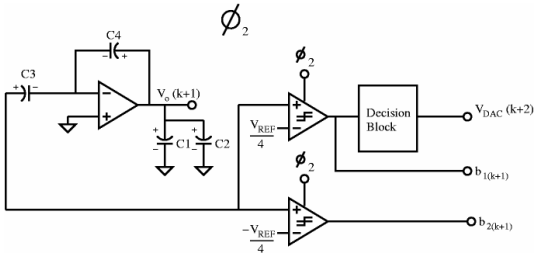

Figure 3c. Phase 2

III. A Novel Algorithmic Converter

The proposed new algorithmic converter contains 3 capacitors. The operation is explained below.

A. Reset Phase (Fig.4a):

Capacitors C_1 and C_2 are charged to the input voltage V_{in}. C_3 is the load capacitor to the amplifier which is being reset. Also during this phase, V_{in} is compared with references $\pm\frac{V_{REF}}{4}$ to give the MSB of the digital code.

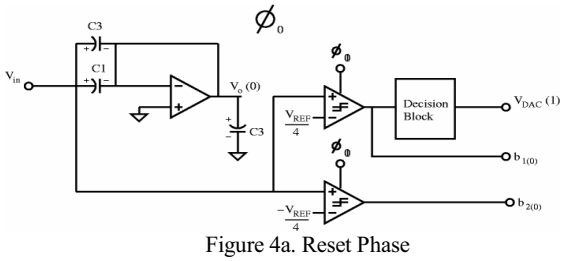

Figure 4a. Reset Phase

B. Phase 1 (Fig.4b):

Capacitor C_1 is connected as the feedback to the amplifier, and connecting one of capacitor C_2 to the DAC voltage does the reference subtraction. Hence C_2 discharges to the DAC voltage, and the residual output of the amplifier is given by

$$V_o(k+1) = 2 \cdot V_o(k) - V_{DAC}(k+1)$$

$$V_{DAC}(k+1) = V_{ref} \text{ for } V_o(k) < V_{ref}$$

$$V_{DAC}(k+1) = -V_{ref} \text{ for } V_o(k) > V_{ref}$$

C_3 and C_1 are charged to the residual voltage. The residual voltage is compared with the reference to obtain the next bit in the conversion and this decides the next DAC voltage to be subtracted from the next residue.

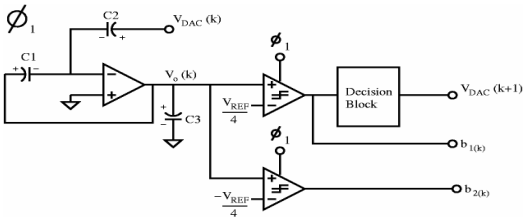

Figure 4b. Phase 1

C. Phase 2 (Fig.4c):

During this phase capacitors C_2 and C_3 are interchanged (C_1 and C_3 have the same potential stored on them), C_3 is connected to DAC voltage and the next residue is obtained. The next bit is obtained by comparing the residue to the reference.

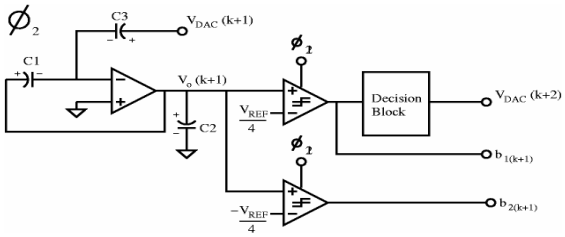

Figure 4c. Phase 2

The outputs of both comparators are used in the decision block to determine successive DAC voltages.

IV. Performance Limitations

A. Comparator Offsets

The use of a 1.5-bit per phase architecture removes the problem of comparator offsets. Offsets up to Vref/4 can be tolerated. The design of the comparator is easier and high-speed low power comparators can be used.

B. Amplifier Offsets

In the new architecture, the amplifier offsets affects the residues exponentially in each cycle. The residue equation is given as follows:

$$V_O(k) = 2^k V_{in} - 2^{k-1} V_{dac}(1) - 2^{k-2} V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + (2^{k-1} - 1) V_{os}$$

Since the input and the first residue are not affected by the offset, the first and the second MSBs of the converter output are offset free. The offset effect of the converter is illustrated in Figure 5. Redundancy error correction makes the offset of the amplifier give rise only to an effective offset in the system. The transfer curve of the ADC shifts left or right depending on the sign of the offset. Simulations show that the final offset of the system is twice the amplifier offset.

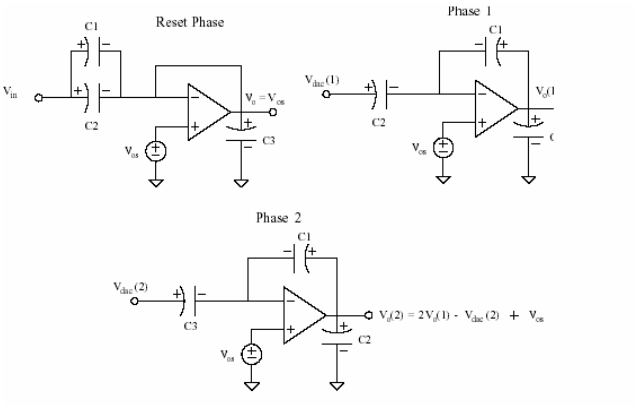

Figure 5 Effect of amplifier offset in the new converter

In the conventional architecture, the residues are affected by the offset effect as given by

$$V_o(k) = 2^k V_{in} - 2^{k-1}V_{dac}(1) - 2^{k-2}V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + 2(2^{k-1}-1)V_{os}$$

The final offset is twice that of the proposed new converter. With Vin = 0, the output of the converter represents the offset that can be stored and subtracted from subsequent output codes.

C. Finite Op-Amp Gain

Finite op-amp gain reduces the gain of the stage from 2 and thus causes INL and DNL. For the multiply-by-2 circuit shown in figure 4 the stage gain is given by

$$V_o = \frac{C_s + C_f}{C_f(1+\frac{1}{A}+\frac{C_s}{C_f A})}V_{in} \approx 2(1-\frac{2}{A})V_{in}$$

In the proposed approach the residue with op-amp finite gain is given by

$$V_o(k) = \left[2 - \frac{1}{Ao}\left(3+\frac{C_p}{C}\right)\right]V_o(n-1) - \left[1-\frac{1}{Ao}\left(2+\frac{C_p}{C}\right)\right]V_{dac}(n)$$

Cp is the parasitic capacitance at the virtual ground node of the op-amp. From simulations, an op-amp DC gain of 75 dB is required for the INL to be less than 0.5 LSBs. Simulation was performed with a parasitic capacitance of about 1.2pF at the virtual ground node of the op-amp ($C_1 = C_2 = C_3 = C = 2$ pF).

D. Capacitor Mismatch

Good layout techniques can give 0.1% mismatch, which corresponds to 10 bits of accuracy. For $C_2 = C_1(1+\alpha)$ and $C_3 = C_1(1+\beta)$, the residue equations during phase 1 and phase 2 are given respectively by

$$V_o(n) = V_{in}\cdot(2+\alpha)^{\frac{n+1}{2}}(2+\beta)^{\frac{n-1}{2}} - V_{dac}(1)\cdot(1+\alpha)(2+\alpha)^{\frac{n-1}{2}}(2+\beta)^{\frac{n-1}{2}}$$
$$- V_{dac}(2)\cdot(1+\beta)(2+\alpha)^{\frac{n-1}{2}}(2+\beta)^{\frac{n-3}{2}} \ldots\ldots - V_{dac}(n)\cdot(1+\alpha)$$

and

$$V_o(n) = V_{in}\cdot(2+\alpha)^{\frac{n-2}{2}}(2+\beta)^{\frac{n}{2}} - V_{dac}(1)\cdot(1+\alpha)(2+\alpha)^{\frac{n}{2}}(2+\beta)^{\frac{n-2}{2}}$$
$$- V_{dac}(2)\cdot(1+\beta)(2+\alpha)^{\frac{n-2}{2}}(2+\beta)^{\frac{n-2}{2}} \ldots\ldots - V_{dac}(n)\cdot(1+\beta)$$

The INL and DNL curves for 0.1% mismatch is shown in Figure 6. Mismatch > 0.1% makes the INL > 0.5 LSBs. MATLAB was used for simulations.

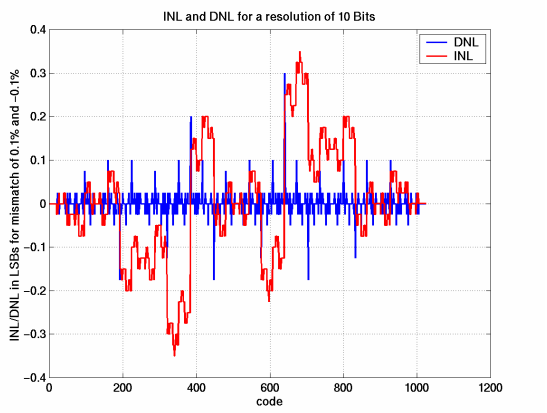

Figure 6 INL and DNL curves for a capacitor mismatch of 0.1%

E. Thermal Noise

The output referred kT-C noise of the multiply-by-2 circuit is given by

$$\frac{2kT}{C_2}\left(1+\frac{C_1}{C_2}\right) \approx \frac{4kT}{C}$$

The signal gain is 2 and assuming C1 = C2, the input referred noise is given by kT/C, where C1 = C2 = C.

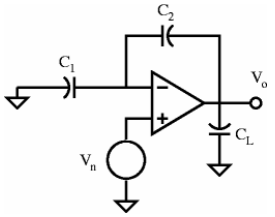

Figure 7. Op-amp in feedback configuration

For the feedback op-amp shown in Figure7, the input-referred noise is given by

$$\frac{4kT(1+N_f)}{3C_{L,eff}}\cdot\frac{1+\frac{C_1+C_p}{C_2}}{\left(\frac{C_1}{C_2}\right)^2}$$

Here,

$$C_{L,eff} = C_L + \frac{C_2(C_1+C_p)}{C_1+C_2+C_p}$$

N_f refers to the contribution of the load transistors, and Cp represents the parasitic capacitance at the virtual ground node of the opamp. For $C_1 = C_2$, the total input referred noise of the multiply-by-2 circuit is given by

$$\overline{V_{n,stg}^2} = \frac{kT}{C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$$

The total noise of an algorithmic stage using the above circuit is given by

$$V_{n,tot}^2 = V_{n,1}^2 + \frac{V_{n,2}^2}{4} + \frac{V_{n,3}^2}{16} + ...$$

where $V_{n,1}$ represents the noise from the ith cycle.
In the new converter, C1 is switched only in the reset phase and the noise in this phase is given by

$$\overline{V_{n,stg}^2} = \frac{kT}{C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$$

In the subsequent phases C1 is never switched and hence does not contribute to the total noise. The noise in the subsequent cycles is given by

$$V_{n,i}^2 = \frac{kT}{2C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$$

The total input referred noise is given by $\frac{7}{6}\cdot\frac{kT}{C} + \frac{4}{3}\cdot\frac{8kT(1+N_f)}{3C_{L,eff}}$.

For a single stage op-amp, $C_{L,eff} = \frac{3C}{2}$, whereas for a 2 stage op-amp $C_{L,eff} = C_c$, where C_C is the compensation capacitor of the 2-stage op-amp.

F. Reduced Area and Power Consumption

Let C_{new} and C_{old} be the switching capacitors in the proposed and existing architectures respectively. Assuming single-stage op-amps for both the architectures, the respective load on the op-amps is ($3C_{new}$/2) and ($5C_{old}$/2). Assuming the input pair is the dominant source of noise in both the converters, the total input referred noise is given by $\frac{191kT}{54C_{new}}$ and $\frac{132kT}{45C_{old}}$ respectively. For equal SNR $\frac{C_{new}}{C_{old}} = 1.2$. Thus, there is a 10% reduction of capacitor area in the proposed architecture.

(1) For equal slew rate the current ratio is given by $\frac{I_{old}}{I_{new}} = \frac{5C_{old}}{3C_{new}} = 1.3$. The existing architecture requires 30% more current.

(2) For equal bandwidth, $\frac{gm_{old}}{gm_{new}} = \frac{5C_{old}}{3C_{new}}$. Since $gm\alpha\sqrt{I\frac{w}{l}}$, $\frac{I_{old}(w/l)_{old}}{I_{new}(w/l)_{new}} = 1.69$. Considering equal slew rate, a 30 % bigger input transistors are required which increases the parasitic at the op-amp input. As mentioned earlier, virtual ground node parasitic reduces the interstage gain, which introduces non-linearity. Avoiding this will lead to a 69% higher current in the existing architecture.

Thus the proposed architecture has atleast 30% savings in power and 10% savings in capacitor area.

V. Circuit Components and Simulations

The proposed algorithmic converter requires an op-amp, 2 comparators, 3 capacitors and MOS switches. System level simulation was done using C programs and MATLAB. The following plot shows the FFT of the converter output simulated using MATLAB. The FFT plot is for an oversampling ratio of 64 and a mismatch of 0.2 % in the sampling capacitances. The obtained THD is -60.17 dB.

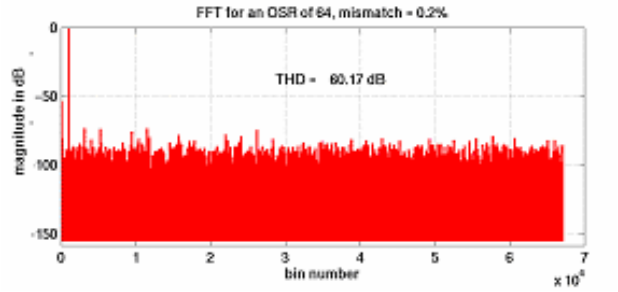

Figure 8. FFT of converter output

VI. Conclusions

An algorithmic converter with a novel switching scheme has been proposed. The conversion rate is 1.5-bits/phase. The non-ideal effects in the converter have been compared with existing architecture with the same conversion speed. The proposed converter was found to be economical in terms of both power and area.

VII. Acknowledgement

This research was funded by the Catalyst Foundation.

References

[1] EILATox-Oregon Workshop, September 9-13, 2002, Oregon State University.

[2] K. Nagaraj *et al.*, " A 250 –mW, 8-b, 52-Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers," IEEE J. of Solid-State Circuits, Vol. 32, No. 3, pp. 312-320, March 1997.

[3] Shang-Yuan *et al.*,"A Digitally Self-Calibrating 14-bit 10-MHz CMOS Pipelined A/D Converter," IEEE J. Solid-State Circuits, Vol 37, pp. 674-683, June 2002.

[4] Hae-Seung Lee, "A 12-bit 600 ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC," IEEE J. Solid-State Circuits, Vol 29, No. 4, pp. 509-515, April 1994.

[5] Christian Enz *et al.*, "Circuit techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," Proceedings of the IEEE, Vol. 84, no. 11, pp. 1584-1614, November 1996

[6] Roubik Gregorian & Gabor C Temes, "Analog MOS Integrated Circuits for Signal Processing", Wiley-Interscience, 1986.