

Automatic Reconfiguration of Untimed Discrete-Event Systems

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Abstract

This work introduces a general formulation of the reconfiguration problem for untimed discrete-event systems (DES), which can be treated directly by supervisory control theory (SCT). To model the reconfiguration requirements we introduce the concept of *reconfiguration specification* (RS); here *reconfiguration events* (RE) are introduced to force a transition from one system configuration to another. Standard SCT synthesis is employed to obtain a *reconfiguration supervisor* (**RSUP**) in which designated states serve as the source states for RE. The reconfiguration problem itself is formulated as that of establishing guaranteed finite reachability of a desired RE source state in **RSUP** from the current state in **RSUP** at which a change in configuration is commanded by an external user. The solvability (or otherwise) of this reachability problem is established by backtracking as in standard dynamic programming.

1 Introduction

Highly complex systems are typically composed of many components. A system configuration (mode) is implemented by a particular subset of the system’s components exhibiting a specific functionality. Dynamic reconfiguration is the automatic switching of the current configuration of the system to a new one commanded by the system’s external user (e.g., manager of a factory workcell). The importance of reconfiguration, in the case of complex systems, is two-fold. First, the model now embraces multimodal systems, thereby achieving multifunctionality through multimodality. Second, since reconfiguration enables switching from a faulty configuration to a sound one, the overall system’s reliability, and its robust response to faults, are each enhanced.

There have been extensive investigations into the notion of reconfiguration in the context of different complex systems such as power systems ([1–3]), embedded systems ([4, 5]), hybrid systems ([6, 7]), and manufacturing systems ([8]). Petri-net-based modeling of DES has also been employed to realize dynamic reconfiguration tasks. For example, [9] proposed a communication protocol to coordinate reconfiguration of software agents by coordination matrices. Many other applications of Petri nets could be cited of dynamic reconfiguration of complex systems (e.g., see [10]).

Moreover, some efforts have been applied to engineer reconfigurable DES. For instance, [11] recommended a coordinated approach to solve the problem; the technique stressed communication among the subsystems of the DES. It was further assumed that all subsystems are equipped with coordinators to manage the system reconfigurations. The virtual coordinator exchanges messages with subsystems separately, rather than subsystems intercommunicating directly. Whenever a subsystem desires to execute a global reconfiguration, it first requests permission of the coordinator. However, the approach seems not to be efficiently scalable.

Recently, the notion of state attraction [12] has been used to reconfigure DES by regular specifications. In particular, a coordination automaton (CA) is generated to weakly attract a required reconfiguration. The path from each initial state of CA to its marked state guides a particular supervisor to realize the required reconfiguration [13]. However, this approach is unable to reconfigure DES at any arbitrary state, and the synthesized CA is nondeterministic including more than one initial state.

For the reconfiguration control of DES, SCT [14] has already shown promise. Recall that in SCT a supervisor is synthesized for given formal specifications in such a way as to be *correct by design*. In this spirit [15] addressed the dynamic rescheduling of a timed DES (or TDES) by use of a timed supervisor. In addition [16] proposed a method based on Petri nets and integer programming to optimize the cost of reconfiguration. The method uses linear constraints to synthesize deadlock-free supervisors by SCT.

This paper presents an automatic procedure to reconfigure DES by SCT dynamically. To this end, we introduce the notion of reconfiguration specification (RS) to model reconfiguration requirements; this specification is incorporated into the SCT supervisor synthesis in the usual way. The resulting supervisor not only realizes the behavioral specifications of the DES, but also switches between configurations when reconfiguration is commanded by an external system manager. Finally, it is necessary to know whether a desired reconfiguration is achievable from a particular state of the supervisor or not. At that point we apply a backtracking path-finding algorithm based on dynamic programming to collect all forcible paths (if any) that solve the intended reconfiguration problem.

The paper is organized as follows: Section 2 is devoted to preliminaries. Section 3 elaborates on the realization of the automatic dynamic reconfiguration by SCT. The new definition of RS is stated in Section 3.1. Section 3.2 provides the **RSUP** synthesis process. The reconfiguration problem is formally defined in Section 4.1. In Section 4.2 we describe the collection of forcible backtracking paths; the formal algorithm is presented Section 4.3. Section 5 illustrates the proposed method with an example, and conclusions are drawn in Section 6.

2 Preliminaries

SCT controls DES modeled by the Ramadge-Wonham framework [17, 18]. A DES is formally represented by a generator, say

$$\mathbf{G} = (Q, \Sigma, \delta, q_0, Q_m),$$

where $\Sigma = \Sigma_c \dot{\cup} \Sigma_u$ is a finite alphabet of event labels, partitioned into the *controllable* event labels and the *uncontrollable* ones; Q is the *state set*, assumed finite; $\delta : Q \times \Sigma^* \rightarrow Q$ is the *extended partial transition function*; q_0 is the *initial state*; and $Q_m \subseteq Q$ is the subset of *marked states*. The *closed behavior* and the *marked behavior* of \mathbf{G} are the languages

$$L(\mathbf{G}) := \{s \in \Sigma^* \mid \delta(q_0, s)!\}$$

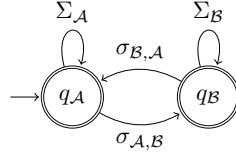


Figure 1: Generator of a binary RS

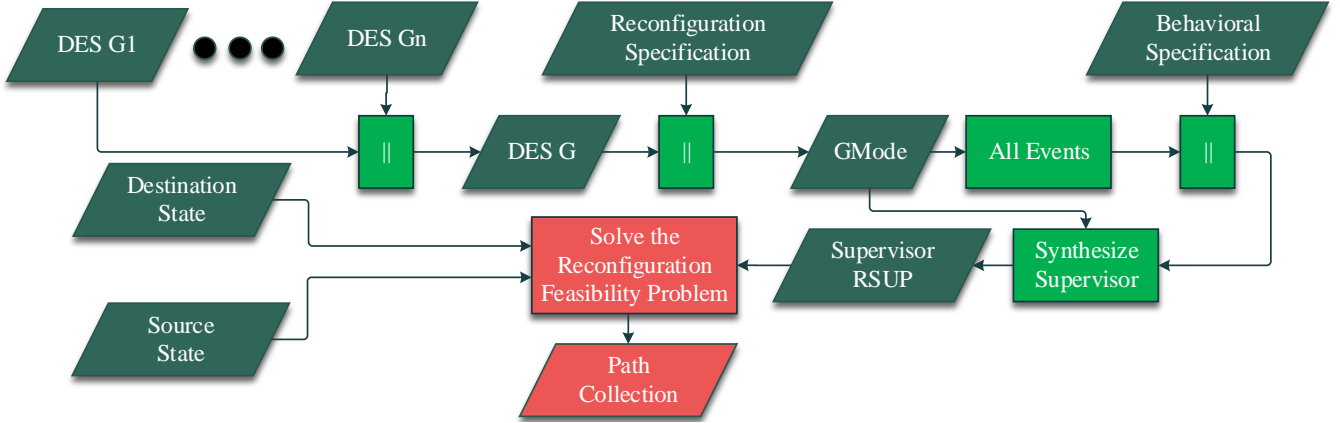


Figure 2: DES reconfiguration process

and

$$L_m(\mathbf{G}) := \{s \in L(\mathbf{G}) \mid \delta(q_0, s) \in Q_m\}$$

Here $\delta(q_0, s)!$ means that $\delta(q_0, s)$ is defined. A supervisory control function for \mathbf{G} is a map $\mathbf{V} : L(\mathbf{G}) \rightarrow \Gamma$, in which $\Gamma = \{\gamma \in Pwr(\Sigma) \mid \gamma \supseteq \Sigma_u\}$ is the set of *control patterns*. ‘ \mathbf{G} under supervision of \mathbf{V} ’ is written as \mathbf{V}/\mathbf{G} .

Given a sublanguage $M \subseteq L_m(\mathbf{G})$ we define the *marked behavior* of \mathbf{V}/\mathbf{G} as $L_m(\mathbf{V}/\mathbf{G}) := L(\mathbf{V}/\mathbf{G}) \cap M$. \mathbf{V} is a *marking nonblocking supervisory control* (MNSC) for the pair (M, \mathbf{G}) if $\overline{L_m(\mathbf{V}/\mathbf{G})} = L(\mathbf{V}/\mathbf{G})$. In practice, \mathbf{V} is implemented by a *supervisor*, which can be taken as a generator **SUP** that represents the maximally permissive controlled behavior $L_m(\mathbf{V}/\mathbf{G})$ subject to a generator specification, say **SPEC**; we denote this computation by $\mathbf{SUP} = \mathbf{supcon}(\mathbf{G}, \mathbf{SPEC})$. For details see, e.g., [14].

3 DES Reconfiguration

3.1 Reconfiguration Specification

A reconfiguration requirement is a transition request to transfer the system from one configuration to another. The set of reconfiguration requirements associated with a DES is represented by the RS. As the first step, the following definition clarifies the notion of configuration (mode).

Definition 1 [Configuration (Mode)]. Let \mathbf{G} be a DES constructed by (synchronous product of) the collection of component sets $C_{\mathbf{G}} = \{C_{\mathbf{G}}^\alpha \mid \alpha \in I\}$, where I is an index set. A *configuration (mode)* of \mathbf{G} is a component set $C_{\mathbf{G}}^0 \subseteq C_{\mathbf{G}}$ such that \mathbf{G}

operates as the corresponding synchronous subproduct, when the elements of C_G^0 and $C_G \setminus C_G^0$ are respectively active and inactive.

The source and destination configurations, corresponding to a reconfiguration task, are connected through a reconfiguration event (RE) which specifies a transition from the former to the latter.

Definition 2 [RE]. Given DES \mathbf{G} with component set C_G , let $C_G^{\mathcal{A}}, C_G^{\mathcal{B}} \subset C_G$ be two configurations of \mathbf{G} , where \mathcal{A} and \mathcal{B} are the component sets which must be deactivated and activated respectively in the course of reconfiguration; then, RE $\sigma_{\mathcal{A},\mathcal{B}}$ must occur to trigger the reconfiguration task. We formalize this task as follows.

Definition 3 [RS]. For a configuration $C_G^{\mathcal{I}}$ of \mathbf{G} , with components $\{\mathbf{G}_a | a \in \mathcal{I}\}$, let $\Sigma_{\mathcal{I}}$ denote the set of exactly the event (labels) appearing in the corresponding components, i.e.

$$\Sigma_{\mathcal{I}} := \bigcup \{\Sigma_a | a \in \mathcal{I}\}$$

For clarity we first consider the case of just two configurations, indexed by \mathcal{A} and \mathcal{B} , and assume that reconfiguration requires switching either from $C_G^{\mathcal{A}}$ to $C_G^{\mathcal{B}}$, with the system \mathbf{G} initially in mode $C_G^{\mathcal{A}}$. As in Definition 2, bring in the corresponding switching events $\sigma_{\mathcal{A},\mathcal{B}}$ and $\sigma_{\mathcal{B},\mathcal{A}}$. We define the RS as the DES

$$E_{\mathcal{R}} := (Q_{\mathcal{R}}, \Sigma_{\mathcal{R}}, \delta_{\mathcal{R}}, q_{0\mathcal{R}}, Q_{m\mathcal{R}})$$

where

- $Q_{\mathcal{R}} := \{q_{\mathcal{A}}, q_{\mathcal{B}}\}$
- $\Sigma_{\mathcal{R}} := \Sigma_{\mathcal{A}} \cup \Sigma_{\mathcal{B}} \dot{\cup} \{\sigma_{\mathcal{A},\mathcal{B}}, \sigma_{\mathcal{B},\mathcal{A}}\}$

Note that $\Sigma_{\mathcal{A}} \cup \Sigma_{\mathcal{B}}$ is disjoint from $\{\sigma_{\mathcal{A},\mathcal{B}}, \sigma_{\mathcal{B},\mathcal{A}}\}$.

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$$\delta_{\mathcal{R}}(q_{\mathcal{A}}, \sigma) := \begin{cases} q_{\mathcal{A}} & \text{if } \sigma \in \Sigma_{\mathcal{A}}, \\ q_{\mathcal{B}} & \text{if } \sigma = \sigma_{\mathcal{A},\mathcal{B}}, \end{cases}$$

$$\delta_{\mathcal{R}}(q_{\mathcal{B}}, \sigma) := \begin{cases} q_{\mathcal{B}} & \text{if } \sigma \in \Sigma_{\mathcal{B}}, \\ q_{\mathcal{A}} & \text{if } \sigma = \sigma_{\mathcal{B},\mathcal{A}}, \end{cases}$$

- $q_{0\mathcal{R}} := q_{\mathcal{A}}$
- $Q_{m\mathcal{R}} := \{q_{\mathcal{A}}, q_{\mathcal{B}}\}$

$E_{\mathcal{R}}$ is depicted in Fig. 1.

It is obvious that, with some notational elaboration, this definition of $E_{\mathcal{R}}$ could be extended to an arbitrary number of distinct configurations and pairwise switchings among them, but we refrain from doing so here.

3.2 Reconfiguring Supervisor Synthesis

In general SCT synchronizes the plant DES \mathbf{G} with its associated behavioral specification prior to synthesizing the supervisor which controls it. To synthesize **RSUP** we provide in this section an extended supervisor synthesis procedure in which the RS is taken into account.

The main idea is to treat the RS on the same footing as any other behavioral specification. The process is illustrated in Fig. 2.

We start by synchronizing all the components associated with \mathbf{G} ; here the operator ‘ \parallel ’ denotes *synchronous product* [19]. Then, \mathbf{G} is synchronized with the RS $E_{\mathcal{R}}$ leading to the multimodal version of \mathbf{G} , say **GMode** as follows.

$$\mathbf{GMode} := (\parallel_{i=1}^n \mathbf{G}_i) \parallel E_{\mathcal{R}}$$

Next, the global system specification is defined by the synchronization of the behavioral specification E with all events of **GMode**. Finally, the reconfiguration supervisor is computed as:

$$\mathbf{RSUP} := \text{supcon}(\mathbf{GMode}, [\text{allevents}(\mathbf{GMode}) \parallel E])$$

where the operator **allevents** returns a marked one-state DES selflooped with all the events of the argument. For details see, e.g., [14].

We emphasize that **RSUP** enforces both the behavioral and reconfiguration requirements of \mathbf{G} .

In the next section we complete the design process by presenting an algorithm to solve the final reconfiguration problem.

4 Reconfiguration Solvability

We construct a backtracking algorithm that collects all forcible paths reaching a suitable target state of **RSUP** from an arbitrary current state. To this end, we first present the formal definition of the reconfiguration problem, then obtain the conditions for backtracking forcibility, and finally propose an algorithm to solve the problem.

4.1 Problem Statement

Especially when it is the intended response to some unexpected failure or emergency, reconfiguration could possibly be commanded from an arbitrary state in **RSUP** of the current (running) configuration. Thus the system must be forced onto a path or set of paths in the **RSUP** state space leading from the current state to one at which the desired reconfiguration event is

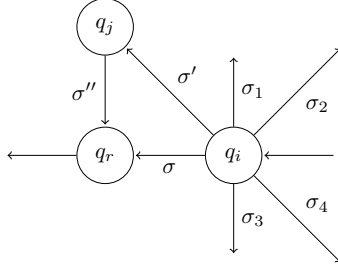


Figure 3: The hypothetical backtracking scenario

defined. The question is then whether or not such a path (set) always exists and can be executed in timely fashion. We thus consider

Problem 1 [Reconfiguration Feasibility]. Denote by q_c the state where **RSUP** currently resides, and let q_r be a state at which a desired reconfiguration event, say σ_r , is defined; namely $\delta_{\mathcal{R}}(q_r, \sigma_r)$! Subject to an appropriate specification of *forcibility*, determine the forcible path (set) from q_c to q_r .

We shall declare a path (set) *forcible* if it can be enforced using the standard SCT “technology” of controllable event disablement, with or without the possible additional use of preemption by a forcible event [14], Sect. 3.8).

The following section describes how to obtain a forcible path (set).

4.2 Backtracking Forcibility

The algorithm is critically governed by the conditions which define forcibility of each backtracking step; if a backtracking step is forcible, then its event is appended to the current path.

We explain the backtracking forcibility conditions (BFCs) by a hypothetical search space as depicted in Fig. 3. We assess the forcibility of the backtracking from q_r to q_i . In other words, we plan to find whether σ contributes to an forcible path (from q_i to q_r) or not.

Let $\Sigma^i = \{\sigma_1, \sigma_2, \sigma_3, \sigma_4, \sigma'\}$ be the set of defined events at q_i , competing with σ to occur. Let also $\Sigma_i = \{\sigma\}$ be the defined events transitioning from q_i to q_r . If any of the following four conditions hold, then backtracking to q_i is permissible, and σ is a solution to this problem:

BFC-1: $\Sigma^i = \emptyset$

There is no event competing with σ to occur at q_i . In other words, σ is the exclusive event which can occur at q_i .

BFC-2: $(\forall \sigma' \in \Sigma^i) \sigma' \in \Sigma_c$

If all of the Σ^i events are controllable, then they can be disabled; therefore, σ can occur at q_i .

BFC-3: $[(\nexists \sigma' \in \Sigma_i) \text{pr}(\sigma', \sigma)] \wedge [(\forall \sigma' \in \Sigma_u^i)(\exists \sigma'' \in \Sigma^i)] \text{pr}(\sigma'', \sigma')$

Σ^i is composed of both controllable and uncontrollable events. The first subformula says no competing event should be able to preempt σ . The second subformula asserts that each uncontrollable event must be preemptable by at least another event. Note that the binary relation $\text{pr}(\sigma', \sigma'')$ holds if the forcible event σ' can preempt σ'' (see, section 3.9 of [14]). Furthermore,

Algorithm 1 Path Collector Algorithm (\mathcal{PCA})

Input:

q_r ▷ Target state
 q_s ▷ Source state
 Q_T ▷ State list
 $\mathcal{P}_{\text{temp}}$ ▷ Temporary list of an incomplete path

Output:

\mathcal{P} ▷ Path collection

```
1: if  $Q_T = \emptyset$  then
2:   return  $\mathcal{P}$  ▷ All instances of  $\mathcal{PCA}$  are terminated.
3: else
4:    $Q \leftarrow \{q \mid \delta(q, \sigma) = q_r\}$ 
5:   for each  $q_i \in Q$  do
6:      $\Sigma_i \leftarrow \{\sigma \mid \delta(q_i, \sigma) = q_r\}$ 
7:      $\Sigma^i \leftarrow \{\sigma \mid \delta(q_i, \sigma) \neq q_r\} - \Sigma_i$ 
8:     if  $q_i = q_s$  then
9:        $\mathcal{P} \leftarrow$  append  $\Sigma_i$  to  $\mathcal{P}_{\text{temp}}$ 
10:       $Q_T \leftarrow Q_T - \{q_i\}$ 
11:     else
12:       for each  $\sigma \in \Sigma_i$  do
13:         if (BFC-1||BFC-2||BFC-3||BFC-4) then
14:            $\mathcal{P}_{\text{temp}} \leftarrow$  append  $\sigma$  to  $\mathcal{P}_{\text{temp}}$ 
15:            $Q_T \leftarrow Q_T - \{q_i\}$ 
16:           return  $\mathcal{PCA}(q_i, q_s, Q_T, \mathcal{P}_{\text{temp}})$ 
17:         end if
18:       end for
19:     end if
20:   end for
21: end if
```

Σ_u^i and Σ_c^i represent the largest uncontrollable and controllable subsets of Σ^i , respectively, where $\Sigma^i = \Sigma_c^i \dot{\cup} \Sigma_u^i$.

BFC-4: $(\exists \sigma' \in \Sigma_u^i)(\forall \sigma'' \in \Sigma_j \cup \Sigma^j) [\delta(q_i, \sigma') = q_j \wedge \sigma'' \in \Sigma_c]$, where Σ_j contains the event(s) transitioning from q_j and to q_r , and Σ^j contains the event(s) transitioning from q_j to the other states.

This condition determines the succession of the uncontrollable events leading to a state containing only controllable events; since the controllable events can be disabled, both σ and $\sigma'\sigma''$ are forcible paths.

We employ the foregoing conditions, as decision-making criteria, to solve the reconfiguration problem by a backtracking algorithm in the next section.

4.3 Reconfiguration Solvability Algorithm

Admissible paths can be collected by the Algorithm 1. The inputs are the target state, from which the backtracking starts; the source state, which is the algorithm's goal to be visited; the state list of the supervisor, which is the search space of the problem including the target and source state; and a temporary list of incomplete paths initialized to empty, in which the potential solutions are stored, corresponding to each instantiation of the algorithm. The output is the collection of the found paths.

The algorithm keeps the track of the visited states and events. If it visits a state that is the destination of more than one event, the algorithm checks inductively the solvability of those branches.

Algorithm 2 Reconfiguration Solvability Algorithm (\mathcal{RSA})

Input: q_r

▷ Target state

 q_s

▷ Source state

 \mathbf{RSUP}

▷ Supervisor

Output:solvability

```
1:  $Q_T \leftarrow Q_{\mathbf{RSUP}} - \{q_r\}$ 
2:  $\mathcal{P} \leftarrow \mathcal{PCA}(q_r, q_s, Q_T, \emptyset)$ 
3: if  $\mathcal{P} \neq \emptyset$  then
4:   return The reconfiguration problem IS solvable by any path of  $\mathcal{P}$ .
5: else
6:   return The reconfiguration problem IS NOT solvable.
7: end if
```

Line 1 defines the terminal case; if all states are checked, then the path collection will be delivered.

Line 4 gathers the states that have transitions to the current target state. The defined events at each found state are stored in two variables: variable Σ_i which contains the event(s) transitioning from the found state q_i to the current state (*Line 6*); and variable Σ^i which stores the event(s) transitioning from q_i to the other states (*Line 7*).

If q_i is the source state (*Line 8*), then a path is found. Hence, the recent found event is attached to the temporary solution, and the result is stored in the path collection (*Line 9*). Moreover, q_i is removed from the global list of unvisited states (*Line 10*). Otherwise, BFCs are checked with respect to the elements of Σ_i and Σ^i (*Line 13*). If any of these conditions holds, then the backtracking from the current state to q_i is authorized, thereby appending σ to the temporary solution variable (*Line 14*). Then, the global variable list is updated by removing q_i (*Line 15*), and a new instantiation of the algorithm is called according to the updated current state (*Line 16*). Note that both Q_T and \mathcal{P} are global variables that can be read and modified by any instantiation of \mathcal{PCA} .

Finally, Algorithm 1 can be incorporated appropriately into the final solvability checker function, i.e., Algorithm 2. First, the state list is initialized to the unvisited states; thus, the target state is initially excluded (*Line 1*). Then, all of the found paths by instantiations of \mathcal{PCA} are gathered (*Line 2*). The fourth argument of \mathcal{PCA} represents the found path that is initially empty. As already asserted, each successful backtracking step appends the found event to its incomplete path. At the end, the decision is made based on the path collection (*Lines 3-7*).

5 Example

We provide an example to illustrate a configuration problem associated with a DES.

Figure 4 depicts SMALL FACTORY (**SF**) with two 3-state machines **M1** and **M2**, and buffers **BUF1** and **BUF2** with three slots and one slot, respectively. Assume that the machines can work with either of the buffers. In other words, **SF** has two modes: $C_{\mathbf{SF}}^1 = \{\mathbf{M1}, \mathbf{M2}, \mathbf{BUF1}\}$, and $C_{\mathbf{SF}}^2 = \{\mathbf{M1}, \mathbf{M2}, \mathbf{BUF2}\}$. Moreover, the events are described in Table 1. Given the required RS as Fig. 5, the synthesized **RSUP** is controllable including 78 states and 270 events.

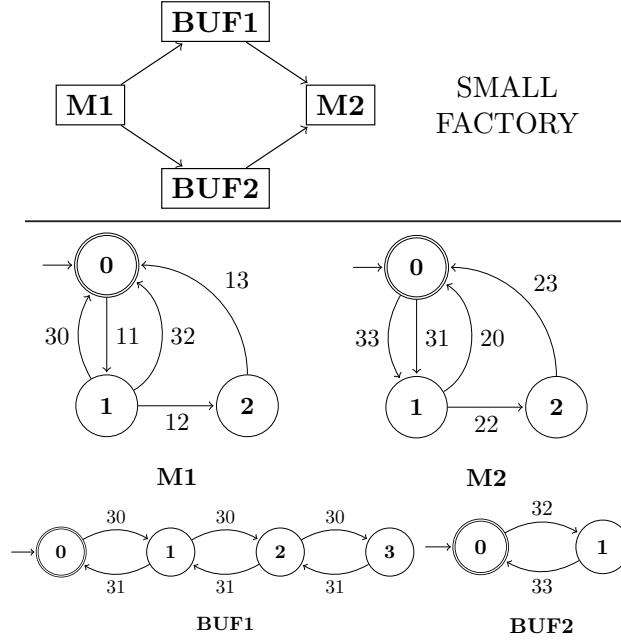


Figure 4: The schematic of SMALL FACTORY

Assume that SF resides currently at $[41]$ ¹ and a reconfiguration is requested to switch from C_{SF}^1 to C_{SF}^2 . Let $[9]$ be the destination state, including $\langle 91 \rangle$ where the reconfiguration event $\langle 91 \rangle$ is defined.

Consequently, $\mathcal{RS}\mathcal{A}$ backtracks from the $[9]$ to $[41]$ to find all forcible paths. The shortest path is $\langle 23, 31, 20, 31, 20, 31 \rangle$, as depicted in Fig. 6. The path computation is analyzed as follows.

- Backtracking $[9]$ to $[5]$: according to BFC-2, backtracking is authorized; because $\langle 11 \rangle$ can be disabled.
- Backtracking $[5]$ to $[19]$: $\langle 11 \rangle$ can be safely disabled, but $\langle 22 \rangle$ may occur sooner than $\langle 20 \rangle$, thereby preempting it according to BFC-3. According to the BFC-4, $\langle 23 \rangle$ can be disabled, so the occurrence of $\langle 22 \rangle$ is handled and blocked by the aforesaid disablement. Therefore, both paths $\langle 20 \rangle$ and $\langle 22, 23 \rangle$ are qualified paths.
- Backtracking $[19]$ to $[12]$: the same as backtracking $[9]$ to $[5]$.
- Backtracking $[12]$ to $[32]$: the same as backtracking $[5]$ to $[19]$.
- Backtracking $[32]$ to $[26]$: according to BFC-1, backtracking is authorized; because there is no event competing with $\langle 31 \rangle$ to occur.
- Backtracking $[26]$ to $[41]$: the same as backtracking $[32]$ to $[26]$, considering $\langle 23 \rangle$ instead of $\langle 31 \rangle$.

The results demonstrate that the reconfiguration problem is solvable, and the supervisor can randomly select any path from the forcible path collection to realize the reconfiguration.

¹In this section, symbols $[q]$ and $\langle \sigma \rangle$ represent state q and event σ , respectively.

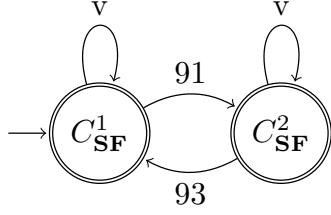


Figure 5: The RS corresponding to SMALL FACTORY (the label v represents the event set $\{11, 12, 13, 20, 22, 23, 30, 31, 32, 33\}$)

Table 1: Descriptions of SMALL FACTORY events

Event	Description
11	M1 takes a workpiece.
20	M2 successfully completes processing a workpiece.
12 / 22	Breakdown occurs in M1 / M2 .
13 / 23	M1 / M2 is repaired.
30 / 32	M1 increments BUF1 / BUF2 .
31 / 33	M2 decrements BUF1 / BUF2 .
91	The reconfiguration $C_G^1 \rightarrow C_G^2$ is requested.
93	The reconfiguration $C_G^2 \rightarrow C_G^1$ is requested.

It is important to note, finally, that at state [9], which serves as source state for the RE ⟨91⟩ the controllable event ⟨11⟩ must be disabled, and ⟨91⟩ must be forced to preempt the uncontrollable events ⟨20, 22⟩. This is acceptable on physical grounds, inasmuch as ⟨11⟩ (**M1** takes a new workpiece) is controllable, and ⟨20, 22⟩ can only occur while **M2** is working, so that preemption can be plausibly assumed to take place in the working time delay interval.

Note that the 2-way RS may result in blocking in case of retaining the possibility of a reconfiguration from C_{SF}^2 back to C_{SF}^1 , since disabling ⟨91⟩ ends up with the disablement of another reconfiguration. We may address two approaches to solving this issue: first, C_{SF}^1 can be considered as the initial state of RS, thereby solving the second reconfiguration problem independently of the first one; alternatively, a 1-way RS can be used for each reconfiguration.

6 Conclusion

This paper proposes a solution to the reconfiguration problem for DES. To this purpose, we first model reconfiguration requirements of the DES by RS. Then, SCT synthesizes **RSUP**, considering the RS. Finally, forcible paths are computed by a dynamic-programming-based algorithm, so it can check the solvability of a user-initiated reconfiguration request. The algorithm in fact backtracks from a desired reconfiguration event source state to the current state in **RSUP**. Guaranteed finite reachability of the source state is confirmed (or otherwise) by the construction of the forcible path set.

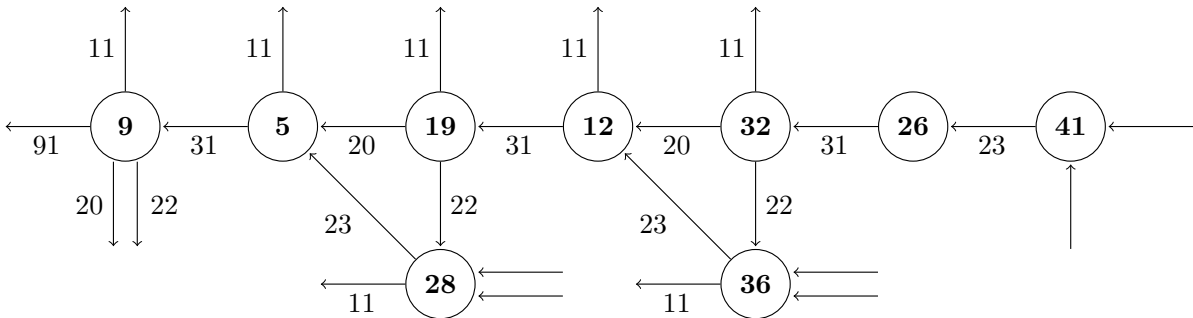


Figure 6: The forcible backtracking goes from [9] back to [41]

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