A Temperature-to-Digital Converter Based on an Optimized Electrothermal Filter

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***Abstract*—This paper describes the design of a CMOS temperature-to-digital converter (TDC). It operates by measuring the temperature-dependent phase shift of an electrothermal filter (ETF). Compared to previous work, this TDC employs an ETF whose layout has been optimized to minimize the thermal phase spread caused by lithographic inaccuracy. To minimize electrical phase spread, the TDC's front-end consists of a wide bandwidth gain-boosted transconductor. The transconductor's output current is then digitized by a phase-domain $\Sigma\Delta$ modulator whose phase-summing node is realized by a chopper demodulator. To minimize the residual offset caused by the demodulator's switching action, the demodulator is located at the virtual ground nodes established by the transconductor's gain-boosting amplifiers. Measurements on 16 samples (within one batch) show that the TDC has an untrimmed inaccuracy of less than $\pm 0.7\,^{\circ}\mathrm{C}$ (3σ) over the military range ($-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$).**

***Index Terms*—Electrothermal filters, phase-domain sigma-delta modulator, synchronous demodulation, temperature sensors.**

I. Introduction

It has been shown [1] that absolute temperature can be accurately determined by measuring the temperature-dependent phase shift of an integrated electrothermal filter (ETF). Using this approach, a temperature-to-digital converter (TDC) with an untrimmed inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ over the military range ($-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$) has been realized [2]. This compares favorably with the inaccuracy of batch-calibrated band-gap temperature sensors [3], [4].

An integrated ETF consists of a heater and a (relative) temperature sensor realized in close proximity on the same silicon substrate. AC power dissipation in the heater causes a time-varying temperature gradient, which the sensor then converts back into electrical AC signals. Since the rate at which heat diffuses through the substrate is finite, the phase of the sensor's output will lag that of the power dissipation in the heater. This phase shift, ϕ_{ETF}, is a function of the filter's geometry and of the temperature-dependent thermal diffusivity of the silicon substrate [5], [6].

Various electrothermal frequency-locked loops have been realized [1], [7], [8], in which an ETF is used as the frequency-determining element. Such loops maintain a constant phase shift in the ETF by driving it at a temperature-dependent frequency. With this approach, an untrimmed inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) over the extended industrial temperature range ($-40\,^{\circ}\mathrm{C}$ to $105\,^{\circ}\mathrm{C}$) has been achieved. In the TDC of [2], however, an ETF was driven at a fixed frequency. The ETF's temperature-dependent phase shift was then digitized by a phase-domain $\Sigma\Delta$ modulator. With this approach, an untrimmed inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) was achieved over the military temperature range.

Since the thermal diffusivity of the substrate is insensitive to process spread [1], [9], [10], the spread in an ETF's thermal phase shift will be mainly determined by lithographic inaccuracy. This can be minimized by optimizing its layout [11] and by making its critical dimensions sufficiently large. Another source of error is the electrical phase shift introduced by the front-end, and, more importantly, its spread. In principle, these can both be minimized by maximizing the front-end's nominal bandwidth. However, this must be done in a power efficient fashion, in order not to incur significant self-heating errors.

In previous work [1], [2], the front-end consisted of a preamplifier followed by a transconductor. The preamplifier consisted of a number of stages, each consisting of a PMOS transconductor with a near minimum-size PMOS diode load. The overall bandwidth of this front-end was about 25 MHz. In this work, a new front-end is described in which a wide-band transconductor replaces the previous multi-stage front-end [12]. While drawing roughly the same amount of current, this transconductor achieves a significantly higher bandwidth (115 MHz). To exploit the expected decrease in electrical phase spread, the new front-end has been combined with an improved ETF, whose layout has been optimized to minimize the effect of lithographic inaccuracy on its thermal phase spread [11].

In Section II, the optimized ETF is described. Section III provides an overview of the implemented TDC. The circuit implementation is described in Section IV, while the measurement results are presented in Section V. The paper ends with conclusions in Section VI.

II. Optimized Electro-Thermal Filter

A simplified layout of the optimized ETF is shown in Fig. 1(a), while its photomicrograph is shown in Fig. 1(b). Like a previous ETF [1], [2], it consists of an n^{+} diffusion heater, which is surrounded by a thermopile made of p^{+} diffusion/Aluminium thermocouples. However, compared to the previous ETF, its layout has been optimized to maximize the SNR at the thermopile's output, while maintaining the same phase-shift (about 90 degrees) at 100 kHz.

For the same power dissipation, reducing the heater area leads to a greater concentration of heat, and, thus, to larger temperature variations in the substrate. For this reason, the optimized

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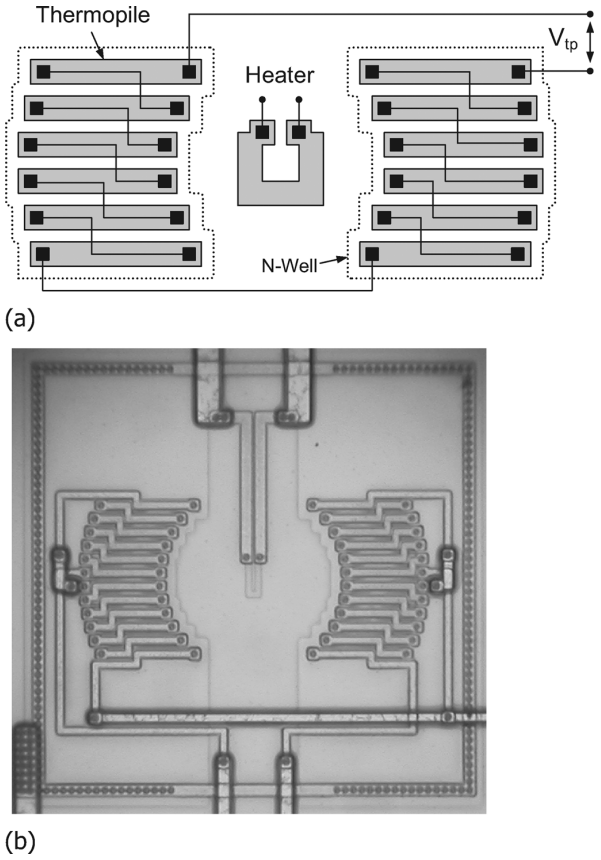

Fig. 1. Simplified layout (a), and photomicrograph (b) of the optimized ETF.

ETF uses a folded heater layout rather than the rectangular layout of the previous ETF. In addition, the thermopile's "hot" junctions are located on a roughly circular, constant phase-shift contour. This maximizes the thermopile's output amplitude, which is proportional to the vector sum of the temperature variations at each of these junctions. Finally, the length of each arm, and hence its thermal noise contribution, was chosen to maximize the SNR at the thermopile's output. Compared to an earlier ETF [1], [2], these considerations allowed the number of thermocouples, and hence the ETF's output signal, to be increased from 20 to 24. In addition, the thermopile resistance was reduced from 36 kΩ to 20 kΩ, leading to a thermal noise reduction from 24 nV/$\sqrt{\text{Hz}}$ to 18 nV/$\sqrt{\text{Hz}}$. For the same heater power dissipation, these changes lead to a 50% increase in the output SNR. Monte Carlo simulations, in which the position of the thermopile junctions is varied randomly [11], show that the optimized ETF exhibits about 20% less phase spread than the previous ETF (Fig. 2). In these simulations, it was assumed that the standard deviation of the inaccuracy in junction position is 70 nm, or 10% of the minimum feature size of the 0.7 μm CMOS process used.

Since each p^+ arm of the ETF's thermopile exhibits a parasitic junction capacitance to the n-well, the ETF also exhibits electrical filtering. The thermopile behaves like a distributed RC filter, with a total resistance of 20 kΩ and a total capacitance of 600 fF. Simulations show that at the intended drive frequency of 85 kHz [2], the resulting electrical phase shift is only 0.14 degrees, which is much smaller than the ETF's thermal phase shift.

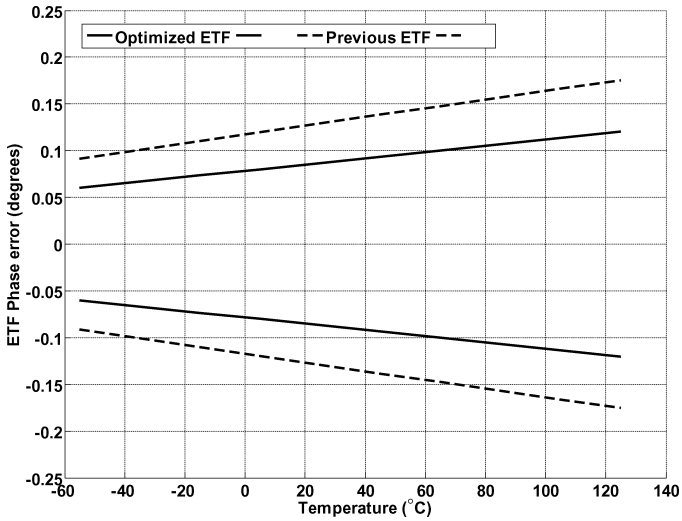

Fig. 2. 3σ boundaries on the thermal phase spread of a previous ETF and an optimized ETF based on Monte Carlo simulations of the effect of lithographic inaccuracy.

However, the electrical phase shift will spread by tens of percent over process corners due to spread in the absolute doping levels of the p^+ arms and the n-well. This spread forms another bound on the absolute accuracy of the ETF's phase response.

III. System Design

A simplified block diagram of an ETF-based TDC is shown in Fig. 3. In it, the ETF is driven by a square-wave, at a constant frequency f_{drive}, while its output, with a temperature-dependent phase-shift ϕ_{ETF}, is applied to a front-end. The output of the front-end is then fed to a phase-domain $\Sigma\Delta$ modulator, which consists of a multiplier, an integrator, a quantizer and a single-bit phase DAC. Depending on the output of the quantizer, the output of the front-end will be multiplied by one of the two digitally phase-shifted versions of f_{drive}, $f_{\mathrm{drive}}(\phi_0)$ and $f_{\mathrm{drive}}(\phi_1)$, generated by the phase DAC. The multiplier acts as the modulator's summing node [13], and outputs a current whose DC component is proportional to the cosine of the phase difference between the output of the front-end and that of the phase DAC. Although the cosine function is only linear for small phase differences around 90 degrees, any residual nonlinearity caused by large phase differences will be the same for all devices, and so will not lead to increased spread. The average of the modulator's bit-stream will then be a weighted average of the two reference phase shifts ϕ_0 and ϕ_1 that approximate ϕ_{ETF}.

A block diagram of the implemented TDC is shown in Fig. 4. As in [2], the ETF is driven at $f_{\mathrm{drive}} = 85$ kHz by a square-wave derived from a crystal oscillator. Its output is then a small (sub-millivolt) AC signal, which is converted into a current by a transconductor $\mathrm{g_m}$, and then digitized by a phase-domain $\Sigma\Delta$ modulator. The modulator's multiplier (Fig. 3) is implemented as a chopper demodulator, embedded in the transconductor, while its integrator is implemented by capacitor C_{int}. This capacitor also filters out the harmonics of f_{drive} present at the output of the demodulator. The voltage across C_{int} is then boosted by a differential-to-single-ended amplifier, and applied to a digital latch (in an off-chip FPGA).

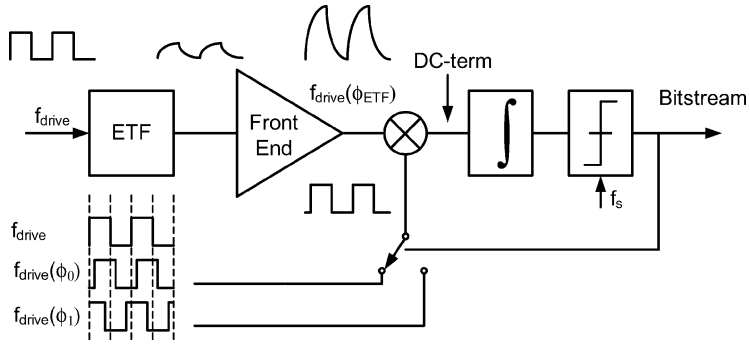

Fig. 3. Simplified block-diagram of an ETF-based TDC.

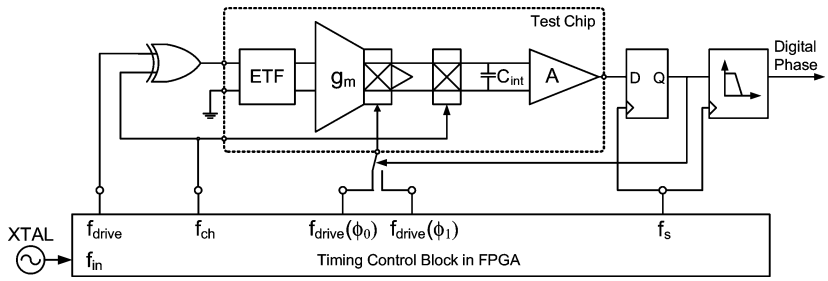

Fig. 4. TDC system block diagram.

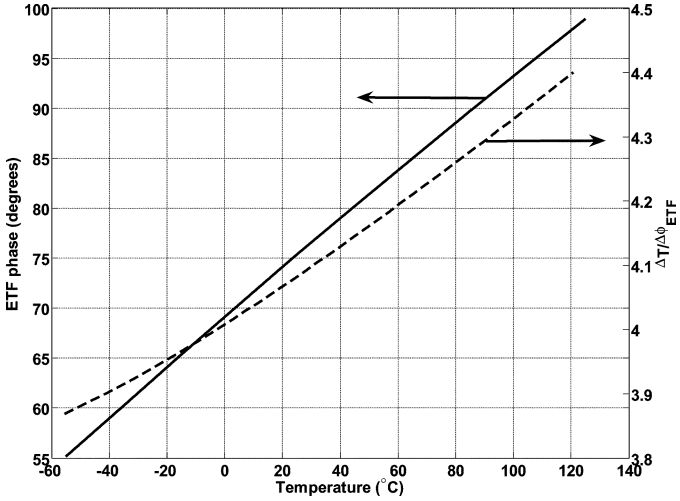

Fig. 5. Simulated phase shift of the optimized ETF (left axis) and the resulting sensitivity function relating small-signal temperature variations to phase variations (right axis).

The latch thus acts as the modulator's quantizer. The FPGA also generates the two phase reference signals, $f_{\rm drive}(\phi_0)$ and $f_{\rm drive}(\phi_1)$ from the output of the crystal-oscillator.

For $f_{\rm drive} = 85$ kHz, Fig. 5 illustrates the simulated phase shift of the optimized ETF over the military temperature range (left axis). The derivative of this function's inverse is also shown. Its maximum value defines a worst-case sensitivity factor $S^T_{\phi_{\rm ETF}}$ that links phase errors to temperature errors.

$$S^T_{\phi_{\rm ETF}} = \frac{\partial T}{\partial \phi_{\rm ETF}} = 4.5 \left[\frac{^\circ{\rm C}}{\rm degrees}\right] \quad (1)$$

$$\Delta T = 4.5 \Delta \phi_{\rm ETF}. \quad (2)$$

This means that thermal phase spread, caused by lithographic inaccuracy (see Fig. 2), will give rise to worst-case temperature measurement errors of 0.8 °C (previous ETF) and 0.6 °C (optimized ETF), respectively. Errors contributed by other sources, such as the electrical phase spread added by the transconductor, g_m, and the residual offset added by the synchronous demodulator, should be made much smaller than this.

Fig. 6(a) shows an idealized block diagram of the TDC's front-end. Since an ETF is a low-pass filter, it will filter out the higher harmonics of the square-wave drive signal, and so its output will be dominated by the filtered first harmonic of the drive signal. The harmonics present at the output of the synchronous demodulator will also be filtered out by the integrator of the phase-domain $\Sigma\Delta$ modulator. To first-order, therefore, the operation of the front-end can be analyzed by modelling both the ETF's drive signal, $V_{\rm drive}$, and the feedback signal of the phase-domain $\Sigma\Delta$ modulator, $V_{\rm FB}$, as sinusoidal functions:

$$V_{\rm drive}(t) = \cos(2\pi f_{\rm drive} t) \quad (3)$$

$$V_{\rm FB}(t) = \cos(2\pi f_{\rm drive} t + \phi_{\rm FB}) \quad (4)$$

where $\phi_{\rm FB}$ toggles between ϕ_0 and ϕ_1 depending on the polarity of the modulator's bit-stream. The ETF's output signal, $V_{\rm ETF}$, will then be a phase-shifted version of $V_{\rm drive}$:

$$V_{\rm ETF}(t) = A \cdot \cos(2\pi f_{\rm drive} t + \phi_{\rm ETF}) \quad (5)$$

where A is the amplitude and $\phi_{\rm ETF}$ is a temperature-dependent phase shift. The amplitude A is a function of the ETF's geometry, the power dissipated in the heater, and the sensitivity of the thermopile. The transconductor g_m converts $V_{\rm ETF}$ into a current $i_{\rm gm}$, which is then multiplied by the feedback signal, $V_{\rm FB}$, leading to a demodulated signal $i_{\rm sig}$:

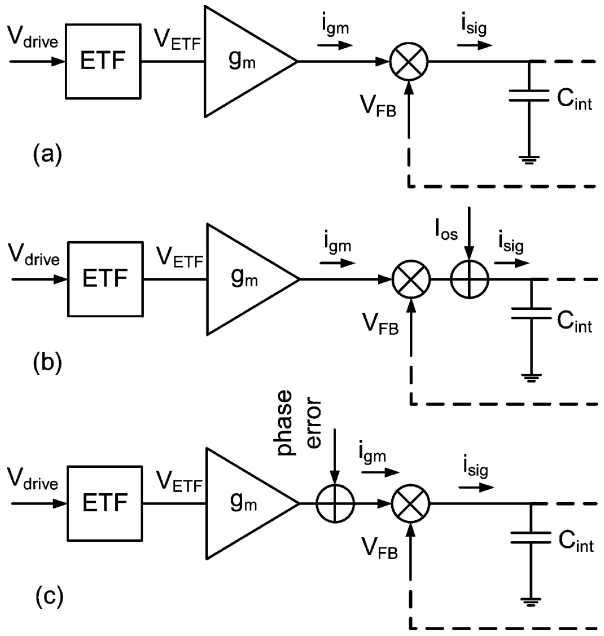

Fig. 6. Simplified block diagram of the interface electronics for an ETF (a), with residual offset (b), and with phase error (c).

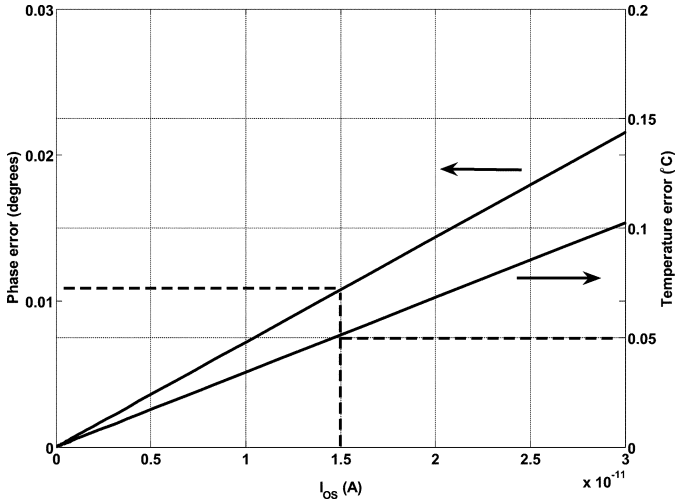

Fig. 7. Simulated phase error and the corresponding temperature measurement error as a function of residual offset current.

$$i_{\mathrm{gm}}(t) = g_{\mathrm{m}} \cdot A \cdot \cos(2\pi f_{\mathrm{drive}} t + \phi_{\mathrm{ETF}}) \tag{6}$$

$$i_{\mathrm{sig}}(t) = i_{\mathrm{gm}} \cdot V_{\mathrm{FB}} = g_{\mathrm{m}} \cdot A \cdot \cos(2\pi f_{\mathrm{drive}} t + \phi_{\mathrm{ETF}}) \cdot \cos(2\pi f_{\mathrm{drive}} t + \phi_{\mathrm{FB}}) \tag{7}$$

The current defined by (7) has AC terms that will be filtered out by C_{int}, as well as a DC term that carries the phase information:

$$i_{\mathrm{sig,DC}}(t) = \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} - \phi_{\mathrm{FB}}). \tag{8}$$

The feedback in the phase-domain $\Sigma\Delta$ modulator (Fig. 3) acts to balance the average charge accumulated by the integrator:

$$\mu \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} - \phi_0) + (1-\mu) \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} - \phi_1) \approx 0 \tag{9}$$

where μ is a number between 0 and 1, which represents ϕ_{ETF} as a weighted average of the two phase references, ϕ_0, and ϕ_1:

$$\mu \approx \frac{\cos(\phi_{\mathrm{ETF}} - \phi_1)}{\cos(\phi_{\mathrm{ETF}} - \phi_1) - \cos(\phi_{\mathrm{ETF}} - \phi_0)}. \tag{10}$$

If $(\phi_{\mathrm{ETF}} - \phi_1)$ and $(\phi_{\mathrm{ETF}} - \phi_0)$ are close to 90 degrees, the cosine function can be linearized, leading to a linear relation between μ and ϕ_{ETF}:

$$\mu \approx \frac{\phi_{\mathrm{ETF}} - (90 + \phi_1)}{\phi_0 - \phi_1}. \tag{11}$$

Non-idealities such as the *residual* offset (Fig. 6(b)) added to the DC signal of (8), or the electrical phase error (Fig. 6(c)) added by the transconductor to the AC signal of (6), lead to errors in the digitized value of ϕ_{ETF}, which via (2), lead to temperature measurement errors.

In the case of a residual offset current, I_{OS}, added to the demodulated DC signal (Fig. 6(b)), the modulator's feedback will still ensure that the average charge accumulated by the integrator is approximately zero. However, a different steady state value μ' results:

$$\mu' \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} - \phi_0) + (1-\mu') \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} - \phi_1) + I_{\mathrm{OS}} \approx 0. \tag{12}$$

The deviation of μ' from the value expected from (9) leads to an error in the digitized value of ϕ_{ETF}. Fig. 7 (left axis) illustrates the simulated phase error as a function of residual offset. The resulting temperature error, calculated from (2), is also shown (right axis). A residual offset current of 15 pA leads to a phase error of approximately 0.01 degrees and a temperature error of 0.05 °C. This simulation has been performed for the optimized ETF at room temperature, $f_{\mathrm{drive}} = 85$ kHz, a heater power of 1 mW, and a transconductance of 300 μS.

The other source of non-ideality is the electrical phase shift added to the transconductor's output current i_{gm}. The source of this phase shift is the finite bandwidth of all the circuitry between the ETF's output and the synchronous demodulator's input (Fig. 6(c)). This phase error ϕ_{error} is indistinguishable from that of the ETF, and directly translates into a temperature measurement error. Adding ϕ_{error} to ϕ_{ETF} in (9), leads to a different steady-state value μ'':

$$\mu'' \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} + \phi_{\mathrm{error}} - \phi_0) + (1-\mu'') \cdot \frac{1}{2} \cdot A \cdot \cos(\phi_{\mathrm{ETF}} + \phi_{\mathrm{error}} - \phi_1) \approx 0. \tag{13}$$

From (13), it can be shown that a phase error of only 0.01 degrees leads to a temperature error of 0.05 °C. Assuming that the ETF is driven at 85 kHz, and that the transconductor behaves like a first order filter, this translates into a -3 dB bandwidth of more than 100 MHz.

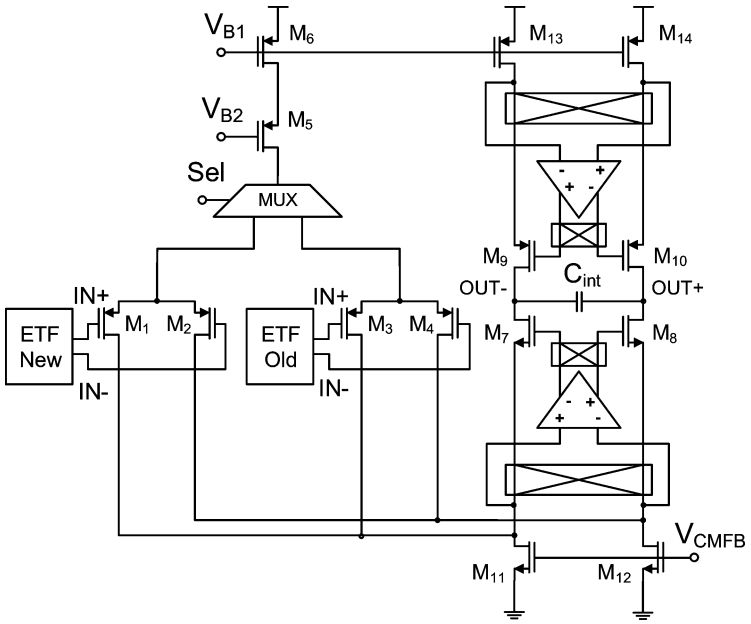

Fig. 8. Gain-boosted transconductor amplifier.

The ETF's phase-shift is a near-linear function of temperature [2], and so achieving a resolution of 0.05 °C (in line with the expected accuracy) over the military temperature range (−55 °C to 125 °C) means that the phase-domain $\Sigma\Delta$ modulator must have a resolution of at least 12-bits. Since the modulator's over-sampling ratio can be made quite large, its resolution will be mainly limited by the leakage of its *passive* (g_m-C) integrator [14], which, in turn, is determined by the finite output impedance of the transconductor. To achieve sufficient resolution, the transconductor's output impedance was increased by the use of gain-boosting. As will be discussed in the following section, the CMOS switches of the demodulator can then be advantageously located at the virtual grounds established by the gain-boosting amplifiers. This significantly reduces the magnitude of the DC offset current at the output of the demodulator, caused by the fact that a net DC current is required to establish a switching waveform across the parasitic capacitances at its input.

As in [2], any residual DC offset current can be eliminated by chopping the ETF and the entire front-end at a frequency $f_{\rm ch}$ (20 Hz), which is much lower than $f_{\rm drive}$ (85 kHz). The bit-stream was decimated by a sinc^1 filter, with a length of $\mathrm{N}/f_{\rm ch}$, where N is an integer, so that its notches perfectly eliminate the ripple caused by the low-frequency chopping. This filter also limits the system's noise bandwidth, thus suppressing most of the wide-band thermal noise produced by the ETF's thermopile.

IV. Circuit Design

As discussed in the previous section, the TDC's transconductor should be designed to have a wide bandwidth. It should have a sufficiently high output impedance, so as to minimize integrator leakage, and maximize the resolution of the phase domain $\Sigma\Delta$ modulator. The noise contribution of the transconductor should be kept below that of the ETF. Finally, the residual offset current produced by the synchronous demodulator should be minimized. To satisfy these requirements, the transconductor was implemented as a gain-boosted folded-cascode amplifier, with a PMOS input pair, and an embedded chopper demodulator (Fig. 8). In order to compare the performance of the ETF used in [2] with that of the optimized ETF, the transconductor employs two PMOS input pairs (M_{1-4}) connected in parallel. By multiplexing the tail current (60 μA) provided by the cascoded current source (M_{5-6}), any one of the two ETFs can be selected for use in the TDC. Transistors M_{7-8} cascode the current sources M_{11-12} (each carrying 40 μA), while M_{13-14} (each carrying 10 μA) are cascoded by means of M_{9-10}. The offset current of the PMOS current sources (M_{13-14}) is chopped by means of the upper chopper.

Any electrical phase shift introduced between the input pair of the transconductor and the input of the synchronous demodulator will give rise to a temperature error, see (13). As discussed in Section II, the thermopile behaves like a distributed RC filter with a phase-shift of 0.14 degrees at 85 kHz. To avoid increasing this phase-shift significantly, the transconductor's input capacitance (Fig. 9), $C_{\rm par,gm}$, was designed to be small (50 fF) compared to the thermopile's total capacitance (600 fF), by making the input devices relatively small (36 μm/0.7 μm). The voltage across the input devices gives rise to a differential AC current $i_{\rm sig,AC}$, which is then phase detected by the embedded chopper demodulator. Over temperature and process corners, simulations show that the minimum unity-gain BW of the corresponding transconductance is greater than 115 MHz. At $f_{\rm drive} = 85$ kHz, this translates into a nominal phase shift of 0.01 degrees in the AC current entering the synchronous demodulator, which is much smaller than the 0.14 degrees of electrical phase shift introduced by the ETF itself (Section II). Although the total phase shift translates into a temperature-sensing inaccuracy of about 0.6 °C, it should be noted that the phase spread within a batch will be an order of magnitude smaller. Compared to the use of a preamp in [1],

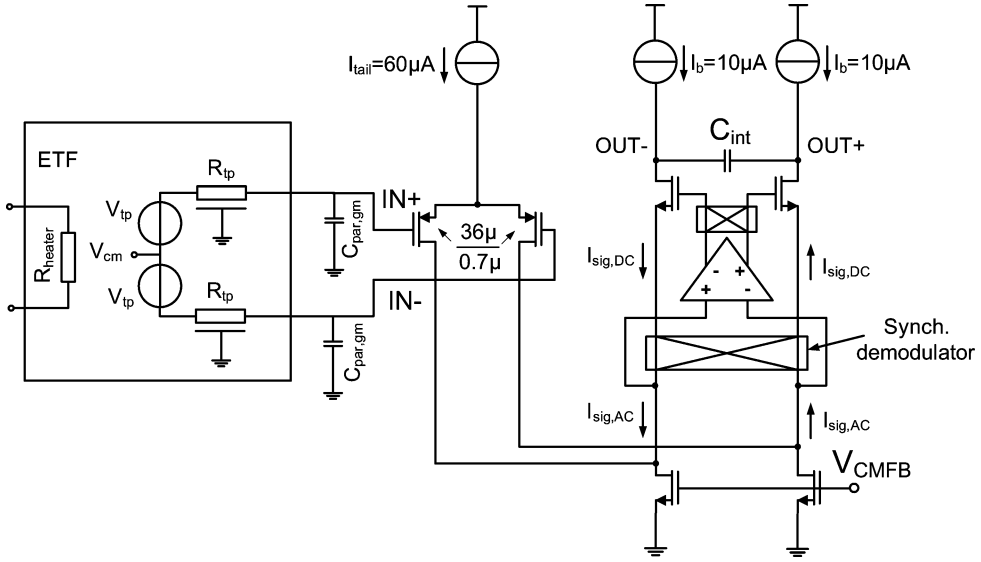

Fig. 9. Electrical filtering due to the thermopile's parasitic capacitance, and due to the input pair's parasitic capacitance.

[2], the use of a single transconductor provides a significantly wider bandwidth for the AC current entering the demodulator −115 MHz versus 25 MHz.

In a $\Sigma\Delta$ modulator based on a passive (g_m-C) integrator, the integrator leakage p, is determined by the DC output impedance of the transconductor R_{out}, the integrating capacitor C_{int}, and the sampling frequency f_S:

$$p = e^{-1/f_S R_{out} C_{int}}. \tag{14}$$

The width of the widest dead band Δx, in the modulator's DC characteristic normalized to its reference is given by [14]:

$$\Delta x = \frac{1-p}{1+p}. \tag{15}$$

The amplifier's simulated DC gain is greater than 140 dB, which corresponds to a DC output impedance of more than 33 GΩ. With $C_{int} = 70$ pF, and a 2.67 kHz sampling frequency, this means that the dead bands associated with integrator leakage will be no wider than 0.004 degrees in terms of ETF phase. Via (2), this translates into a temperature measurement inaccuracy of less than 0.02 °C.

Simulations show that the transconductor has an input-referred thermal noise floor of 12.7 nV/$\sqrt{\text{Hz}}$ (the ETF's noise level is at 18 nV/$\sqrt{\text{Hz}}$) and a $1/f$ noise corner of 50 kHz. Operating the chopper demodulator at 85 kHz ensures that most of the $1/f$ noise is modulated away from DC.

Any offset current added to the current integrated by C_{int} will give rise to a temperature error, see (12). The chopper demodulator itself is a major contributor of such offset. This issue can be analyzed by considering the main branch of a classical PMOS-input folded-cascode amplifier shown in Fig. 10 (input pair not shown). Current sources I_1 and I_2, carrying a current I_b, represent the upper PMOS current sources, and the chopper demodulator is located at the sources of the cascode transistors M_{1-2} [15], [16]. In the presence of an offset V_{OS} between the NMOS cascode transistors, a net DC voltage V_S is established at the sources of the cascode transistors and across the chopper. The transient waveforms of the signals in the circuit of Fig. 10 are shown in Fig. 11. Due to the action of the chopper, a square-wave voltage V_d appears across the folding nodes of the amplifier. On the one hand, V_d charges and discharges the parasitic capacitors C_{par}, leading to an AC current I_{p1}-I_{p2} [17], while on the other hand, it modulates the output currents of the bottom NMOS current sources, M_{3-4} (with finite output impedances R_{out3-4}), leading to another AC current I_{d3}-I_{d4}. The sum of these two currents is an AC current, I_{CH1}-I_{CH2}, which is rectified by the chopper itself into an output current I_{S1}-I_{S2}. At a chopping frequency f_{ch}, the DC value of this current I_{OS} is:

$$I_{OS} = 4 \cdot f_{ch} \cdot C_{par} \cdot |v_d| + \frac{2 \cdot |v_d|}{R_{out3-4}}. \tag{16}$$

To minimize I_{OS}, the parasitic capacitances at the high-impedance input nodes of the chopper demodulator should be shielded from the DC voltage across its outputs. As shown in Fig. 12, a suitable location for the chopper is between the source terminals of the cascode transistors and the input terminals of the booster amplifiers. This way, the booster amplifiers [18], [19] will establish a virtual ground at the high-impedance, high-capacitance, folding nodes of the main amplifier. Therefore, the amplitude of the square-wave voltage V_d is reduced by the gain of the booster amplifier, and the amplitude of the offset current I_{OS}, as well. The output of the boosters must then also be chopped in order to maintain the correct feedback polarity. This technique has two advantages. Firstly, fixing the chopper's input nodes at virtual ground reduces the magnitude of I_{OS} by three orders of magnitude (from simulations), compared to the situation of non gain-boosted transconductor of Fig. 10. Secondly, chopping the booster's output means that the contribution of its offset (and $1/f$ noise) to the amplifier's output current is also chopped. Simulations show that, for a 10 mV worst-case offset between the cascode transistors and a 10% mismatch between the chopper switches, I_{OS} is about 150 pA. This is then cancelled (Fig. 4) by chopping

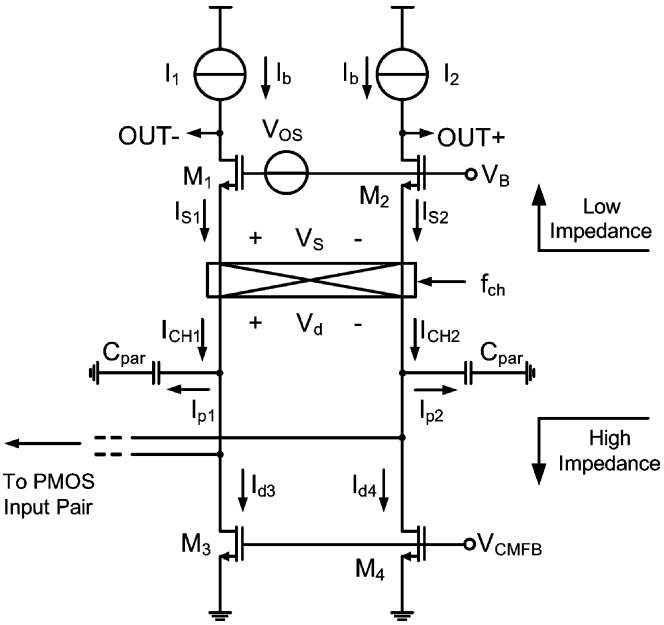

Fig. 10. Main branch of a folded-cascode amplifier with embedded chopper demodulator.

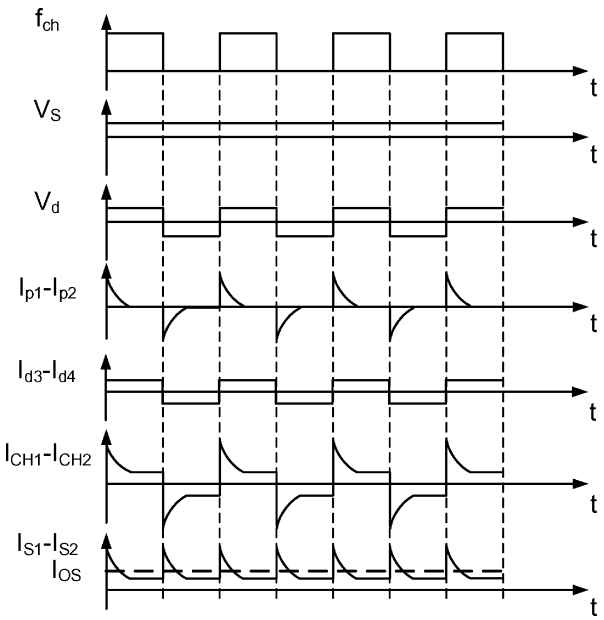

Fig. 11. Transient wave-forms of the circuit in Fig. 10.

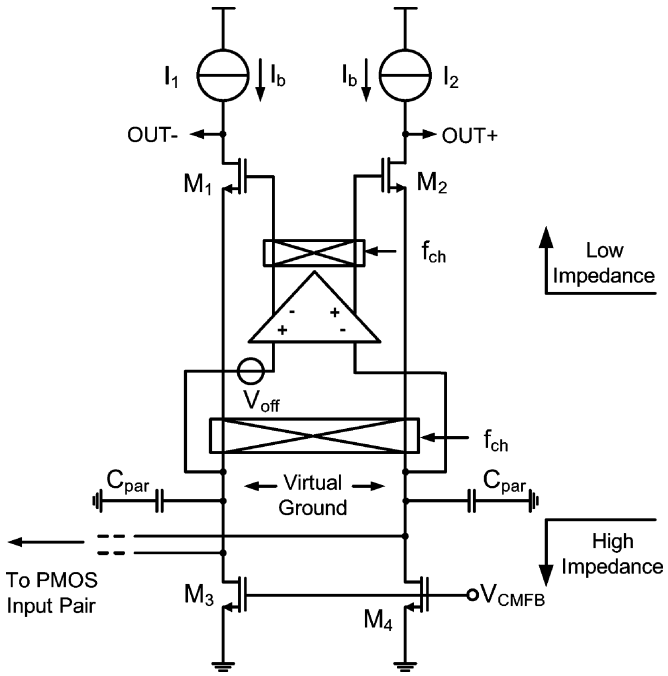

Fig. 12. Modified circuit that turns the capacitive folding nodes into virtual grounds.

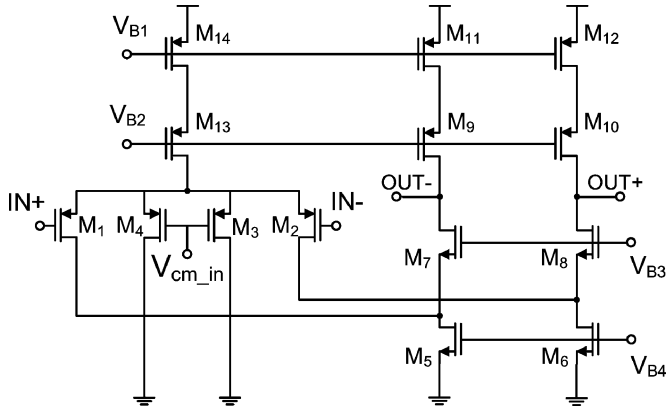

Fig. 13. The booster amplifier for the NMOS cascode transistors with input common mode regulation.

the entire front-end (including the ETF) at a lower frequency $f_{\rm ch}$ [3].

The requirements on the DC output impedance of the transconductor (to limit the dead bands) mean that the booster amplifiers have to have a DC gain in excess of 60 dB. To obtain this, as well as the highest possible common mode rejection ratio, they were implemented as fully differential folded-cascode amplifiers. Fig. 13 illustrates the booster amplifier of the NMOS cascode devices of the main amplifier (Fig. 8). A similar topology is used for the booster amplifier of the PMOS cascode devices. Input common-mode regulation is used to set the common-mode level of the booster's input terminals [20]. The input pair ($\rm M_1$ and $\rm M_2$) is provided with two extra transistors ($\rm M_3$ and $\rm M_4$) in a common-source configuration, whose gates are connected to the input common mode reference, $V_{\rm cm\_in}$. Due to the feedback between the input and output of the booster amplifier via the main cascode transistors, the output common-mode voltage is regulated in such a way that the input common-mode voltage is equal to $V_{\rm cm\_in}$. To enhance stability, load capacitors of 0.9 pF (not shown) were added to the output terminals of the booster amplifiers [18]. The booster amplifiers each consume 30 μA from the 5 V supply, or about 25% of the transconductor's power consumption.

Since the signal swing across $C_{\rm int}$ is too small to drive an off-chip latch, it is buffered by a differential-to-single-ended amplifier (Fig. 4). The amplifier has a gain of 40 dB and a rail-to-rail output. As in [1], heater drive inversion (HDI) is used to minimize the effect of capacitive cross talk in the ETF.

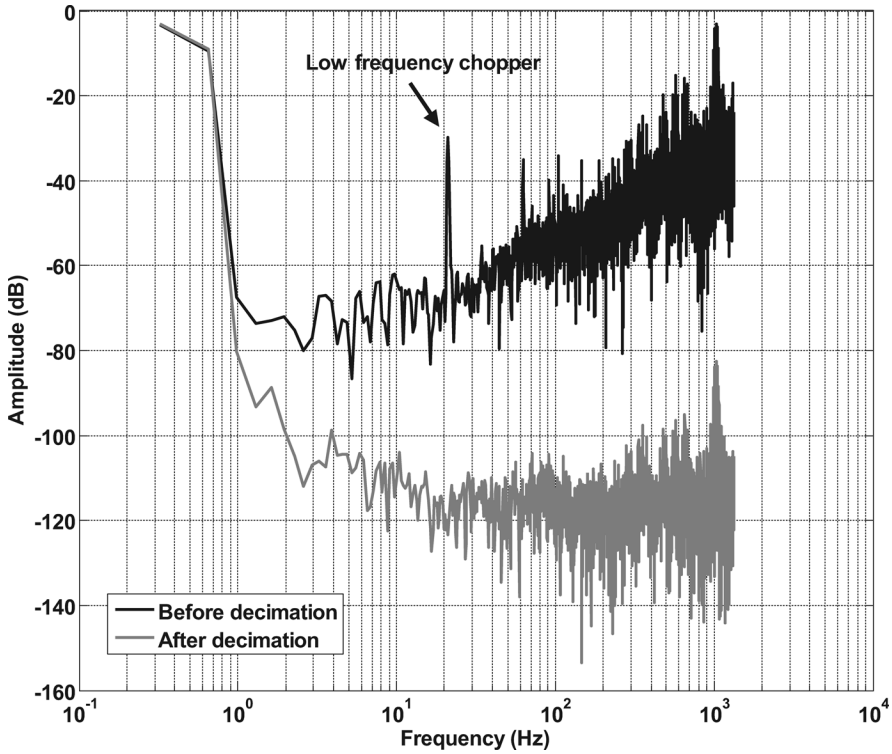

Fig. 15. The measured output spectrum of the TDC at room temperature before and after decimation (8192-point FFT, Hanning window).

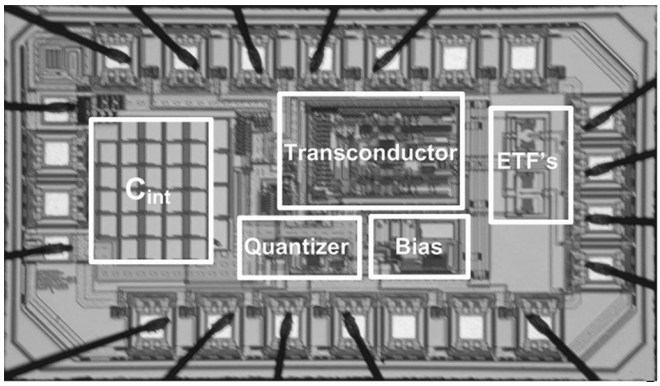

Fig. 14. Chip photomicrograph.

V. Measurement Results

The optimized ETF, the ETF of [1] and [2], and the TDC's analog front-end were realized in a standard 0.7 μm CMOS technology. The chip has an area of 2.3 mm^2 (Fig. 14) and was packaged in a ceramic package. The selected ETF and the temperature-to-digital converter each consume 2.5 mW from a 5 V supply. The timing signals were generated in an FPGA and derived from a 16 MHz crystal oscillator. The ETF was driven at a frequency of 85 kHz, and the difference between the two reference phases ϕ_0 and ϕ_1, was chosen to be 90 degrees ($\pm$45 degrees), which is large enough to cover the expected variation in the ETF's phase shift over the military temperature range. The sampling rate of the phase-domain $\Sigma\Delta$ modulator was 2.67 kHz, and the low frequency chopper was driven at 20 Hz. The modulator's output was decimated by a 14-bit counter, which acts as a 1st-order sinc filter and limits the system bandwidth to 0.16 Hz. A sinc^1 filter was chosen over a more complex sinc^2 filter, because the former actually achieves slightly more resolution. This is because the modulator's resolution is mainly limited by the ETF's thermal noise, which, for the same filter length, is more effectively suppressed by the narrower noise bandwidth of a sinc^1 filter. Fig. 15 shows the output spectrum of the phase domain $\Sigma\Delta$ modulator at room temperature before and after decimation. The tone at 20 Hz is due to use of the low-frequency chopping (Fig. 4), and is completely suppressed by the decimation filter. The variance of the measured noise in the decimated bit-stream was 0.006 degrees (rms), which corresponds to a temperature-sensing resolution of 0.03 °C (rms).

To measure the accuracy of the TDCs, they were mounted in good thermal contact with a large aluminium block, and their temperature was then measured by a PT-100 temperature sensor. The implementation of an on-chip multiplexer (Section IV), meant that TDCs based on both the previous and the optimized ETF could be characterized. The averages of the measured phase-versus-temperature characteristics of 16 devices are shown in Fig. 16, as well as the simulated characteristics. These characteristics were obtained by inverting (10) and then performing an 8th order least-squares polynomial fit on the measured data, i.e., the output of the PT-100 sensor and the decimated output of the chips. Due to their different geometries, the slope of their phase characteristics is significantly different. However, as intended [11], the characteristics intersect at a phase-shift of about 90 degrees. From these results, the maximum value of the sensitivity function $S^T_{\phi_{\mathrm{ETF}}}$ of the old ETF is 4.7 °C/degrees, while that of the optimized

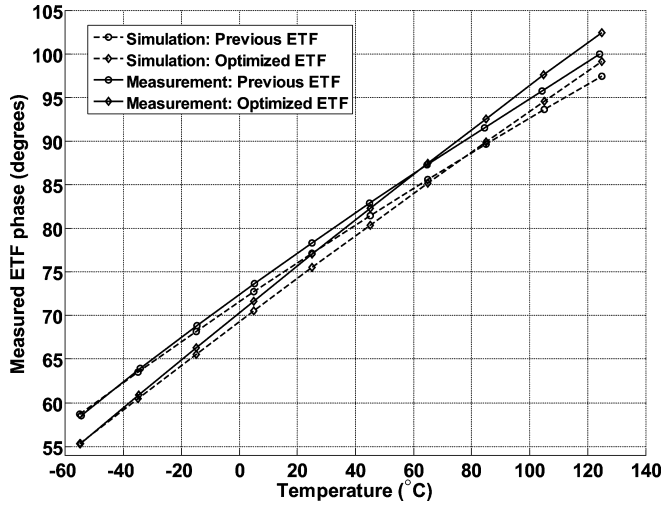

Fig. 16. Measured and simulated phase characteristics of TDCs based on both ETFs.

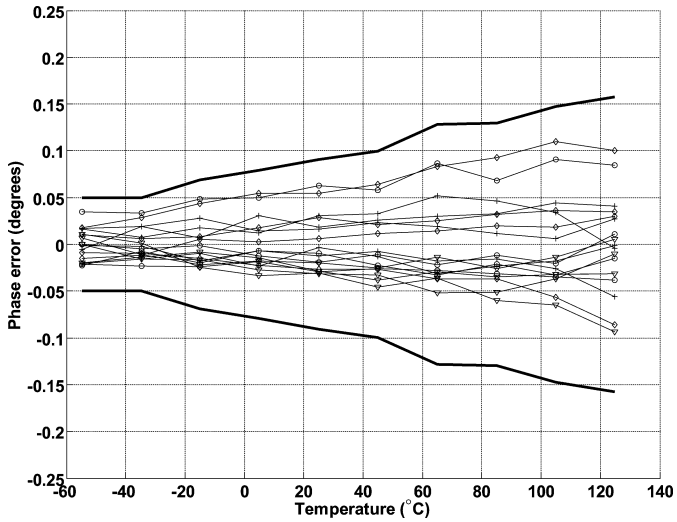

Fig. 17. The measured deviation of each TDC's phase (using the optimized ETF) from the average phase-temperature characteristic (bold line: 3σ error).

ETF is 4.1 °C/degrees. The latter is slightly smaller than the simulated value presented in (2).

The average characteristics were then used to translate the decimated output of *each* TDC into an absolute temperature value. For the optimized ETF, the phase deviation from the average characteristic is shown in Fig. 17 (16 devices). The corresponding temperature deviation is shown in Fig. 18. Due to an error in the fitting process, the temperature deviation is somewhat worse than that reported in [12]. It can be seen that a TDC based on the optimized ETF achieves an untrimmed inaccuracy of about $\pm 0.7\,^{\circ}\mathrm{C}$ (3σ) over the military range ($-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$), while a TDC based on the previous ETF only achieves an inaccuracy of $\pm 0.8\,^{\circ}\mathrm{C}$ (3σ). These results are in line with the predicted 20% reduction in the sensitivity of the optimized ETF's phase response to lithographic inaccuracy.

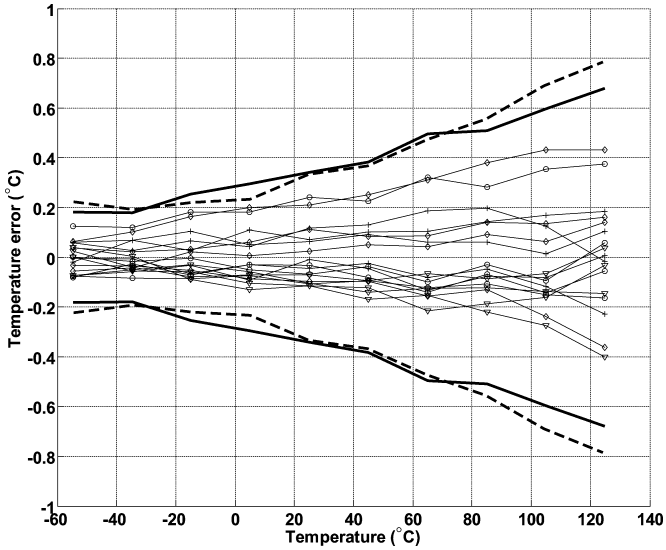

Fig. 18. Measured temperature deviation of each TDC's output (bold line: 3σ error for TDC's based on the optimized ETF, dotted line: 3σ error for TDC's based on the previous ETF).

VI. Conclusion

A CMOS temperature-to-digital converter (TDC) based on thermal diffusivity sensing has been implemented. It consists of a phase-domain $\Sigma\Delta$ modulator, which measures the temperature-dependent phase shift of an electrothermal filter (ETF). By optimizing the layout of the filter, the sensitivity of its phase response to lithographic errors was decreased by 20% and its SNR was increased by 50%. To minimize the phase error introduced by the interface electronics, a wide-band, gain-boosted, single-stage transconductor was used instead of the multi-stage pre-amplifiers used in previous work. In addition, the residual offset current introduced by the chopper demodulator of the phase-domain $\Sigma\Delta$ modulator was minimized by locating it at virtual ground nodes. Using these techniques, an untrimmed temperature-sensing inaccuracy of $\pm 0.7\,^{\circ}\mathrm{C}$ (3σ) over the military range ($-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$) was achieved (16 samples).

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