A Single Phase Latch for High Speed GaAs Domino Circuits

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Abstract

A Single Phase Latch (SPL) suitable for GaAs domino logic gates and compatible with DCFL is presented. Two versions of the SPL are reported in this work: Single Ended SPL used in pure domino logic and Differential SPL used in dynamic Cascode Voltage Switch Logic. SPL is compared with other common GaAs dynamic circuits and latches. The results demonstrate that SPL is superior in terms of device count, area, clock rate and power consumption.

1. Single Phase Latch (SPL) Design

Pipelining dynamic logic circuits provides full use of the clock period. In typical dynamic design [1], one half of the clock cycle is used for a precharging and the other half for the logic evaluation, so that when parts of the circuit evaluate the other parts precharge and vice–versa.

Circuit diagrams for a Singled Ended and Differential SPL are shown in Figure 1(a) and (b). They were designed for implementation in a 0.6 μm E/D process (H–GaAsIII) from Vitesse.

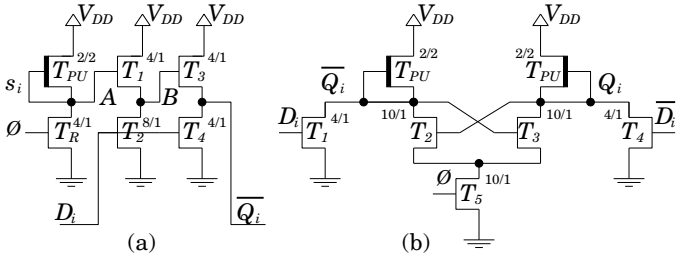

Figure 1. (a) Single Ended and (b) Differential Latches. Device dimensions are in μm.

2. Performance Comparison

Table 1 compares the performance of SPL in relation to the best performance reported dynamic latch for high speed GaAs domino circuits and static latch work. As can be observed SPL has the best performance in terms of operation frequency, chip area, device count and power dissipation.

Differential SPL provides an alternative to latch CVSL reducing the number of devices with less power consumption and operation frequency, and a marginal degradation in performance is illustrated.

3. Acknowledgement

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References

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[2] Vitesse Semiconductor Corporation, "ASIC Designer's Reference Library", FX/VIPER Gate Array Macrocell Libraries, April 1996.

[3] K. R. Nary and S. I. Long, "Dynamic Latch for High Speed GaAs Domino Circuits", *IEE Electronics Letters*, vol. 28, no. 1, pp. 36–37, January 1992.

Table 1. D-Latches Comparisons

Latch→ Perf.↓	DCFL [2]	Dynamic [3]	SPL Single	SPL Diff.
μm^2	4500	2508	1070	1605
Devices	12	8	6	7
MHz	750	350	2000	833
mW	2.38	0.8	0.69	0.46
$\frac{\mu m^2 \times mW}{MHz}$	14.28	5.73	0.36	0.88