Modelling of Multilevel Converters

Thierry Meynard, Maurice Fadel, Noureddine Aouda

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***Abstract*— In this paper, the imbricated cells multilevel converters are studied and modeled from a control view point. These converters make use of several switches connected in a series, which allows using switches with reduced voltage ratings; these low voltage switches have lower conduction losses and can switch at higher frequency. In addition to this feature common to all converters using series connected switches, the control signals of multilevel converters can be phase shifted to increase the apparent switching frequency and improve the dynamic performances of the whole converter. It will be shown that a multilevel inverter leg, composed of p pairs of switches and $p-1$ capacitors, forms a multivariable nonlinear system that cannot be properly modeled by standard methods such as state-space averaging. The transient behavior of this system depends on the current harmonics and their phase shift with the different control signals. A specific model will be detailed, studied, and used to illustrate the properties of these converters. In particular, the natural balancing of the voltage across the switches will be demonstrated and the time constants involved in this process will be determined.**

***Index Terms*—Converters, harmonic analysis, modeling, multilevel systems, power electronics, state-space methods, steady-state stability.**

I. Introduction

GENERALLY speaking, the modeling of static converters for control design purposes is difficult because these systems involve continuous elements (inductors, capacitors) as well as discrete elements (switches). The operation of the converter is a periodic sequencing of different modes of operation corresponding to different topologies. These remarks imply that two types of model can be developed—continuous or discrete.

Models of the first type can be easily obtained when the varying quantities can be assimilated to their average value over a switching period. This is generally true for PWM converters involving filters such that current and voltage ripples are small. This approach leads to different types of models (equivalent average circuit, state-space averaging, etc.) [1].

Models of the second type do not require any assumption, but the model is generally complex and its use for control design is often troublesome. Though tedious, the linearization around a point of operation is generally quite efficient [2], [3].

Obtaining a model can also be the result of an harmonic analysis at the first order of the state variables, which leads to a continuous first harmonic model [4].

Manuscript received July 3, 1995; revised January 13, 1997.

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Publisher Item Identifier S 0278-0046(97)04135-X.

In the case of the converters studied in this paper, it can be shown that the derivative of the dc component of the state variables does not directly depend on the dc component. This derivative depends on the harmonics in the converter. Nevertheless, these harmonics are imposed by the dc components of the state variables. So, a dc model describing the relation between the state variables and their derivative can be found, but it must be derived from the study of the harmonic equivalent circuit. From this standpoint, the model described in this paper does not belong to any of the three types of model listed here (above).

Using static converters at ever-increasing power levels gave rise to new topologies among which are the imbricated cells multilevel converters, which allow increasing the commutated voltage as well as the apparent frequency. Designing the control circuits of these converters requires a modeling process that is, in this case, tightly linked to the converter topology. A special characteristic of these converters is that the capacitor voltage variations are imposed by the load current harmonics rather than by the average load current, although the harmonics are generally much less than the average value. It will be shown that these harmonics guarantee automatic voltage balancing across the semiconductors, which is the most important problem in the field of high-voltage power conversion. For these reasons, models based on average values cannot be used for these converters, and it is very important to develop a model accounting for the harmonics.

This can be achieved by choosing a mode of operation of the converter, replacing blocking switches with voltage sources including the harmonics of the voltage across the switch, and conducting switches with current sources, including the harmonics of the current through the switch.

II. Imbricated Cells Multilevel Converters

The topology of a multilevel converter is given in Fig. 1. In this section, the current ripple in current source I and the voltage ripples in voltage source E, and in every floating capacitor C_k, are neglected to derive, very simply, most of the properties of the system. However, it will be shown further on, that this assumption would lead to a wrong conclusion concerning the variation of the capacitor voltages. We will see that even when the harmonics are very small compared with the dc component, they are the ones to rule the evolution of the capacitor voltages.

A. Topology and Basic Operation

Multilevel converters use several floating voltage sources and imbricated commutation cells to reach high voltage and improve the waveform of the chopped voltage. Choppers,

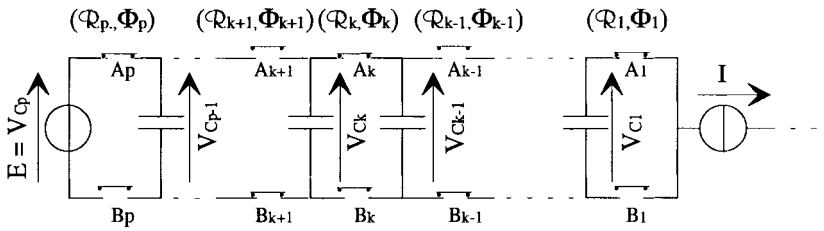


Fig. 1. Multilevel commutation cell.

voltage-source or current-source inverters, and cycloconverters with any number of switches connected in series can be implemented.

The switches are arranged in pairs (A_k, B_k) that operate like the two switches of a standard commutation cell:

- they must never conduct simultaneously because it would short-circuit voltage sources V_{Ck-1} and V_{Ck};
- they must never be blocking at the same time because current source I would be open-circuited;
- if both switches are controlled, dead times must be provided to compensate for turn-off delays;
- the switches reversibility for voltage and current must comply with the reversibility of the voltage and current sources;
- $\cdots$.

In fact, this multilevel commutation cell can be considered as a generalization of the conventional commutation cell which is obtained in the particular case when $p = 1$.

B. Voltage Across the Blocking Switches

The major advantage of this structure is that the floating capacitors $V_{C1}, \cdots, V_{Cp-1}$ allow mastering the voltage distribution across the blocking switches. The voltage applied across the blocking switch of any cell is imposed by the voltage sources V_{Ck} and V_{Ck-1} (Fig. 2)

$$(V_{Ak})_{\text{off}} = (V_{Bk})_{\text{off}} = V_{Ck} - V_{Ck-1}, \quad k = 1, \cdots, p \quad \text{and} \quad V_{C0} = 0, V_{Cp} = E. \tag{1}$$

The quantity $V_{Ck} - V_{Ck-1}$ will be referred to as cell voltage of cell k.

The sum of the instantaneous voltage across the switches is equal to the voltage E, and there is always half of the switches in the conduction mode; consequently, the voltage balance across the blocking switches is given by

$$(V_{Ak})_{\text{off}} = (V_{Bk})_{\text{off}} = E/p, \qquad k = 1, \cdots, p \tag{2}$$

which yields, by trivial recurrence

$$V_{Ck} = k \cdot E/p, \qquad k = 0, \cdots, p. \tag{3}$$

Practical experiments showed that this voltage balance is obtained when the duty cycles of the different commutation cells are equal and the phase shift is $2\pi/p$.

C. Current Through the Conducting Switches

The instantaneous current in each switch is equal to the current in the current source when the switch is conducting and zero when the switch is blocking. So, if the current source can be taken as constant over a switching period, the average current in a switch is given by

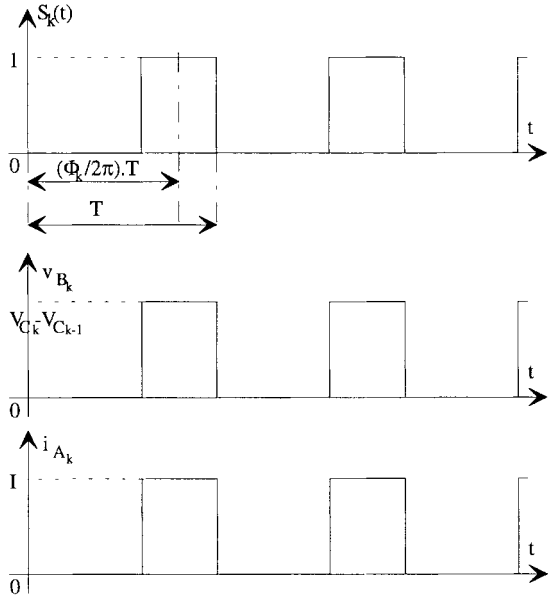


Fig. 2. Control and ideal current and voltage waveforms.

$$I_{k\text{avg}} = \mathcal{R}_k \cdot I. \tag{4}$$

This implies that the average current in each floating capacitor is

$$I_{C_{k\text{avg}}} = (\mathcal{R}_{k+1} - \mathcal{R}_k) \cdot I, \qquad k = 1, \cdots, p-1. \tag{5}$$

Consequently, imposing equal duty cycles to all cells is sufficient to cancel the average current in these capacitors and keep their voltages stable.

D. Chopped Voltage Waveform

The chopped voltage applied to current source I can be expressed as the sum of the voltage across the switches of the lower branch. All these voltages are square voltage waves with the same duty cycle $\mathcal{R}$. However, the phase shift between the control signals of the different cells can be chosen freely. It can be shown that choosing control signals phase shifted by $2\pi/p$ is optimum in that it allows cancelling harmonics centered at $F_{sw}, 2 \cdot F_{sw}, \cdots, (p-1) \cdot F_{sw}$, these last harmonics being the same as in a standard "two-level" commutation cell [6].

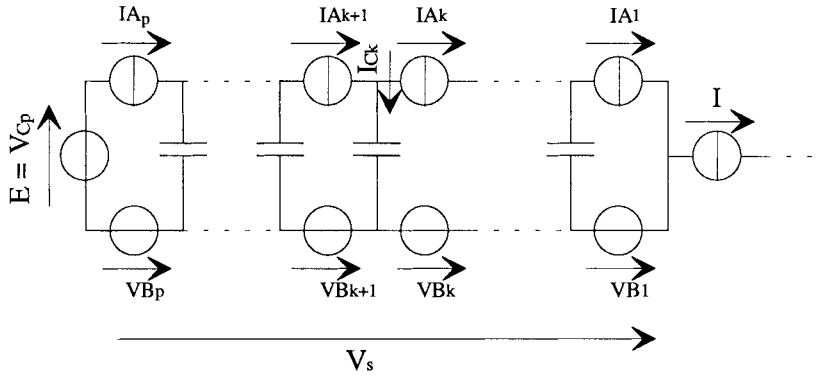


Fig. 3. Equivalent circuit.

III. Stability of the Voltage Distribution

A. Scope of the Problem

The safety of operation of a multilevel converter may depend on the voltage distribution. For this reason, it is very important to check the stability of this voltage distribution, i.e., determine whether the system is capable of compensating for small (or even large?) perturbations around the balanced point of operation. At this point of the study, we can only note that the model based on dc components leads to the following conclusion:

- if the duty cycles are all identical, and the current source harmonics are zero, the capacitor voltages are constant, whatever their initial values.

Any model based on the dc component or state-space averaging will yield this conclusion. In practical implementations, this conclusion must be revised because the current source impedance is noninfinite and the current harmonics are not zero. Accounting for the influence of harmonics requires a thorough study of this system, which is the aim of this paper.

B. Different Approaches to the Problem

This matter was first studied by simulation. Different behaviors and very different time responses have been observed, but the system always converged toward that special balanced voltage distribution. The values of the circuit but also the point of operation had a very strong influence on the type of response.

Prototypes have also been tested and despite the different imperfections related to actual circuits, the voltage unbalance has always been less than 5%.

Finally, this self-balancing property was demonstrated using standard circuit theory [6] and it has been shown that self-balancing was guaranteed as soon as the impedance of the current source was noninfinite (nonideal current source). In the special case when $p = 2$, the time constants have even been determined analytically.

However, except for the special case when $p = 2$, these approaches gave no information on the time constants involved in the transient.

The aim of this paper is to develop a model capable of representing the self-balancing property of this circuit, and to understand the influence of the different parameters.

IV. Modeling

The different approaches listed above seemed to show that the self-balancing property was related to the harmonics of the current source I instead of its dc component, so that the model will be based on these harmonics.

The operation of the multilevel converter of Fig. 1 is equivalent to the circuit in Fig. 3.

This circuit is obtained by choosing one mode of operation of the converter and replacing each blocking switch with a voltage source including the harmonics of the voltage across that switch and each conducting switch with a current source including the harmonics of the current flowing through that switch.

A. Assumptions

In the rest of the paper, we will go on the following assumptions.

- The switches are ideal (on-state voltage, off-state current, delays, and switching times are zero).
- Switches being ideal, dead times are zero.
- The floating capacitors are designed to limit the variations of the voltage applied to each commutation cell; in the first part of the calculation, these voltages are taken as constant over a switching period. In the same way, the variations of voltage source E are supposed to be slow compared with the switching period.
- The load has a time constant which is less than the switching period so that at each switching period, the load current is the steady-state current.

B. Various Steps of the Calculation

The calculation carried out in the Appendix proceeds as follows:

- given the state of the system ($X_k = V_{Ck}, k = 1, \cdots, p-1$) and the value of the voltage source E, the control signals ($\mathcal{R}_k$ and $\Phi_k, k = 1, \cdots, p$) determine the phase and amplitude of the voltage harmonics across switches B_k ($V^n_{B_k}, ; k = 1, \cdots, p; n = 1, \cdots, r$);
- the chopped voltage V_s is the sum of voltages across switches B_k, so the harmonics of chopped voltage V_s can be derived ($V_s^1, V_s^2, \cdots, V_s^r$ complexes);
- depending on the impedance of current source I (Z, complex), these voltage harmonics give current harmonics ($I^1, \cdots, I^r$, complexes);

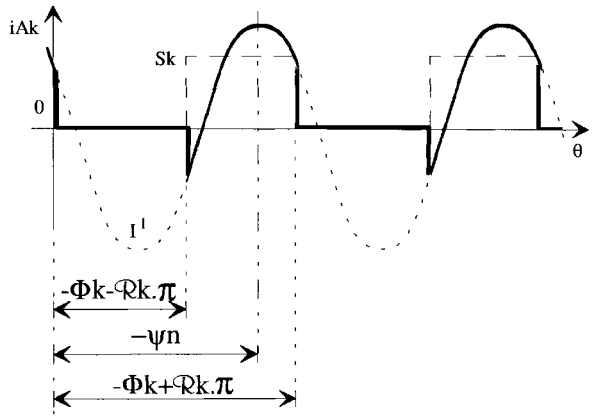


Fig. 4. Control signal S_k, current harmonic I^1, and current through A_k.

- the average current in each switch $(I_{Ak}, k = 1, \cdots, p)$ can then be calculated as a function of the phase-shift between the control signal and the current harmonic;
- the average current in the capacitor is the difference between the current in the adjoining switches;
- given the value of the capacitors $(C_k, k = 1, \cdots, p-1)$, the variation of the voltage across each capacitor $(dX_k, k = 1, \cdots, p-1)$ can be derived.

C. Calculation of the Model Accounting for the nth Harmonic

The nth harmonic of a zero to one square signal with phase Φ and duty cycle $\mathcal{R}$ is given by

$$H_n = \frac{2}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot \mathcal{R}) \cdot e^{j \cdot n \cdot \Phi}. \tag{6}$$

The chopped voltage delivered by the multilevel commutation cell is the sum of the voltages across the switches of the lower branch. Since the voltage across the kth switch is zero when conducting and $V_{C_k} - V_{C_{k-1}}$ when blocking (true for $k = 1, \cdots, p$ with $V_{C_0} = 0$ and $V_{C_p} = E$), V_s^n, the nth harmonic of the chopped voltage delivered by the multilevel commutation cell is given by

$$V_s^n = \sum_{k=1}^{p} \frac{2}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot \mathcal{R}_k) \cdot (V_{C_k} - V_{C_{k-1}}) \cdot e^{j \cdot n \cdot \Phi_k}. \tag{7}$$

Taking

$$G_k^n = \frac{1}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot \mathcal{R}_k) \cdot e^{j \cdot n \cdot \Phi_k} \tag{8}$$

equation (7) can be written in the matrix form

$$V_s^n = 2[G_1^n - G_2^n \cdots G_{p-1}^n - G_p^n] \begin{bmatrix} V_{C_1} \\ \vdots \\ V_{C_{p-1}} \end{bmatrix} + 2 G_p^n E. \tag{9}$$

The load current can then be written as a function of the impedance at this frequency:

$$I^n = \frac{V_s^n}{Z^n} = |I^n| \cdot e^{j \cdot \Psi^n}. \tag{10}$$

This current harmonic generates a current through A_k that depends on duty cycle $\mathcal{R}_k$ and phase shift $n \cdot \Phi_k - \Psi^n$ (Fig. 4).

The contribution of this current harmonic to the average current in the switch is

$$\begin{aligned} I_{A_k}^n &= \frac{1}{2 \cdot \pi} \cdot \int_{0\Phi_k - \mathcal{R}_k \cdot \pi}^{-\Phi_k + \mathcal{R}_k \cdot \pi} |I^n| \cdot \cos(n \cdot \theta + \Psi^n) \cdot d\theta \\ &= \frac{|I^n|}{2 \cdot n \cdot \pi} \cdot (\sin(n \cdot (-\Phi_k + \mathcal{R}_k \cdot \pi) + \Psi^n) \\ &\quad - \sin(n \cdot (-\Phi_k - \mathcal{R}_k \cdot \pi) + \Psi^n))) \end{aligned} \tag{11}$$

which yields

$$I_{A_k}^n = \frac{|I^n|}{n \cdot \pi} \cdot \sin(n \cdot \mathcal{R}_k \cdot \pi) \cdot \cos(n \cdot \Phi_k - \Psi^n). \tag{12}$$

This quantity can be written as

$$I_{A_k}^n = \mathrm{Re}\left(\frac{1}{n \cdot \pi} \cdot \sin(n \cdot \mathcal{R}_k \cdot \pi) \cdot e^{-j \cdot n \cdot \Phi_k} \cdot |I^n| \cdot e^{j \cdot \Psi^n} \right) \tag{13}$$

which, according to G_k^n defined above (8), can be calculated by

$$I_{A_k}^n = \mathrm{Re}(\mathrm{conj}(G_k^n) \cdot I^n). \tag{14}$$

Since

$$\dot{V}_{C_k}^n = \frac{1}{C_k} I_{C_k}^n = \frac{1}{C_k} [I_{A_{k+1}}^n - I_{A_k}^n] \tag{15}$$

we have the following matrix formulation:

$$\begin{bmatrix} \dot{V}_{C_1} \\ \vdots \\ \dot{V}_{C_{p-1}} \end{bmatrix} = \mathrm{Re}\left(\begin{bmatrix} \frac{1}{C_1} \cdot \mathrm{conj}(G_2^n - G_1^n) \\ \vdots \\ \frac{1}{C_{p-1}} \cdot \mathrm{conj}(G_p^n - G_{p-1}^n) \end{bmatrix} \cdot I^n \right). \tag{16}$$

In addition, from (9), (10), and (16) we get

$$\begin{aligned} [\dot{V}_{C_k}] = 2 \,\mathrm{Re}\Bigg(& \begin{bmatrix} \vdots \\ \frac{1}{C_k} \cdot \mathrm{conj}(G_{k+1}^n - G_k^n) \\ \vdots \end{bmatrix} \cdot \frac{1}{Z^n} \\ & \cdot ([\cdots G_k^n - G_{k+1}^n \cdots][V_{C_k}] + G_p^n E) \Bigg). \end{aligned} \tag{17}$$

X and E being real, this equation can be written in a standard $\dot{X} = A \cdot X + B \cdot U$ form with

$$\begin{aligned} A = 2 \,\mathrm{Re}\Bigg(& \begin{bmatrix} \vdots \\ \frac{1}{C_k} \cdot \mathrm{conj}(G_{k+1}^n - G_k^n) \\ \vdots \end{bmatrix} \cdot \frac{1}{Z^n} \\ & \cdot [\cdots G_k^n - G_{k+1}^n \cdots] \Bigg) \end{aligned} \tag{18}$$

$$B = 2 \,\mathrm{Re}\left(\begin{bmatrix} \vdots \\ \frac{1}{C_k} \cdot (G_{k+1}^n - G_k^n) \\ \vdots \end{bmatrix} \cdot \frac{1}{Z^n} \cdot G_p^n \right). \tag{19}$$

D. Calculation of the Model Accounting for the r First Harmonics

Taking several harmonics into account, (17) becomes

$$[\dot{V}_{C_k}] = \sum_{n=1}^{r} 2\,\mathrm{Re}\left(\left(\begin{bmatrix} \vdots \\ \frac{1}{C_k}\cdot \mathrm{conj}(G_{k+1}^n - G_k^n) \\ \vdots \end{bmatrix}\cdot \frac{1}{Z^n} \cdot ([\cdots G_k^n - G_{k+1}^n \cdots][V_{C_k}] + G_p^n E)\right)\right). \quad (20)$$

This results in a model such as

$$\dot{V}_{C_k} = A(\mathcal{R}_k)V_{C_k} + B(\mathcal{R}_k)E, \qquad k = 1,\cdots,p-1$$

with

$$A = -2\,\mathrm{Re}\left(\begin{bmatrix} \frac{\mathrm{conj}(G_1^1 - G_2^1)}{C_1} & \cdots & \frac{\mathrm{conj}(G_1^r - G_2^r)}{C_1} \\ \vdots & \ddots & \cdots \\ \frac{\mathrm{conj}(G_{p-1}^1 - G_p^1)}{C_{p-1}} & \cdots & \frac{\mathrm{conj}(G_{p-1}^r - G_p^r)}{C_{p-1}} \end{bmatrix} \cdot \begin{bmatrix} \frac{(G_1^1 - G_2^1)}{Z^1} & \cdots & \frac{(G_{p-1}^1 - G_p^1)}{Z^1} \\ \vdots & \ddots & \cdots \\ \frac{(G_1^r = G_2^r)}{Z^r} & \cdots & \frac{(G_{p-1}^r - G_p^r)}{Z^r} \end{bmatrix}\right)$$

$$B = 2\,\mathrm{Re}\left(\begin{bmatrix} \frac{\mathrm{conj}(G_1^1 - G_2^1)}{C_1} & \cdots & \frac{\mathrm{conj}(G_1^r - G_2^r)}{C_1} \\ \vdots & \ddots & \cdots \\ \frac{\mathrm{conj}(G_{p-1}^1 - G_p^1)}{C_{p-1}} & \cdots & \frac{\mathrm{conj}(G_{p-1}^r - G_p^r)}{C_{p-1}} \end{bmatrix} \cdot \begin{bmatrix} \frac{G_p^1}{Z^1} \\ \vdots \\ \frac{G_p^r}{Z^r} \end{bmatrix}\right). \quad (21)$$

V. Checking the Model

A. Principle of the Validation

This model allows predicting the evolution of the capacitor voltages starting from any initial conditions and for any duty cycle. In the next section, the model will be checked by comparison with a simulation program (that simulates the different modes of operation corresponding to the different states of the switches). This will be done using two different converters. The first is a step-down chopper using three imbricated cells (Fig. 5) and a half-bridge voltage-source inverter using seven imbricated cells (Fig. 6).

The simulation package SUCCESS is used as a reference and the accuracy of the model can be evaluated in various conditions.

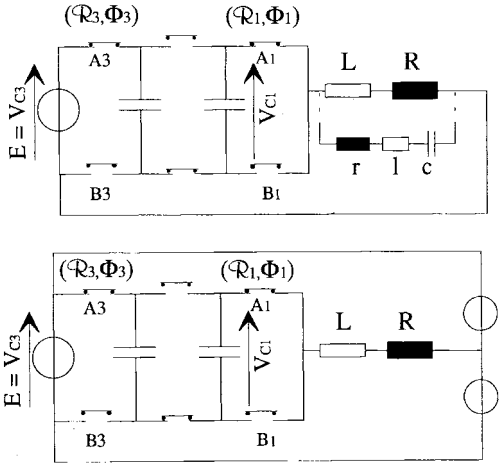


Fig. 5. Four-level converters (three cells) [unless specified, the following values are used for all simulations: $E = 2$ kV, $C_1 = C_2 = 0.1$ mF, $L = 0.2$ mH, $R = 10\ \Omega$ W, $r = 10$ MΩ MW, $l = 0.5$ mH, $c = 4.7\ \mu$F, $\mathcal{R}_1 = \mathcal{R}_2 = \mathcal{R}_3 = 0.5$, $\Phi_1 = 0$, $\Phi_2 = 120°$, $\Phi_3 = 240°$)]. (a) Step-down chopper. (b) Voltage-source inverter.

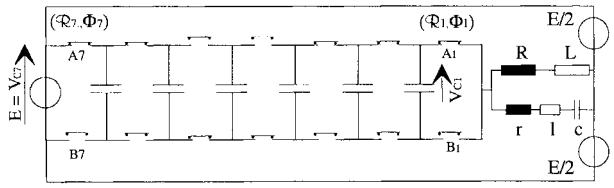


Fig. 6. Eight-level voltage-source inverter (seven cells). ($E = 2000$ v $C_1, \cdots, C_6 = 100\ \mu$F $R = 10\ \Omega$ $L = 200\ \mu$H $c = 4.7\ \mu$F $l = 500\ \mu$H $r = 1\ \Omega$).

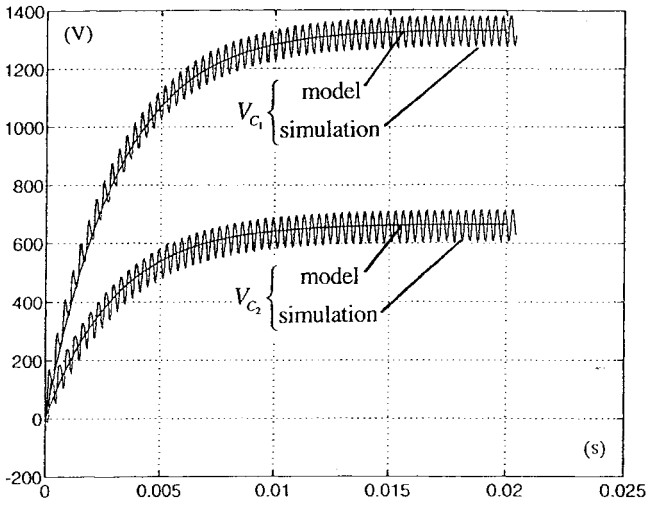
B. Start Up with Constant Duty Cycles and Constant Input Voltage

The start up of the three-cell chopper of Fig. 5(a) with $\mathcal{R} = 0.5$ is studied by simulation and with the model. The waveforms obtained for the capacitor voltages are compared in Fig. 7(a).

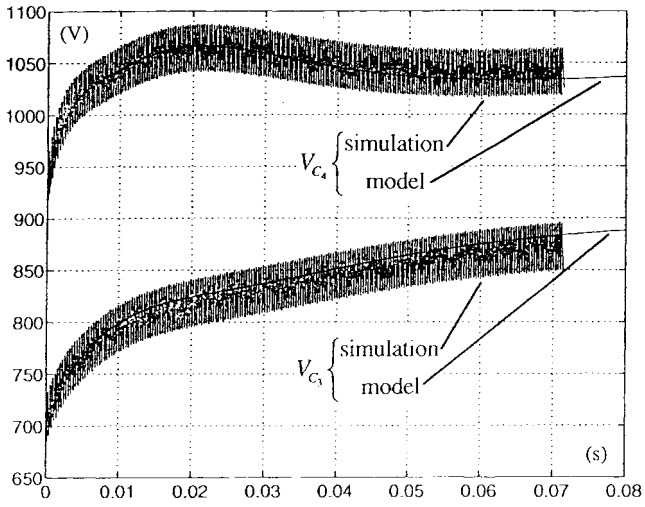
Despite a quick evolution of the capacitor voltages, which is not in agreement with the assumptions listed above, this comparison illustrates the good behavior of the model.

However, it should be noted that in the chopper configuration, the switches in the upper branch are transistors and those in the lower branch are simple diodes; in the model, the assumption is made that the two switches of a given cell are always in opposite states which is generally true, except in two cases:

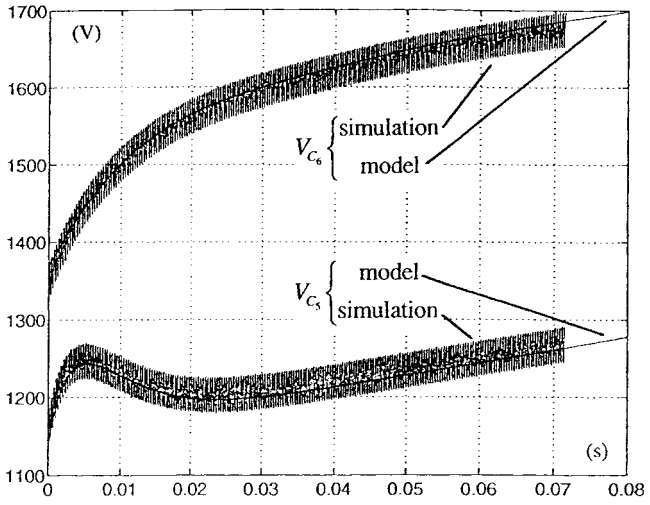
- discontinuous conduction mode—this case is obtained when the current tends to zero or a negative value; the current cannot change sign in the diodes so it stays zero and the two switches of the same cell are in the off-state simultaneously;
- "shorted-cell" mode—if the voltage across a cell tends to become negative ($V_{C_k} < V_{C_{k-1}}$), the transistor and the diode of that cell may conduct simultaneously, thus holding the cell voltage to zero (reverse conduction of the transistor).



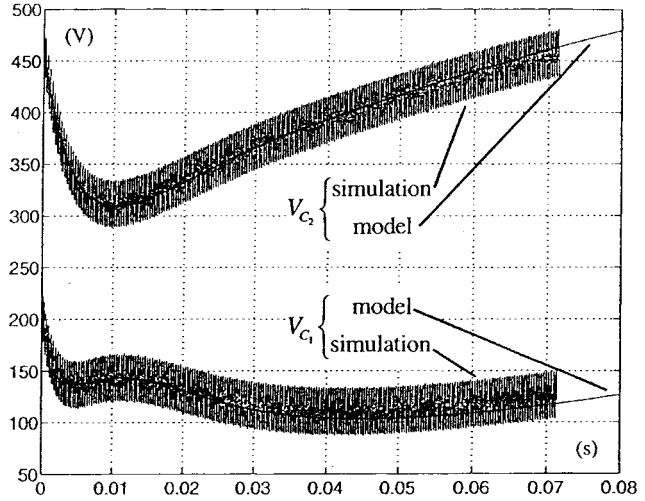
(a)



(c)



(b)



(d)

Fig. 7. Voltage across floating capacitors at start up (simulation and model). (a) Three-cell circuit [cf., Fig. 5(a)]. (b) Seven-cell circuit (cf., Fig. 6).

Voltage across floating capacitors at start up (simulation and model). (c) and (d) Seven-cell circuit (cf., Fig. 6).

When these phenomena occur, the simulation gives very different results. However, these modes are not the standard modes of operation (the second one is even dangerous for the converter) and we will not try to adapt the model to these particular conditions.

Compared results for the seven-cell voltage-source inverter are given in Fig. 7(b)–(d). In that case, the transient is quite long and the simulations have been stopped before the steady state to keep the figures clear. However, the purpose is to show the accuracy of the model, even for the pulsewidth modulation (PWM) mode of this voltage source inverter.

C. Start Up with Variable Duty Cycles

Such conditions are met in voltage-source inverters (sinusoidal variation of the duty cycles) such as the circuit in Fig. 5(b). The results compared in Fig. 8 still reveal a good agreement of the model and the system.

D. Start Up with Variable Input Voltage

Fig. 9 displays results obtained with a variable input voltage. In that case, the auxiliary r-l-c network is activated by taking $r = 1\ \Omega$ which speeds the natural balancing property. With a ramping input voltage, the model represents the system with a good accuracy except for the first few periods at the start of the perturbation. Many comparisons have been done in different conditions of operation and the model always matched the simulation after a few periods.

It should be noted that representing the evolution of the average (i.e., "averaged over a switching period") voltage across the capacitor requires taking rapid phenomena (i.e., occurring within a switching period) into account. These phenomena are accounted for by means of the harmonics.

The number of harmonics accounted for by the model must also be studied. Obviously, as long as the duty cycles are equal the dc component has no influence on the capacitors' voltages, and the model best fits the simulation when the number of harmonics is increased. However, the improvement is not significant beyond a certain number of harmonics because the current harmonics decrease with the frequency for two reasons:

- the impedance of the current source increases with increasing frequency;

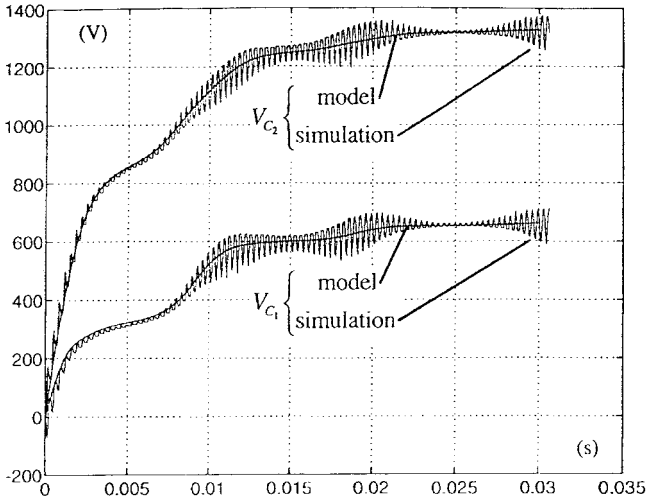


Fig. 8. Voltage across the floating capacitors at start up with 50-Hz modulation (10% $< \mathcal{R} <$ 90%) of the duty cycle. Simulation and model of the circuit in Fig. 5(b) compared.

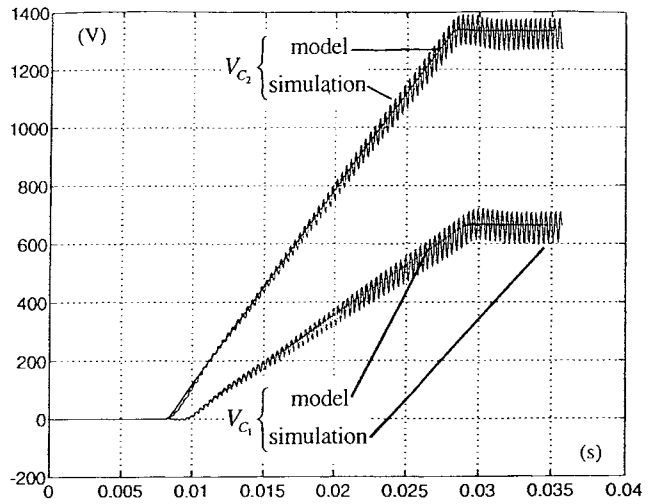


Fig. 9. Voltage across the floating capacitors with ramping input voltage (E ramps up from 0 V at 8 ms to 2 kV at 28 ms). Simulation and model of the circuit in Fig. 5(a) compared.

- the harmonics of the chopped voltage decrease with increasing frequency.

For this reason, it is generally useless to take more than ten harmonics into account.

On the other hand, the natural balancing property may disappear or be poorly represented if the number of harmonics accounted for is less than the number of cells. Consequently, the number of harmonics is generally chosen between the number of cells and ten.

When the current source impedance is modified by an auxiliary circuit such as the *RLC* network of Figs. 5(a) and 6, the impedance at the natural frequency of this network may be much lower than at any other frequency so that this current harmonic becomes predominant. In that special case, the model accounting for this only harmonic can be sufficient.

The first use of this model may be quick simulation. For example, the simulations presented here with a number of harmonics equal to the number of cells were about 20 times quicker with the model implanted in MATLAB than the simulation of the whole circuit in SUCCESS. This ratio does not vary significantly when the RLC circuit is used or not. However, quick simulation is not the only application, and we will give a few other examples of application in the following section.

VI. Applications of the Model

With such a model, the quantitative analysis is made simple. Despite the nonlinearity inherent in these converters, the static and dynamic characteristics can be easily calculated. Among the many possible utilizations of this model, three very interesting straightforward examples have been chosen.

A. Direct Calculation of the Steady State

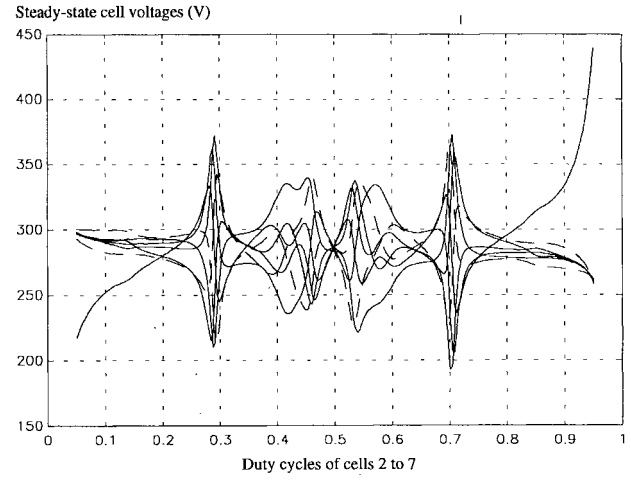
The state model of the converter (21) describes the evolution of the capacitor voltages as a function of the duty cycles. With this model it is very easy to determine the steady-state voltages

$$\dot{X} = 0 \Rightarrow Xp = -A(\mathcal{R})^{-1} * B(\mathcal{R})E. \qquad (22)$$

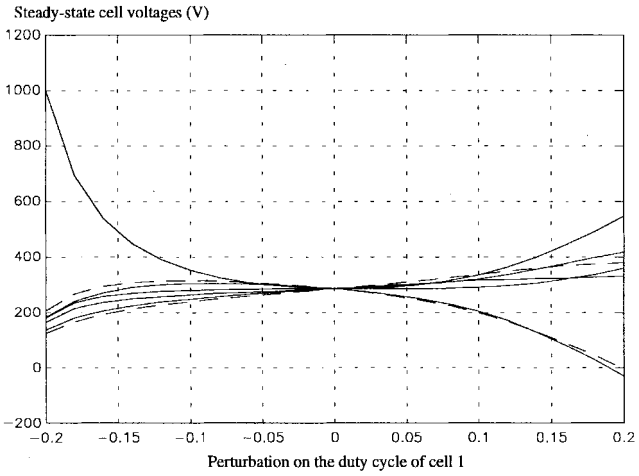
So, the model can be readily used to demonstrate the natural balancing property (with equal duty cycles, the only stable point is $V_{C_k} = k \cdot E/p$). This is already a good result because it is very difficult to demonstrate with other approaches. But the new thing is that the influence of duty cycle imbalance (slight imperfections of the control signals, different delays of different switches at turn-off, etc.) can also be studied, which was not possible by other means. For example, in Fig. 10, the influence of a perturbation of the duty cycle of cell one on the different cell voltages is studied. These curves have not been labeled individually to keep them simple and because the designer will be mainly concerned by a worst case approach; the important thing is to determine what the maximum unbalance can be, no matter what cell it is applied on. In Fig. 10(a), the perturbation is kept constant and the point of operation is moved through all the operating area ($\mathcal{R}$ varies from zero to one; $\mathcal{R}_1 = \mathcal{R} + 0.02; \mathcal{R}_2 = \mathcal{R}_3 = \cdots = \mathcal{R}_7 = \mathcal{R}$). This figure shows, in particular, that all cells may be influenced by the perturbation on $\mathcal{R}_1$ and that these influences depend strongly and nonlinearly on the point of operation. In Fig. 10(b), the point of operation is kept constant ($\mathcal{R}_2 = \mathcal{R}_3 = \cdots = \mathcal{R}_7 = 0.5$), but the perturbation on $\mathcal{R}_1$ is varied ($\mathcal{R}_1 = \mathcal{R} + \tilde{\mathcal{R}}$; $\tilde{\mathcal{R}}$ varies from -0.2 to $+0.2$). We can check that the system is balanced when the perturbation is zero and observe that the system is highly nonlinear. It should be noted that in these two cases, the average component must also be accounted for, but this can be done with the average model used in Section I.

B. Extracting the Different Time Constants

When designing such a high-voltage converter, another concern is the dynamic related to the balancing property and this information is also included in this model. For a given duty cycle, the dynamic of the system is included in matrix A, hence the name of dynamic matrix. Calculating the eigenvalues of this matrix allows characterizing the modes of the system



(a)



(b)

Fig. 10. Steady-state cell voltages for unbalanced duty cycles (circuit of Fig. 6). (a) Constant perturbation, variable duty cycle (all duty cycles equal except a 0.02 bias on the first cell). (b) Constant duty cycle, variable perturbation ($\mathcal{R}_1$ varies from 0.3 to 0.7—all others are equal to 0.5).

and deriving the time constants τ_i

$$[\omega_1, \omega_2, \cdots, \omega_{p-1}] = \text{eig}(A(\mathcal{R})) \quad \text{and} \quad \tau_i = \left|\frac{1}{\omega_i}\right|. \tag{23}$$

These time constants give information on the duration of the transient and the time required to rebalance the capacitor voltages after a perturbation.

C. Bode Plots

As for any other system, the static and dynamic behavior can also be studied in Bode plots. The Laplace transform of (21) is

$$T(p) = \frac{V_{C_k}(p)}{E(p)} = (pI - A(\mathcal{R}))^{-1} * B(\mathcal{R}). \tag{24}$$

The study of these transmittances gives information on the low-frequency gains (i.e., self balancing of the cell voltages in these multilevel converters) and on the bandwidth (i.e., which frequencies of the input voltage are dangerous for the converter). This will not be discussed in this paper, but the model is, of course, very useful for this process too.

VII. Conclusion

A static and dynamic model of multilevel converters with imbricated cells must take into account phenomena that occur within a switching period. This excludes all modeling techniques based on the only average value. The model described in this paper uses current sources of which harmonic spectra are determined by the current flowing through the switches. The topology of this equivalent circuit is then used to build the state equation of the model to represent accurately the operation of the converter.

This model can be used to determine the steady-state mode as well as the dynamic response of the capacitor voltages. Linearization of this model will also be very useful to determine the control strategy of the system.

Appendix
Notations

F_{sw}	Switching frequency.
E	Voltage across the dc voltage source.
r	Maximum rank of the harmonics used in the calculation.
i	Instantaneous current in the current source.
I	Current in the current source averaged over a switching period.
I^n	$n = 1, \cdots, r$: Harmonics of the current in the current source (complex vector).
Ψ^n	$n = 1, \cdots, r$: Phases of the harmonics of the current in the current source (complex vector).
p	Number of cells.
C_k	$k = 1, \cdots, p-1$: Value of the capacitors (vector).
V_{C_k}	$k = 1, \cdots, p-1$: Voltage across the capacitors (vector).
V_{C_0}	0.
V_{C_p}	E.
A_k	$k = 1, \cdots, p$: Upper switches of the different cells (vector).
B_k	$k = 1, \cdots, p$: Lower switches of the different cells (vector).
$\mathcal{R}_k$	$k = 1, \cdots, p$: Duty cycles of switches Ak (vector).
Φ_k	$k = 1, \cdots, p$: Phases of the control signal of switches A_k (vector).
v_s	Instantaneous chopped voltage.
V_s	Chopped voltage averaged over a switching period.
V_S^n	$n = 1, \cdots, r$: nth harmonic of the chopped voltage (complex vector).
i_{A_k}	$k = 1, \cdots, p$: Instantaneous current in switch A_k (vector).
I_{A_k}	$k = 1, \cdots, p$: Current in switch A_k averaged over a switching period (vector).
$I^n_{A_k}$	$k = 1, \cdots, p$: Current in switches A_k averaged over a switching period. $n = 1, \cdots, r$: Resulting of the n-th harmonic of current i (matrix).

v_{B_k} $k = 1, \cdots, p$: Instantaneous voltages across switches B_k (vector)

V_{B_k} $k = 1, \cdots, p$: Voltage across switch B_k averaged over a switching period (vector).

$V_{B_k}^n$ $k = 1, \cdots, p$: nth harmonic of voltage (complex matrix).
$n = 1, \cdots, r$

Z^n $n = 1, \cdots, r$: Impedance of the current source at the frequency $n \cdot F_{sw}$ (complex vector).

G_k^n see (A.3).

REFERENCES

[1] R. D. Middelbrook and S. Cuk, "A general unified approach to modeling switching converter power stages," in *IEEE Power Electron. Specialists Conf. Rec.*, 1976, pp. 18–34.

[2] V. Vorperian and S. Cuk, "Small signal analysis of resonant converter," in *IEEE Power Electron. Specialists Conf. Rec.*, 1983, pp. 269–282.

[3] C. Collomb, M. Fadel, Y. Cheron, "Analysis of dc/dc series resonant converter operating above natural frequency," *Eur. Power Electron. Conf. Rec.*, Firenze, Italy, 1991 vol. 4, pp. 542–547.

[4] S. Sanders, J. Noworolski, X. Liu, G. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Power Electron. Specialists Conf. Rec.*, 1990, pp. 333–340.

[5] T. A. Meynard and H. Foch, "Dispositif Électronique de conversion d'énergie electrique," Brevet Français 91.09582, July 1991; Dépot Int. P.C.T. (Eur., Jpn., USA, Canada) 92/00652, July 1992.

[6] ———, "Multilevel choppers for high voltage applications," *Eur. Power Electron. J.* vol. 2, pp. 45–50, Mar. 1992.

[7] ———, "Multilevel converters and derived topologies for high power conversion," in *IECON'95*, Orlando, FL, 1995, pp. 21–26.

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