Residual stress evaluation in resin-molded IC chips using finite element analysis and piezoresistive gauges

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Abstract

The high residual stress in a resin-molded electronic package sometimes makes the electronic functions unstable. Therefore the residual stress in electronic packages, especially on the top surfaces of semiconductor chips, should be evaluated. The objective of this study is to present a simple method for evaluating residual stress in resin-molded semiconductor chips using a combination of experimental and numerical methods. The actual residual stress of the packaging process was measured by using test chips that included piezoresistive gauges. A linear thermoelastic finite element analysis was then carried out using a three-dimensional model. The finite element analysis was performed under a stress-free temperature determined by the temperature dependence of the residual stress, which was experimentally measured by using the piezoresistive test chips. The measured residual stress using the test chips agreed well with the results of the finite element analysis. It was therefore confirmed that the present evaluation method, combining experimental and numerical methods, is reliable and reasonable.

Keywords: residual stress; finite element analysis; piezoresistive gauge; resin-molded package; stress-free temperature

1. Introduction

An electronic package is a composite structure composed of various materials such as silicon, epoxy resin, glass-epoxy substrate, and so on. These materials differ greatly in their coefficients of thermal expansion (CTE). Such differences generate high residual stresses in the resin-molding processes. These stresses, in turn, sometimes lead to failures at junctions or along interfaces between dissimilar materials in the electronic packages. The residual stresses in electronic packages also affect the electronic characteristics of the devices. It was found that the stress or strain on the surface of a semiconductor chip affects transistor characteristics such as transconductance and threshold voltage [1-5]. This type of stress has become one of the most serious issues in the production of electronic devices. This problem is considered especially serious for devices that use ultra-high frequency or high-density packages such as a system-in-a-package (SiP). Hence, it is necessary to evaluate the residual stress on the surface of a semiconductor chip to avoid electronic failure in electronic devices.

Piezoresistive gauges formed on a silicon chip have been used for experimental measurements of the stress in IC chips [6, 7]. Residual stress can be measured during the packaging process by encapsulating a chip that includes piezoresistive gauges into the package. Commercial piezoresistive chips have been generally used as test chips in order to evaluate the residual stress in package production, but a test chip cannot always provide useful information for package designers or developers. The shape of a test chip is limited, as are the configuration and number of gauges, even though there are a lot of package designs or materials. It is therefore considered that the combination of finite element analysis and experimental measurement using piezoresistive test

chips is helpful for evaluating residual stress in IC chips. Because molding resin has viscoelastic properties, viscoelastic finite element analysis has often been performed to estimate the residual stress or warpage in a plastic package [8, 9]. However, the identification of viscoelastic properties by viscoelastic analysis usually requires a lot of work, and it is very difficult to perform an accurate analysis around the glass transition temperature (T_g) of the resin. So a simple but reliable method for evaluating the residual stress in IC chips is required in order to satisfy the need for quick development of electronic devices.

The purpose of this study is to present a simple method for evaluating residual stress in a resin-molded electronic package, with a particular focus on the distribution of stress on an IC chip surface by combining an experimental method with a test chip containing piezoresistive gauges and by using linear thermoelastic finite element analysis. The validity of the present evaluation method was demonstrated by using it to measure the residual stress in the quad flat package (QFP). In this paper, the evaluation method and the results are demonstrated.

2. Measurement of residual stress using piezoresistive test chips

2.1 Piezoresistive test chips

We used commercial test chips manufactured by Hitachi ULSI Systems Co., Ltd. Equation (1) shows the simplest relationship between the stress and the change of resistance. It is well known that the rate of resistance change is proportional to the stress [10].

$$(R - R_0)/R_0 = S \times \sigma \tag{1}$$

Here, S and σ represent the stress sensitivity and the stress, respectively. Then, the residual stress during the packaging process can be determined by measuring the resistance before the packaging process (R_0) and that after the packaging process (R). The piezoresistance properties of the test chips are documented by the manufacturer [11]. The calibration data of the piezoresistive properties is obtained by the four-point bending method, and the specimens for the calibration are prepared from the same wafer that we used. The plotted data in Fig. 1(a) show the rate of resistance change with stress at 30°C for the piezoresistive gauges used in the present study. The stress sensitivity S was determined from the gradient of the least-squares line in Fig. 1(a). The plotted data in Figs. 1(b) and (c) show that S and the piezoresistance vary with temperature. The parameter α of the temperature sensitivity in S and the parameter β of the temperature sensitivity in the piezoresistance were determined from the gradients of the least-squares lines in Figs. 1(b) and (c), respectively. Table 1 summarizes the values of S, α, and β. In the present measurements, the residual stress is obtained using Equation (2), in which the temperature effect on the properties of piezoresistance is taken into account.

$$(R_{(T)} - R_{0(T_0)})/R_{0(T_0)} = \beta(T - T_0) + (1 - \alpha(T - T_0))(S \times \sigma_{(T)}) \tag{2}$$

Here, the subscripts T_0 and T denote the temperatures when R_0 and R were measured, respectively.

Figure 2(a) illustrates the configurations of the gauges on test chips. Two different chip shapes, shown as Chip 1 and Chip 2, were used, as shown in Fig. 2(a). Chip 2-1 and Chip 2-2 are similar in shape but their gauges are in different locations. The test chips are 3 mm or 6 mm in length and 0.3 mm in thickness. Two pairs of piezoresistive gauges (gauges #1~4), located on each test chip as shown in Fig. 2(a), are used to measure the normal stress (i.e., σ_{xx} or σ_{yy} in Fig.2 (a)) in the

longitudinal direction of each gauge. The piezoresistive gauge can be used to measure the normal stress in the longitudinal direction of the gauge; the stress sensitivity in the longitudinal direction of the gauge is the largest. Figure 2(b) shows the pattern and length of each gauge. The gauges are formed on the silicon (001) surface. The longitudinal direction of the gauges (i.e., x- or y-direction in Fig. 2(a)) is the silicon <110> or <-110> direction. As shown in Fig. 3, the analysis coordinate system (x, y, z) is taken in such a way that the x- and y-axes coincide with the silicon <110> and <-110> directions, respectively. The vertical normal stress and the shear stress cannot be separated from the longitudinal normal stress of the gauge in the present test chips; when the longitudinal direction of the gauge is the x- direction, σ_{yy} (vertical normal stress) and τ_{xy} (shear stress) cannot be separated from σ_{xx} (longitudinal normal stress). According to the specifications of the test chips [11], the stress sensitivities in the vertical and shear directions are approximately 1/100 ~ 1/10 that in the longitudinal direction, respectively. It is therefore considered that the longitudinal normal stress measured with the test chip may have an error range of 1 % to 10 %. The permissible measuring range of stress is -250 MPa~+250 MPa, and the measurement accuracy of stress is ±10 MPa according to the manufacturer's specifications.

2.2 Measurement of residual stress

Figure 4 shows the experimental procedure for measuring residual stress using piezoresistive test chips. The chips were encapsulated in a QFP via die bonding, wire bonding, and resin molding. Then, the piezoresistance after each process was measured. R_0 is the piezoresistance of the bare chip. R_1 and R_2 are the piezoresistances after die bonding and resin molding, respectively. The residual

stress during the die bonding process was determined from R_0 and R_1, and the residual stress during the packaging process was determined from R_0 and R_2 using Equation (2). The piezoresistance was measured by a four-point probe method using a digital multimeter.

In this study, R_0 was first measured, and R_1 after die bonding was then measured by probing the test chip directly. The measurements were conducted in a shading box. The temperature during the piezoresistance measurement was monitored using the thermocouple in the shading box. After the wire bonding and resin-molding processes, R_2 was measured in a constant-temperature oven. The temperature was measured with a thermocouple attached to the surface of the QFP specimen using heat-resistant adhesive tape. All of the measurements were carried out after the temperature of the specimen had reached a steady state.

The manufacturing conditions of the QFP specimen were as follows. The die bonding paste was cured at 180°C for 2 hours. In the resin-molding process, the mold temperature was 175°C and the molding resin was cured at 180°C for 5 hours. The configurations of the QFP specimen were measured using a micrometer or the scale of a digital microscope. The thickness of the QFP was 1.4 mm, the thickness between the bottom surface of the die pad and that of the QFP (i.e., the thickness of molding resin under the die pad) was 0.495 mm, and the thickness of the layer of conductive adhesive paste between the die and die pad was 0.01 mm. Other configurations of the QFP specimen for the finite element analysis were those of the design values: the length of the QFP was 14 mm, and the die pad was 6 mm in length and 0.15 mm in thickness. All of specimens have the same constitution except for the die (piezoresistive test chip); the test chips are 3 mm (Chip 1) or 6 mm (Chip 2) in length and 0.3 mm in thickness.

3. Finite element analysis

When linear thermoelastic finite element analysis is used to obtain the residual stress of a plastic package, it is often assumed that there is no thermal stress at the resin molding or the cure temperature [12-14]. This may result in the overestimation of residual stress at room temperature, because the T_g of the molding resin is usually below the resin-molding or cure temperature and because the relaxation of the residual stress is thought to occur around the T_g due to the creep.

In this study, we evaluated residual stress at room temperature using linear thermoelastic analyses based on the stress-free temperature [15], which was decided from the experimental measurement as mentioned in the next section (section 4). This approach is used to reduce the cost of analysis and to obtain more accurate residual stress in a plastic package.

One-quarter of the QFP was modeled as Fig. 5(a), taking account of the symmetry of the QFP. Three-dimensional finite element models of the QFP were generated using I-DEAS™ CAD software. The die, the molding resin, the layer of conductive adhesive paste between the die and die pad, and the die pad itself were modeled, as shown in Fig. 5(a). In this model, the details of the leadframe and bonding wires were ignored in order to minimize the cost of analysis. The main cause of residual stress on the surface of the semiconductor chip is the mismatch of the coefficients of thermal expansion (CTEs) among the semiconductor chip, the molding resin, and the die pad. Hence, the effect of the leadframe and bonding wires around the semiconductor chip on residual stress is considered to be limited. Figure 5(b) shows the finite element model of Chip 1. The numbers of elements and nodes are 17572 and 31731, respectively. The analyses were performed

using ANSYS^{TM} finite element software by reducing the temperature from the stress-free temperature to room temperature (25°C). The material properties of the components in the QFP will be given in the next section.

4. Results of evaluation

4.1 Material properties of components in QFP

Table 2 shows the material properties used in the analysis. The elasticity matrix shown in Table 3 was used to consider the anisotropy of the elastic constants of silicon. Silicon is a cubic crystal, so the elasticity matrix has three independent components in the crystallographic coordinate system as shown in Table 3 [16]. In practical analysis, the components of the elasticity matrix were transformed from the crystallographic coordinate system to the analytical coordinate system by referring to Fig. 3. The CTEs of the molding resins were measured using a thermomechanical analyzer (TMA). The temperature dependence of the elastic constants was not considered, because the residual stress obtained from the linear thermoelastic analysis depends on the elastic constants at the “evaluating temperature” (i.e., room temperature; 25°C in this study) and on the CTE from the “reference temperature” (at which the stress is zero; stress-free temperature) to the “evaluating temperature”. The main cause of residual stress on the surface of the semiconductor chip is considered to be the mismatch between the CTE of silicon and that of the molding resin; the latter are a critical factor in the present analysis. The CTEs of molding resins sometimes fluctuate among

production lots. Therefore, the CTEs of the molding resins actually used in the analysis were measured using the TMA. Other material properties were provided by the manufacturers of the materials.

In this work, two types of resins were used for the molding: Resin A and Resin B, which have different CTEs. The TMA results for these resins are shown in Figs. 6(a) and (b), respectively. The rate of elongation with temperature is shown in each figure. As shown in Fig. 6(a), Resin A clearly has T_g around 120°C. In contrast, the T_g of Resin B is not clear, and the gradient of the line changes gradually from 120°C to 150°C as shown in Fig. 6(b). Resin B is considered a mixture of polymers having different molecular weights. Both resins show good linearity between room temperature and 120°C, and the CTEs of Resin A and Resin B were determined to be 12.2×10^{-6}/°C and 30.1×10^{-6}/°C, respectively. CTEs above 120°C are not needed, since the stress-free temperature defined in section 4.3 is below 120°C.

4.2 Experimental results

We used three kinds of specimens having different combinations of chip shape and resin type: the combination of Chip 1 and Resin A (specimen Chip1-Resin A), that of Chip 1 and Resin B (specimen Chip 1-Resin B), and that of Chip 2 and Resin A (specimen Chip 2-Resin A). Figures 7(a), (b), and (c) show the results of the residual stress after the die bonding (after curing) and packaging (after curing). The residual stress was determined by assuming that the stress of the bare chip equals zero. In the legend for Fig. 7, “near chip edge” means the average stress of gauges #1

and #2 in Chip 1 or Chip 2-2, “near chip center” means the average stress of gauges #3 and #4 in Chip 1 or of gauges #1 and #2 in Chip 2-1.

The residual stresses on the surface of the semiconductor chip in the QFP obtained from the experiments were compressive 80 MPa for Resin A and compressive 160 MPa for Resin B. The CTE of Resin B is 2.5 times that of Resin A. On the other hand, the residual stress on the surface of the semiconductor chip in the QFP with Resin B is twice that with Resin A. Therefore, the higher residual stress in the QFP with Resin B is obviously caused by this resin’s higher CTE. According to our experiments, all die bonding stresses were below 10 MPa. The results clearly show that the effects of die bonding on residual stress in a semiconductor chip are limited in comparison with the effects of resin molding.

4.3 Temperature dependence of residual stress and stress-free temperature

In this study, a finite element analysis during the resin-molding process was carried out, since the die bonding process has little effect on the residual stress of the surface of a semiconductor chip. The analytical results were compared with the experimental results.

First, we measured the temperature sensitivity of the piezoresistance of a test chip bonded to a die pad. If the temperature sensitivity of the piezoresistance of the test chip after die bonding is used in Equation (2), the calculated stress indicates the residual stress during the resin-molding process. The piezoresistance after die bonding varies with temperature as shown in Fig. 8. The parameter β_m of the temperature sensitivity of the piezoresistance after die bonding was determined by the gradient of the least-squares line in Fig. 8. As a result, β_m was determined to be 1.65×10^{-3}/°C. The

stresses shown hereafter were calculated by using β_m in Equation (2); therefore these stresses show the residual stress during the resin-molding process (after die bonding).

The residual stresses during the resin-molding process were measured with increasing temperature in order to determine the stress-free temperature. These measurements were carried out for the Chip 1-Resin A, Chip 1-Resin B, and Chip 2-1-Resin A specimens. The piezoresistances of gauges were measured in a constant-temperature oven. The procedure for the measurement was similar to that in the previous section. The measurements were performed using gauge #4 for the Chip 1-Resin A and Chip 1-Resin B specimens, and gauge #2 was used for the Chip 2-1-Resin A specimen. Figures 9 (a), (b), and (c) show the residual stress with temperature for the Chip 1-Resin A, Chip 1-Resin B, and Chip 2-1-Resin A specimens, respectively. For each specimen, the relationship between stress and temperature shows good linearity, and straight lines were obtained by the least-squares method as shown by the solid lines in Fig. 9. The stress-free temperature is defined as that at which the residual stress becomes zero. We can obtain it from Fig. 9 at the point where the solid line crosses the horizontal axis. The stress-free temperatures of the Chip 1-Resin A, Chip 1-Resin B, and Chip 2-1-Resin A specimens were 116°C, 117°C, and 113°C, respectively. These stress-free temperatures were used as reference temperatures in the linear thermoelastic finite element analysis to estimate residual stress induced at room temperature during the resin-molding process.

As shown in Fig. 9, almost all the stress-free temperatures for the three specimens are a few degrees lower than the T_g of molded resins (approximately 120°C). In addition, the residual-stress-versus-temperature curves show good linearity under the stress-free temperatures. This validates the use of the linear thermoelastic approximation based on the stress-free

temperature. For the thermal stress analysis, if we use the molding temperature (175°C) or curing temperature (180°C) of the resin as the reference temperature at which the stress is zero, the residual stress will be overestimated. The finite element analyses using the stress-free temperatures determined by the residual stress, which is measured by the piezoresistive gauge during the resin-molding process, allow us to determine the residual stress during the resin-molding process.

4.4 FEA results

The counters of residual stress obtained by finite element analyses are shown in Figs. 10 (a), (b), and (c) with the experimental results of measurement using the piezoresistive gauges. These figures show the normal stress in the x direction (σ_{xx}). One-quarter of the chip surface is shown in each figure because of the symmetry of the QFP. The rectangular frames in Fig. 10 illustrate the positions of the piezoresistive gauges with the actual longitudinal proportions. The values indicated in Fig. 10 are the average stresses measured with gauges #1 and #2 or #3 and #4 shown in Fig. 2(a). The experimental data for both Chip 2-1-Resin A and Chip 2-2-Resin A specimens are shown in Fig.10(c); the results of the finite element analyses are the same for these two types of specimens. The values of stress measured with the piezoresistive gauges are shown in Figs. 10 (a), (b), and (c), together with those obtained by finite element analysis at the centers of the respective gauges. In Fig. 10(c), only the experimental result, -57 MPa, is low compared with other gauges in Chip 2-Resin A. Taking this correlation and the stress counters in Fig. 10(c) into consideration, it is considered that the 42% difference (-57MPa (experimental) versus -81MPa (FEA)) is caused by error in the piezoresistance measurement when the piezoresistance of the bare chip or after die

bonding was measured by probing the test chip directly. The piezoresistance of the gauge may be affected by the contact condition between the probe and the electrode pad of the piezoresistive gauge. It is considered that the experimental results may include the error in the measurements of piezoresistance and temperature. From the results in Fig. 10, the difference between experimental and simulation results is found to be under approximately 20 % (except for -57 MPa in Fig. 10(c)). This relative accuracy is sufficient for practical use, because the present method is used for evaluating the stress-induced effect on the electronic characteristics of electronic devices; the present method is not used for evaluating the fracture or delamination from the singular stress field, which requires a strict evaluation of stress, in the electronic package. The electric characteristics of MOSFETs may shift by around 10 % with 100 MPa stress [1-5]; however, an estimation accuracy of as low as a few percent is not required for this amount of shift. Therefore, it is considered that our evaluation method is useful for the design and manufacture of electronic packages. The finite element analysis performed in this study is a simple linear thermoelastic analysis in which neither the viscoelastic properties of the molding resin nor the detailed structure of the packaging is considered in the finite element models. However, we can verify the validity of the linear thermoelastic analysis by using the present method. By combining the linear thermoelastic analyses with the stress-free temperatures determined using the test chip containing the piezoresistive gauges, we can very accurately evaluate the residual stress on the surface of a semiconductor chip in a plastic package. It is reported that the residual stress of an IC chip in a plastic package is greatly affected by the materials and structures of the package [12, 17-18]. Therefore, we must remeasure the stress-free temperature when the materials and structures of a package are changed. Even though we considered such a procedure, our evaluation method can yield a reliable value of residual

stress in the plastic package during its production process at a lower cost compared with conventional methods.

5. Conclusions

We proposed a new method for evaluating residual stress in resin-molded semiconductor chips using test chips that contain piezoresistive gauges in conjunction with linear thermoelastic finite element analysis.

The stress-free temperature was determined from the temperature dependence of the residual stress measured by the piezoresistive gauges. We performed the linear thermoelastic finite element analysis using the stress-free temperature as the reference temperature at which thermal stress is zero, by assuming that the packages behave as linear thermoelastic materials under the stress-free temperature.

The residual stress on the top surface of a semiconductor chip was evaluated by the proposed finite element analysis in conjunction with the stress-free temperature experimentally measured with piezoresistive gauges. The proposed method determines residual stress at an accuracy of 10 to 20 MPa. It is therefore concluded that the proposed method is a cost-effective and reliable approach to evaluating residual stress in a package without relying on detailed information on the nonlinear behaviors of resin materials.

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Captions

Fig. 1. Piezoresistance properties [11].

Fig. 2. Piezoresistive test chips.

Fig. 3. Coordinate system of test chip.

Fig. 4. Experimental procedure for residual stress measurement.

Fig. 5. Finite element analysis model of QFP.

Fig. 6. Experimental results of coefficient of thermal expansion of molding resin by TMA.

Fig. 7. Experimental results of residual stress after die bonding and packaging.

Fig. 8. Temperature dependence of coefficient of piezoresistance.

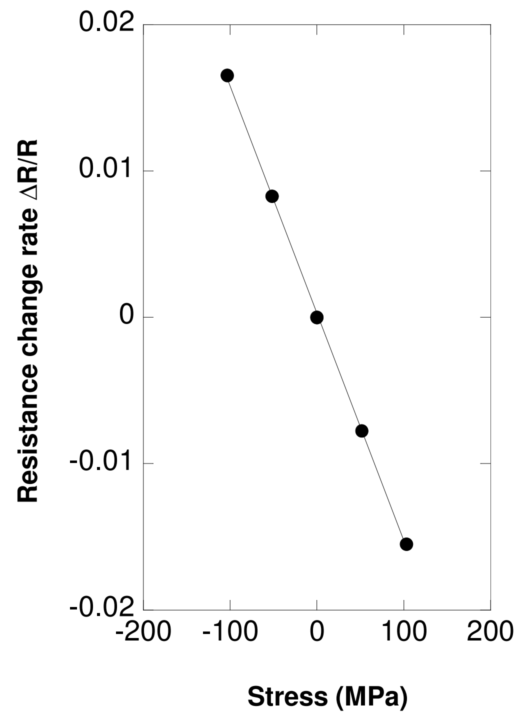
Fig. 9. Temperature dependence of residual stress.

Fig. 10. Experimental results and finite element results of residual stress σ_x in semiconductor chips.

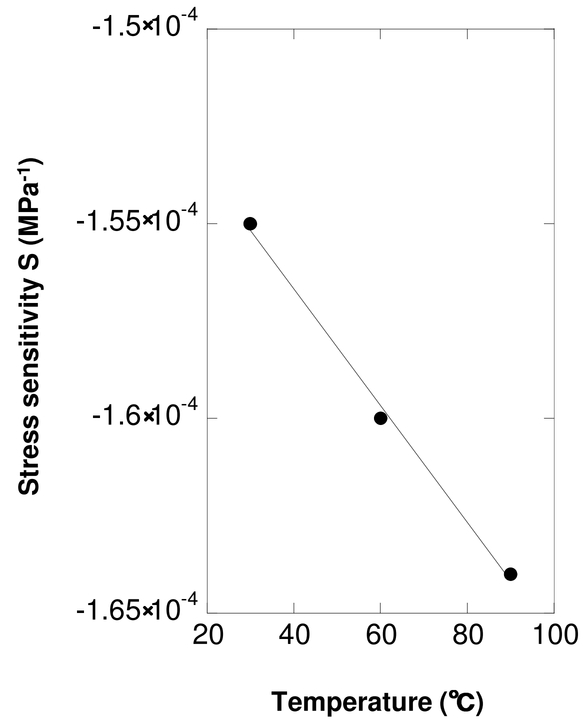
Table 1 Calibration parameters of piezoresistance

Table 2 Material properties used in FEA analysis

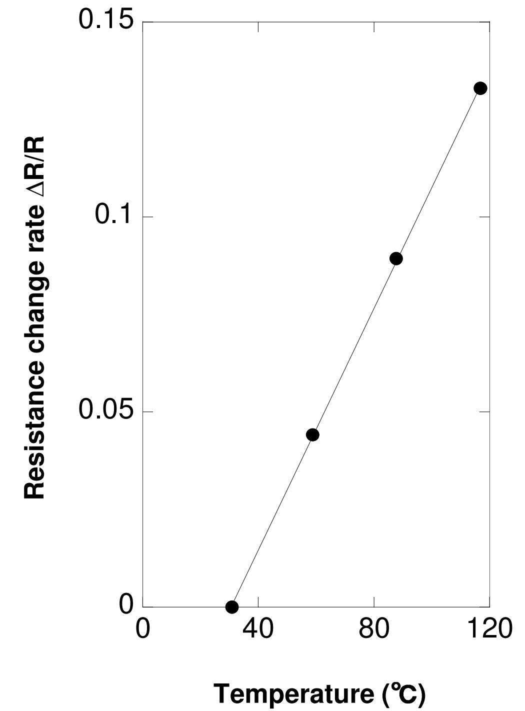
Table 3 Components of stiffness constants of silicon [16]



(a) Stress sensitivity

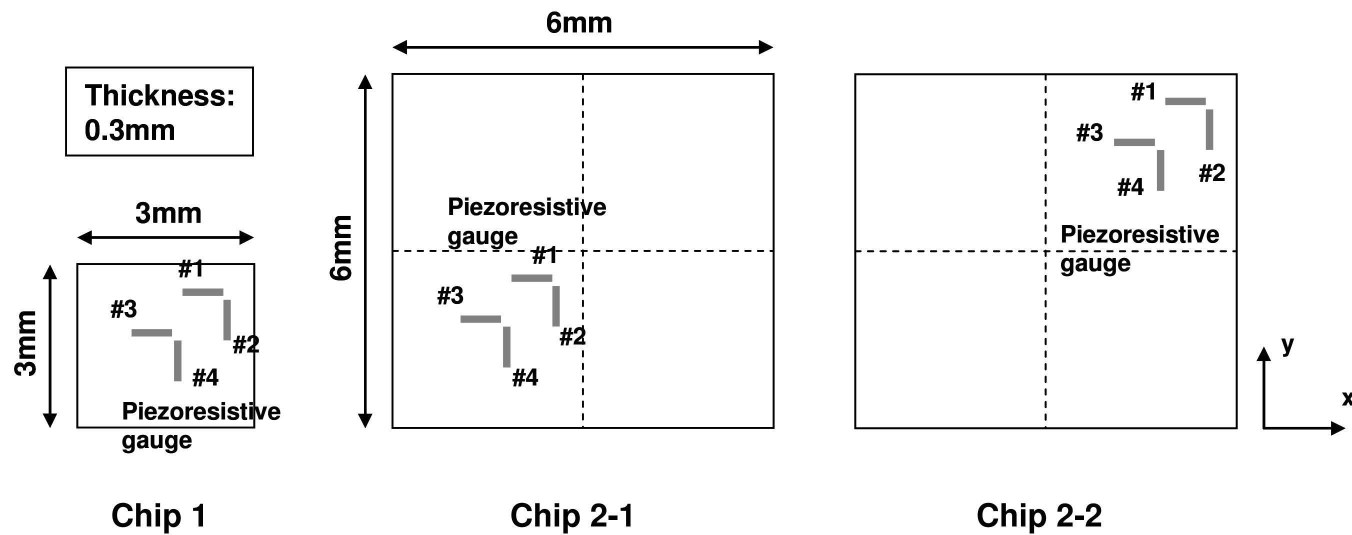


(b) Thermal dependence of stress sensitivity

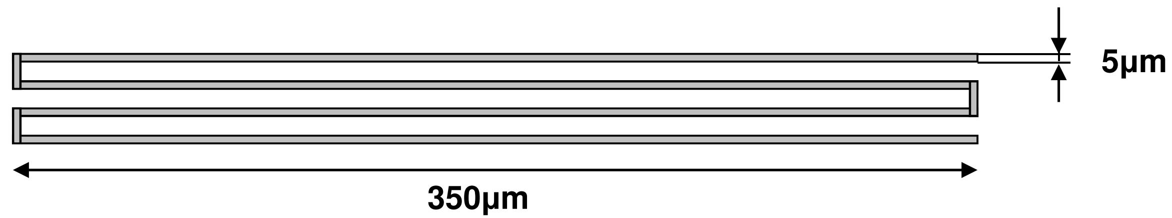


(c) Thermal dependence of piezoresistance

Fig.1 Piezoresistance properties [11)]



(a) Configuration of gauges on a test chip



(b) Shape of piezoresistive gauge

Fig.2 Piezoresistive test chips

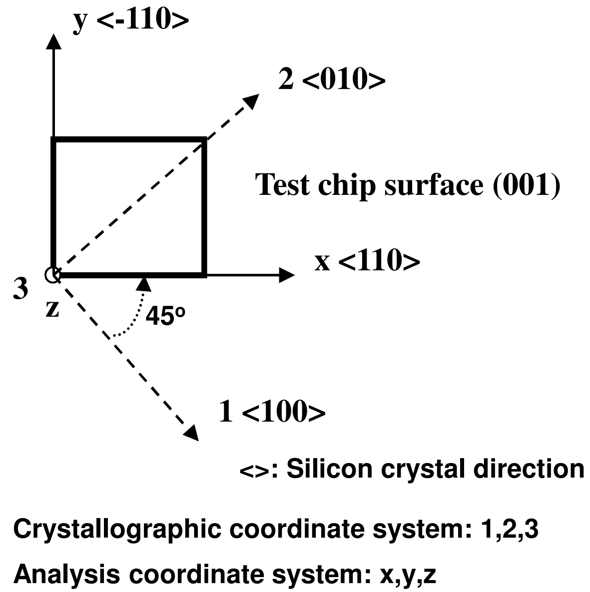


Fig.3 Coordinate system of test chip

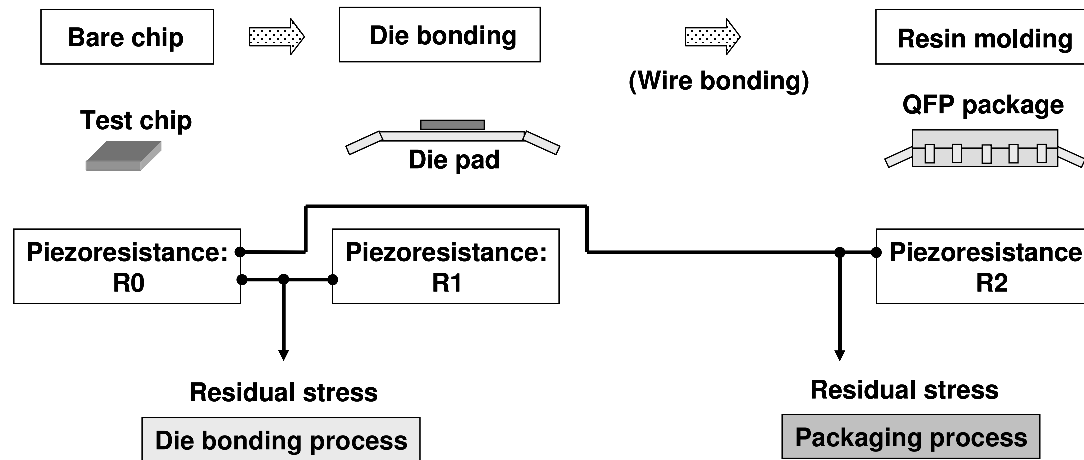
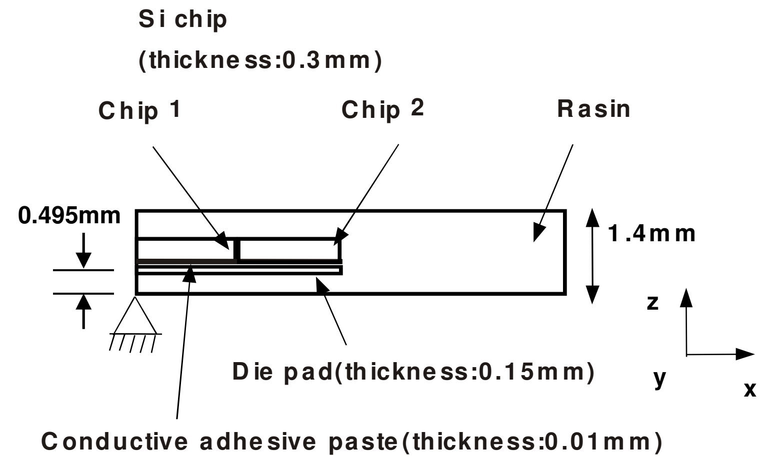
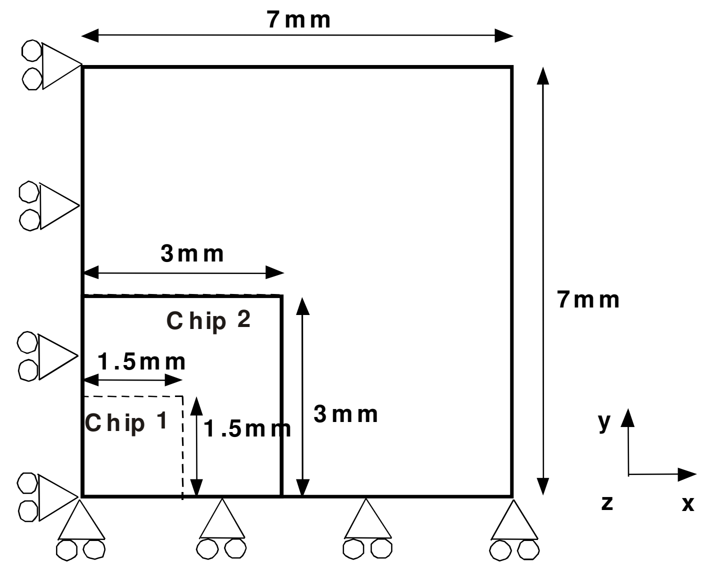


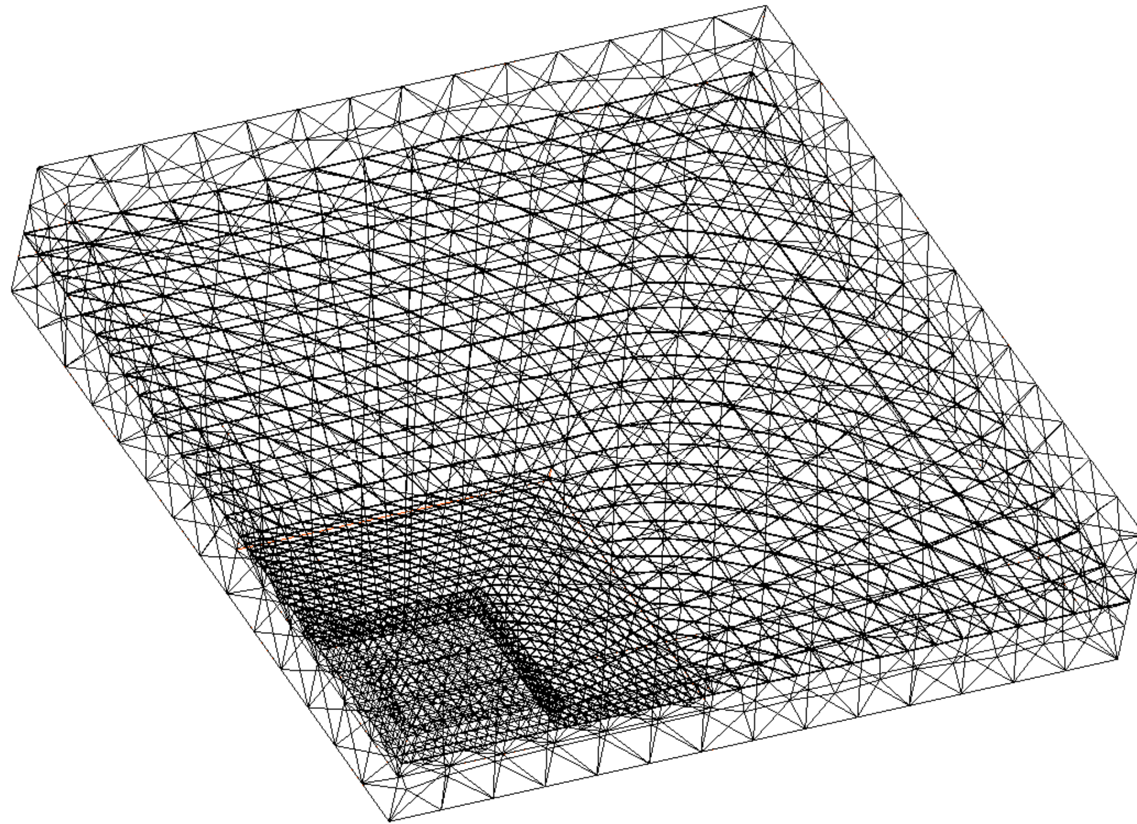
Fig.4 Experimental procedure for residual stress measurement





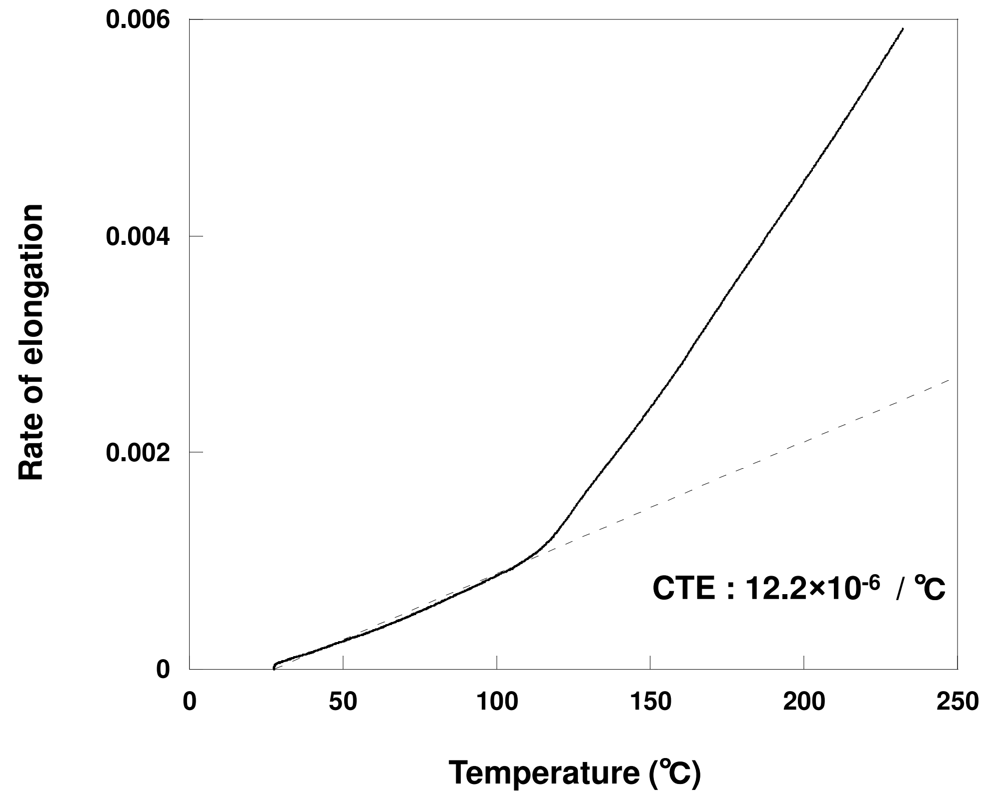
(a) Boundary conditions

Fig.5 Finite element analysis model of QFP



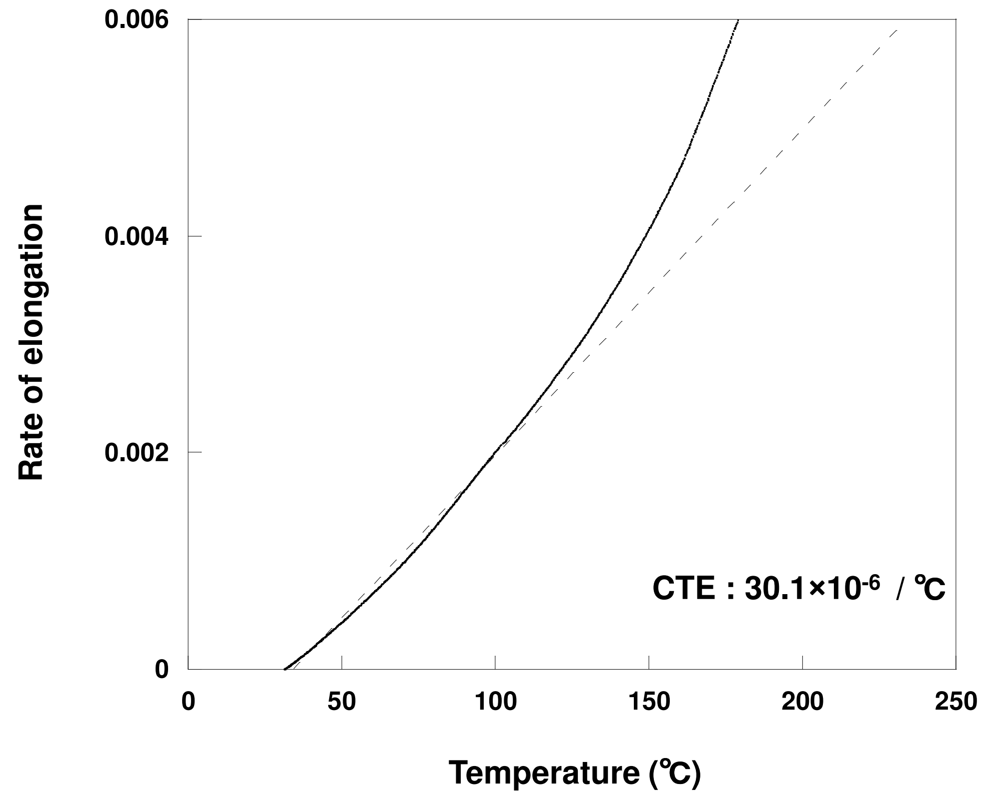
(b) Finite elements (Chip 1)

Fig.5 FEM analysis model of QFP



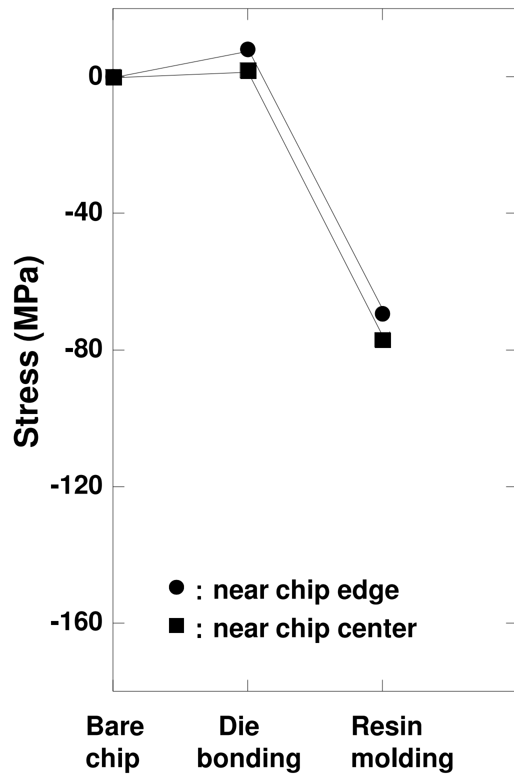
(a) Resin A

Fig.6 Experimental results of coefficient of thermal expansion of molding resin by TMA

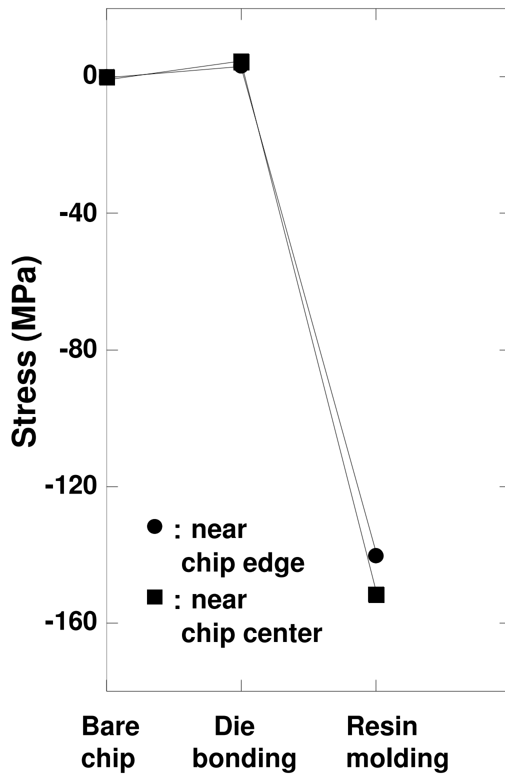


(b) Resin B

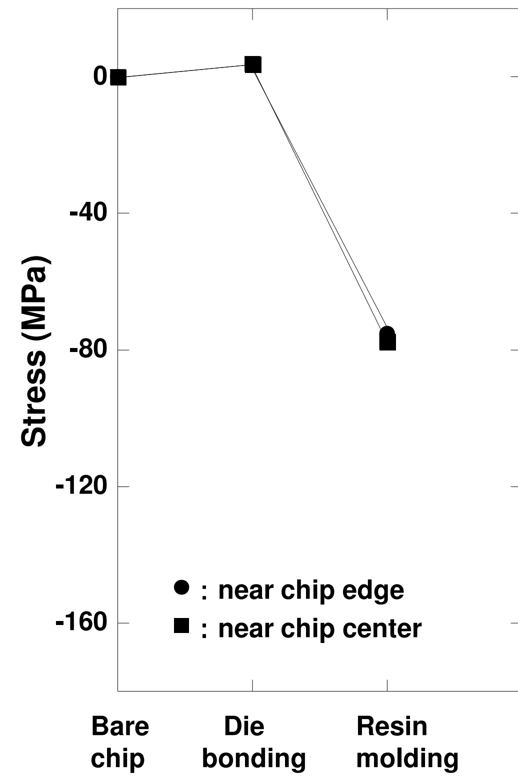
Fig.6 Experimental results of coefficient of thermal expansion of molding resin by TMA



(a) Chip 1- Resin A



(b) Chip 1- Resin B



(c) Chip 2- Resin A

Fig.7 Experimental results of residual stress after die bonding and packaging

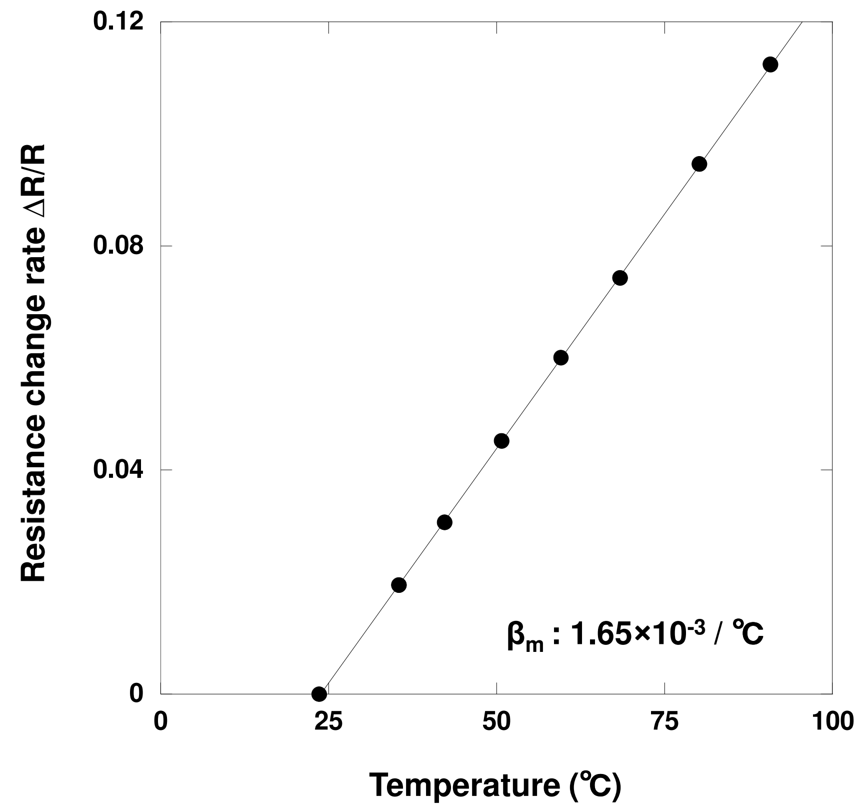
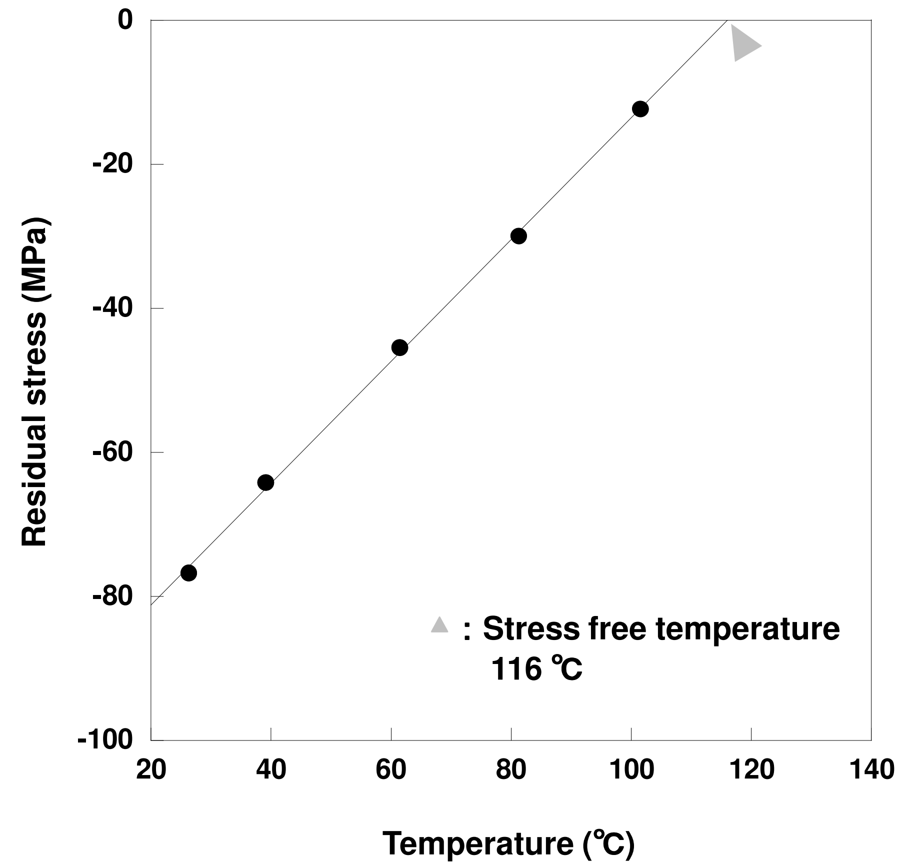


Fig.8 Temperature dependence of coefficient of piezoresistance



(a) Chip 1- Resin A

Fig.9 Temperature dependence of residual stress

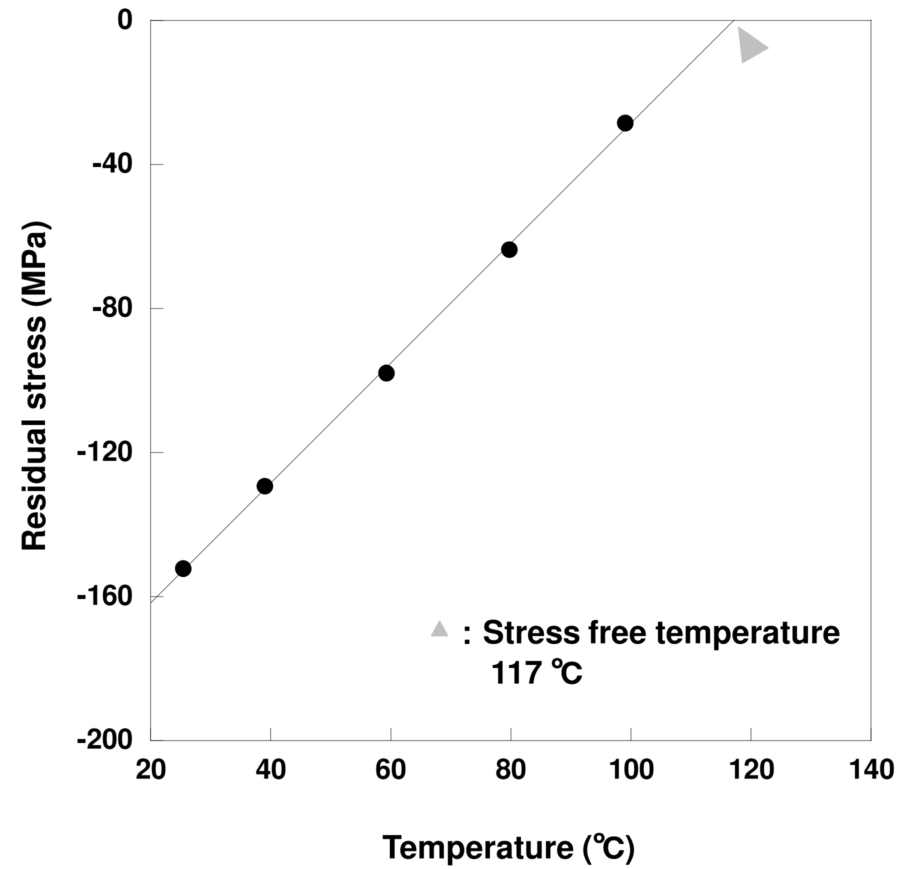
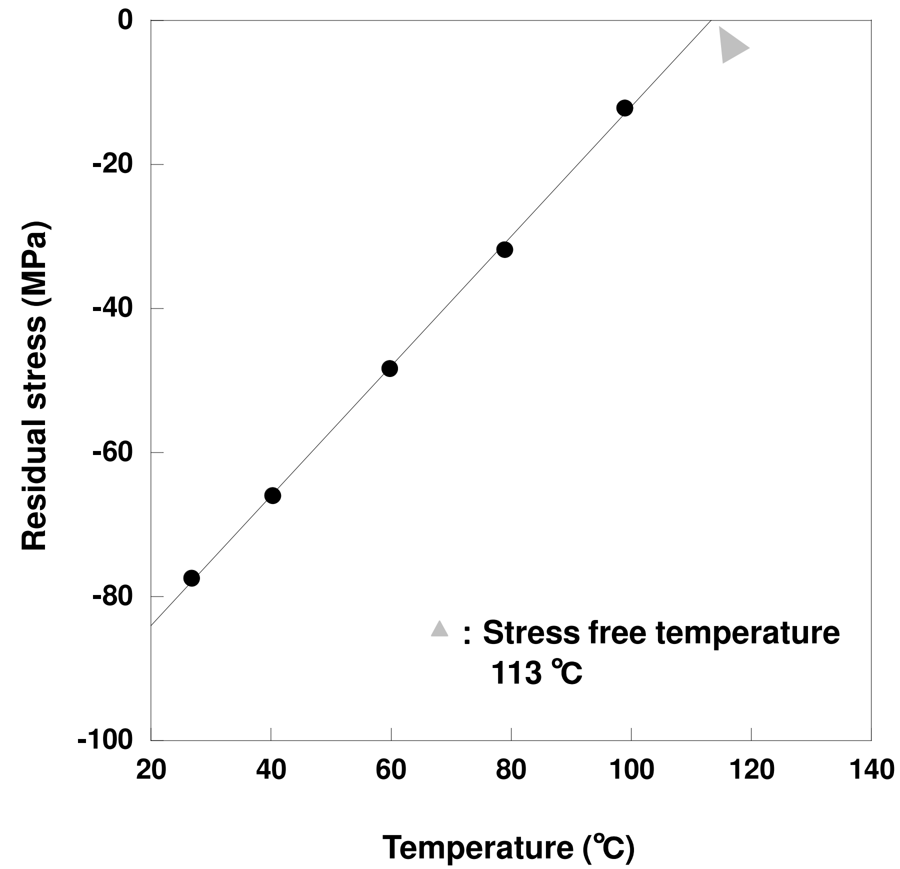


Fig.9 Temperature dependence of residual stress



(c) Chip 2-1- Resin A

Fig.9 Temperature dependence of residual stress

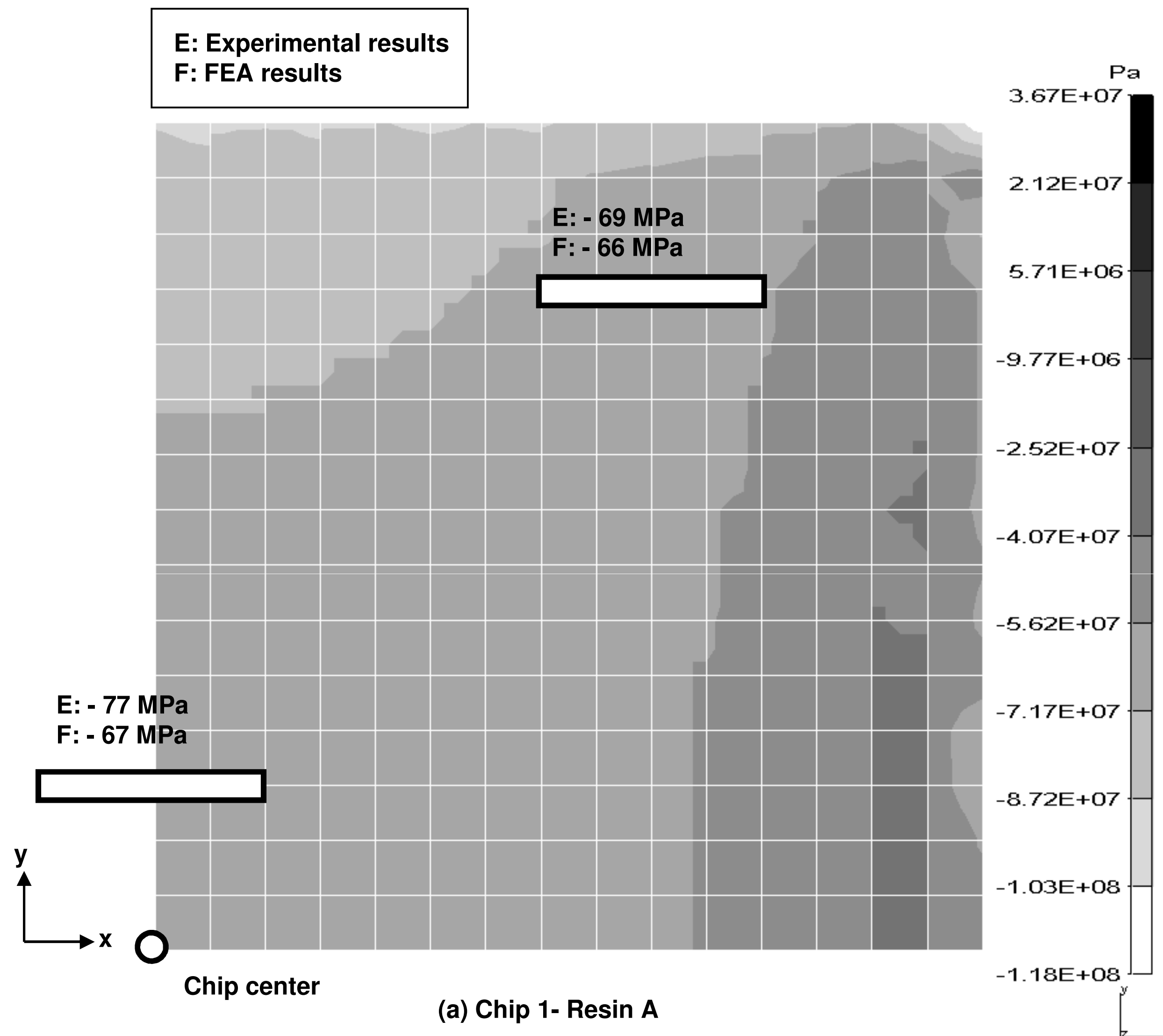


Fig.10 Experimental results and finite element analysis results of residual stress σx in Si chip

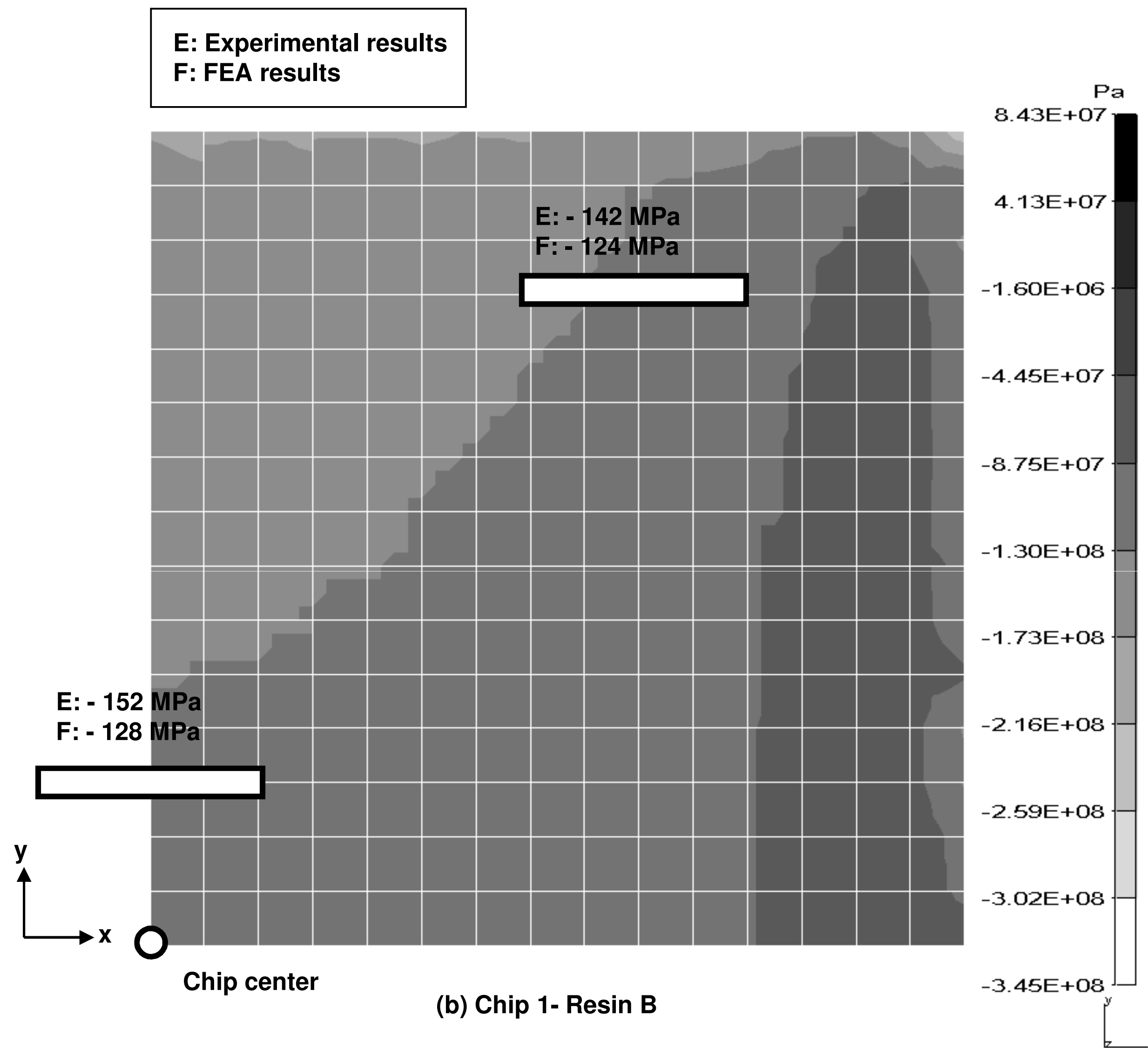
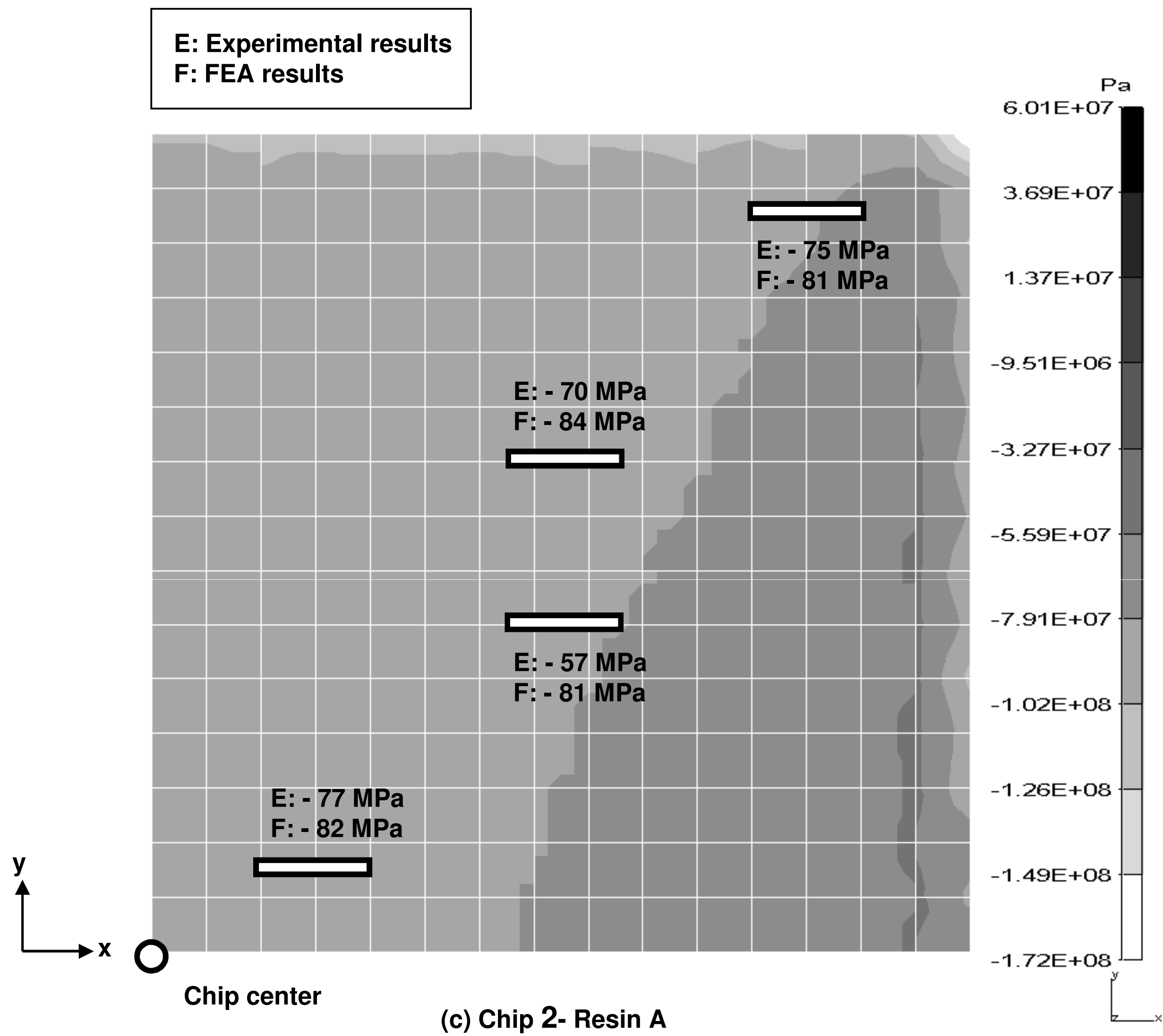


Fig.10 Experimental results and finite element analysis results of residual stress σx in Si chip



(c) Chip 2- Resin A

Fig.10 Experimental results and finite element analysis results of residual stress σx in Si chip

Table 1. Calibration parameters of piezoresistance

Parameter	Value
S : Stress sensibility	**-1.55×10^{-4} /MPa**
α : Thermal dependence coefficient of stress sensibility	**-1.50×10^{-7} /℃**
β : Thermal dependence coefficient of piezoresistance	**1.55×10^{-3} /℃**

Table 2. Material properties used in FEM analysis

	Young's Modulus (GPa)	Poisson's ratio	Coefficient of thermal Expansion ($\times 10^{-6}$/℃)
Si chip	**(Table 3)**	**(Table 3)**	**2.6**
Resin A	**24**	**0.25**	**12.2**
Resin B	**15.6**	**0.24**	**30.1**
Conductive Adhesive paste	**5.39**	**0.4**	**30**
Die pad	**147**	**0.3**	**7**

Table 3. Components of stiffness matrix of silicon [16)]

Crystallographic coordinate system: 1,2,3

c11	**165.7**
c12	**63.9**
c44	**79.6**

Unit: GPa

$$\begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{pmatrix}$$