New single-chip, multicore DSP solution for HSPA enterprise femtocell applications

Texas Instruments

Product Bulletin

The TMS320TCI6489 from Texas Instruments is a high-performance, cost-competitive, single-chip digital signal processor (DSP) solution. Targeted at the demanding enterprise femtocell market, the TCI6489 is capable of supporting PHY and MAC layer processing for 2G, 3G and 4G femtocell base stations, and offers substantial development benefits for manufacturers.

The TCI6489 DSP includes three cores and is capable of supporting 32 users on a single WCDMA carrier. Designed to run both PHY and higher layer processing, it is also capable of supporting 32 users on a single WCDMA carrier. With a broad selection of available analog RF components, the TCI6489 enterprise platform is ideally suited for any femtocell original equipment manufacturer (OEM).

TCI6489 WCDMA enterprise femtocell system parameters

- 32 UEs
- HSDPA up to 15 Mbps
- HSUPA up to 5.7 Mbps
- Cell size < 200 m
- L3/L2/L1 functionality

With TI's TCI6489 femtocell base station solutions, OEMs can use a single device for PHY and full upper-layer processing without incurring excessive research and development expenditures, as a separate RISC processor for Layer 2 and 3 processing is no longer required.

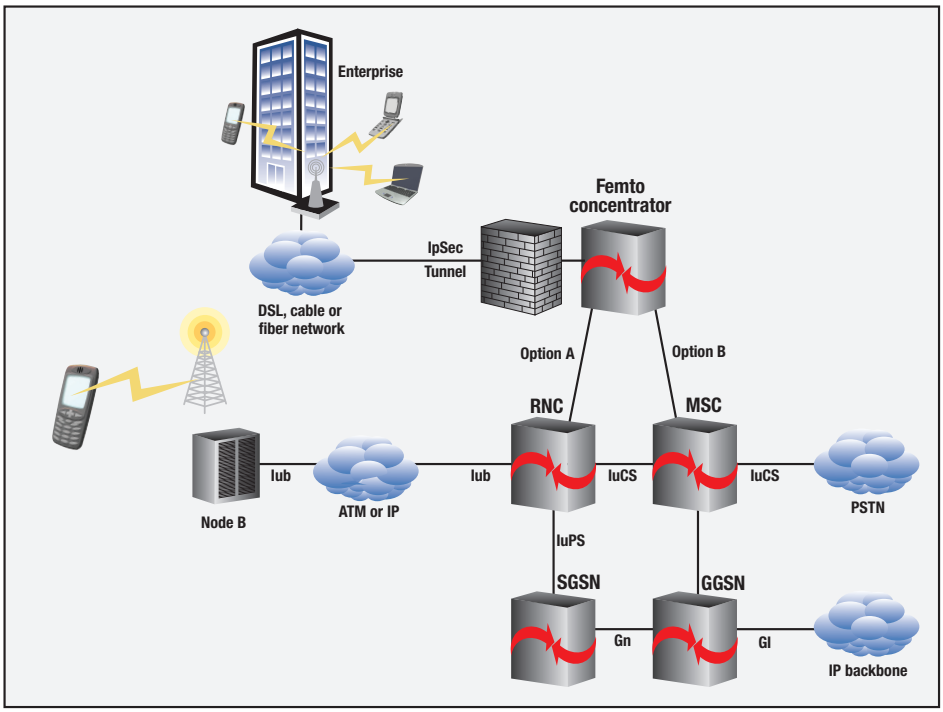
In the office femtocell base stations enhance the wireless experience by bringing higher data rates, better coverage and lower cost plans to the user. A typical femtocell network architecture is shown on next page. The femtocell architecture allows a mobile phone user in enterprise to be connected to a femto base station. This femto base station uses the existing landline connection (typically DSL, cable or fiber) to connect to the wireless operator's network. These femtocell base stations must coexist within the macro base station area and must cope with the challenges of interference, power control and hand off with the macro network.

TI offers a complete software solution for the TCI6489 to reduce manufacturers' time to market and overall development costs, allowing them to respond quickly to these challenges and provide the necessary features and updates operators require. Because TI's solutions are DSP-based and software programmable, OEMs can future-proof their femtocell base station products, thereby appealing to wireless service providers who can easily support new features with field software upgrades.

Key features

TMS320TCI6489 high-performance DSP

- Three 850-MHz, TMS320C64x+™ cores provide flexible processing for supporting different standards
  - Built-in UMTS receiver accelerator coprocessor (RAC)
  - Optimized for wireless baseband applications with turbo and Viterbi decoder coprocessors
  - 1 MB of internal L2 memory per core
  - sGMII Gigabit Ethernet
  - Four antenna interface lanes supporting either OBSAI or CPRI
    - DDR2 667 MHz
  - McBSP – Two McBSP links, each at 100 Mbps
    - McBSP can be used for multichannel clocked serial communications
  - I^2C – One I^2C link at 400 kbps
    - I^2C can be used for communication links between integrated circuits or for peripheral devices on an embedded system
- Ease of programming enables customization combined with fast time to market
  - Allows system developers to make modifications if deployments encounter unexpected issues
  - Speeds time to market for involvement in trials and to obtain critical feedback on solutions
  - Leverages the most comprehensive set of DSP development tools, including TI's Code Composer Studio™ IDE and the DSP/BIOS™ software kernel foundation



A typical femtocell network architecture

Key features continued

- Optimized software for WCDMA
  - Optimized HSPA Layer 1, 2 and 3 software reference design
  - Carrier-class code development provides ease of use and smooth integration

The TCI6489 allows OEMs to address any wireless standard from GSM to LTE. These solutions are also code-compatible with other TI DSPs for the wireless infrastructure market, reusing any previous investments in maco or pico base stations.

High-performance DSP architecture

The TCI6489 DSP is capable of supporting physical layer functionality, including symbol rate, chip rate and full MAC processing. Although femtocells are small in size, they still require powerful performance, as requirements for HSPA femtocells are the same in terms of raw bandwidth as single sectors of macro base stations. While there are simplifications in the RF and in Layer 2 processing, the basic physical layer data rate support is almost equivalent to a single-sector macro.

TI's TCI6489 high-performance DSP has three independent TMS320C64x+™ DSP cores, at the heart of each subsystem. For flexibility, there is 1 MB of L2 SRAM/cache per core on each device. To support wireless applications, each DSP contains a number of specialized coprocessors:

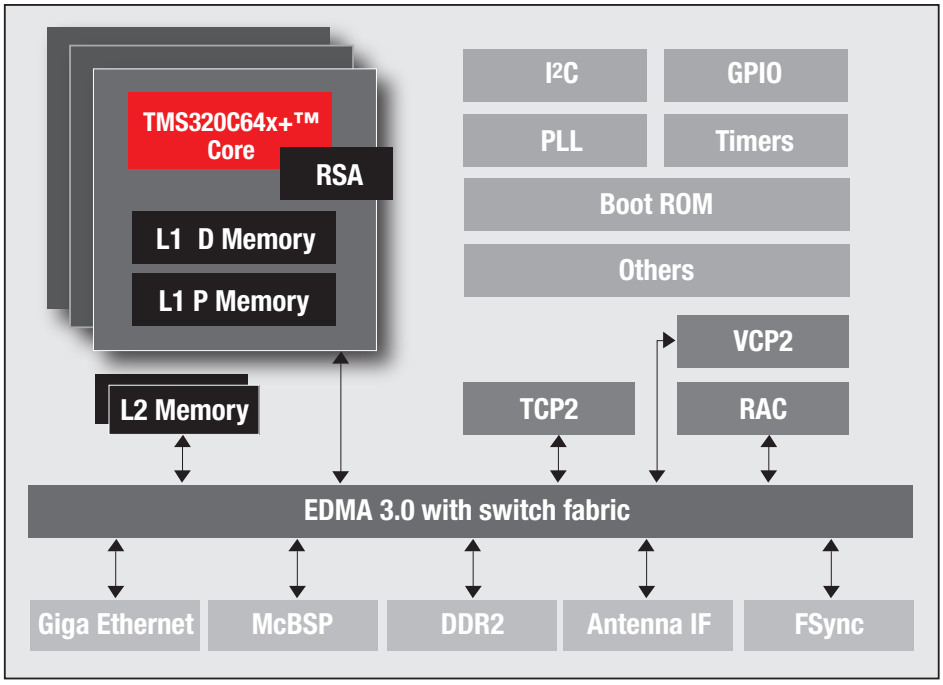
- Viterbi decoder coprocessor 2 (VCP2)
- Turbo decoder coprocessor 2 (TCP2)
- Receiver accelerator coprocessor (RAC)

The RAC subsystem is a chip-rate accelerator, used in the receiver side of the base station and based on a generic correlator coprocessor (GCCP) that supports UMTS-specific operations. The RAC assists in transferring received antenna data to the receive core, performing functions targeted for WCDMA macro base station applications.

These focused set of accelerators deliver the ideal features and performance for any type of femto base station. The subsystem includes two GCCP accelerators, used for finger despread (FD), path search (PS), preamble detection (PD) and stream power estimation (SPE). In addition, the RAC has a back-end interface (BEI) for managing RAC configuration and data output.

Another important feature of the TCI6489 is support of standard interfaces such as Gigabit Ethernet, DDR2 and McBSP.
The TCI6489 supports four AIF lanes, each configurable as either OBSAI or CPRI, with a maximum rate of 3.072 Gbps (OBSAI) and 2.4576 Gbps (CPRI). These features simplify board-level design and further reduce system cost.

Three C64x+™ cores (850 MHz)
3 MB L2 (1 MB per core)
Four AIF lanes



▲ *TCI6489 block diagram*
The TCI6489 has three 850-MHz TMS320C64x+™ DSP cores. Each core includes 1-MB L2 memory.

Layer 1 and 2 processing

The TCI6489 is designed to completely handle the needs of Layer 1 and 2 processing on a single DSP for an enterprise femtocell, with two cores for PHY processing. With 3 MB of internal L2 memory , the TCI6489 is ideally proportioned between performance and memory for femtocells. The TCI6489 is also capable of running Linux for Layer 3 processing using VirtualLogix real-time virtualization software optimized for wireless infrastructure applications.

Transmit chip-rate accelerator using RSA

The DSP subsystem and its associated RSA extensions implement transmit chip-rate processing. The DSP core generates both OVSF and PN codes and provides the multiplied result of these two codes as input to the RSA. The modulated user symbols are also provided as input to the RSA. The RSA applies the code values to the modulated symbols to achieve spreading and scrambling. It is also capable of carrying out the stream aggregation functionality.

WCDMA software reference design

TI has partnered with third-party software suppliers mimoON and Continuous Computing to provide customers with software for Layer 1, 2 and 3 wireless protocol processing (control plane and user plane). This software is 3GPP Release 6 compliant (Release 7 and 8 [LTE] to follow), as well as Femto Forum API-compliant, while also including cognitive radio sniffers and advanced scheduling functions for optimal femtocell performance.

The software is provided in a modular fashion for customization, feature differentiation, and a path for future standards upgrades or modifications. It also supports the Linux operating system for portions of the control plane functionality and higher layers as required.

Other TI components for femtocell base stations

TI offers the industry's broadest portfolio of products for wireless infrastructures, including a complete analog signal chain for femtocell applications. These include digital up- and down-converters, high-speed data converters, and RF products for radio front-end solutions. Other products include power management, timing, backplane interface and standard logic components. TI has a complete end-to-end, analog-to-digital hardware solution for all femtocell base station derivatives in all frequency ranges, bandwidths and capabilities.

Key benefits

- Low-cost, power-efficient baseband designs for enterprise femtocell base stations
  - Single TCI6489 DSP baseband solution
  - Supports both PHY and MAC on each DSP core
  - Targeted UMTS receiver accelerator coprocessor (RAC) as well as VCP2/TCP2 accelerators
- Flexible, software-programmable baseband solution
  - Layers 1, 2 and 3 functionality for WCDMA and eventually LTE
  - Capable of running Linux as necessary
  - Field software upgrades enable emerging applications on existing hardware platforms
  - Single hardware platform supports a varied feature set depending on operator's unique requirements
  - Faster time to market
  - OEMs can reuse their C64x+™ DSP based baseband application software developed for today's macro base stations
  - Software compatibility with legacy C64x+DSP software shortens development time and allows reuse of existing software
  - User-friendly Code Composer Studio™ integrated development environment available to reduce development time and cost

For more information

www.ti.com/femtocell

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